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PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Tx Blanking and SYSCLK on Socket 1 Related Pinouts
DATE:	October 19, 2014
AFFECTED DOCUMENT:	M.2 Spec Rev 1.0
SPONSOR:	Ra'anan Sover; Intel Corp.

Part I

1. Summary of the Functional Changes

The proposed change is to include 2 GNSS Aiding signals, that we already have allocated in the Type 1216 pinout,to the Socket 1 Key E pinout and Type 2226/3026 pinout. Due to lack of free pins in the Key E pinout, it is proposed to define 2 SDIO Input signals as dual functional pins. They would be defined with their original SDIO functionality along with and alternate GNSS Aiding signals functionality to enable a GNSS solution on Type 2230 solutions on Socket 1 Key E solutions. The GNSS signals to be added are the Tx Blanking and SYSCLK signals and it is suggested to overlay them on the SDIO RESET# and SDIO CLK repectively which are also inputs. In this way it is less likely to cause a potential contention.

In the Socket 1 Key E pinout, the actual selection of which functionality is active for a given module would need to be defined between vendor and customer in a BTO/CTO manner.

In the Type 2226/3026 pinout, there is no need for selection as these TX_BLANKING and SYSCLK signals would be replace RESERVED pins similarly to the way and location these signals were added to the Type 1216 pinout in the past.

2. Benefits as a Result of the Changes

Enable a connectorized Connectivity module using Socket 1 Key E and the Type 2226/3026 pinout to benefit from the GNSS Aiding signals provided by the WWAN solution in the same platform similar to that of the soldered down Type 1216 Connectivity module.

3. Assessment of the Impact

SDIO and GNSS Aiding can not be supported simultaneously in the connectorized Socket 1 Key E. It is an either or situation. Either you support SDIO and will not be able to use the GNSS Aiding signals or use the GNSS Aiding signal but no SDIO support. The actual functionality needs to be aligned between vendor and customer in BTO/CTO mode.

No appearent impact to the Type 2226/3026 module as a result of this pinout modification since the pins were previously defined as RESERVED.

4. Analysis of the Hardware Implications

No expected contention because all signals are inputs into the module and all at 1.8V level IO. Although the Vendor-Customer must align on what configuration is being supported/used for correct functionlity.

5. Analysis of the Software Implications

N/A.

6. Analysis of the C&I Test Implications

N/A.

Part II

Detailed Description of the change

Change Table 15 as follows:

			direction dictated by MLDIR	
Communication Specific Signals	SUSCLK	I	Suspend Clock is a 32.768 kHz clock supply input that is provided by platform to enable the add-in card to enter reduce power consumption modes. SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. Accuracy will be up to 200 ppm.	3.3 V
	W_DISABLE1# W_DISABLE2#	I	Active low, debounced signal when applied by the system it will disable radio operation on the add-in cards that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the card.	3.3 V
	LED_1# LED_2#	O	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.	3.3 V
	COEX[1..3]	I/O	Coexistence between WiFi+BT and WWAN on Socket 2	1.8 V
	TX_BLANKING	I	Tx Blanking GNSS Aiding signal from WWAN; Refer to Chapter 3.2.10.3.1 for more details	1.8V
	SYSCLK	I	SYSCLK GNSS Aiding signal from WWAN; Refer to Chapter 3.2.10.3.1 for more details	1.8V
NFC-UIM Signals	UIM_POWER_SRC/GPIO1	I	UICC power out from BB PMU	Per ISO 7816 Specification
	UIM_POWER_SNK	O	NFC PMU power to the UICC	
	SWP	I/O	UICC Secure element	

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Change Table 22 as follows:

Table 22. SDIO Based Module Solution Pinout (Module Key E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PETn1	67
64	RESERVED	RESERVED/PETp1	65
62	ALERT# (O)(0/3.3V)	GND	63
60	I2C_CLK (I)(0/3.3V)	RESERVED/PERn1	61
58	I2C_DATA (I/O)(0/3.3V)	RESERVED/PERp1	59
56	W_DISABLE1# (I)(0/3.3V)	GND	57
54	W_DISABLE2# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (I)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKn0	49
46	COEX2(I/O)(0/1.8V)	REFCLKp0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PETn0	43
40	VENDOR DEFINED	PETp0	41
38	VENDOR DEFINED	GND	39
36	UART CTS (I)(0/1.8V)	PERn0	37
34	UART RTS (O)(0/1.8V)	PERp0	35
32	UART RXD (I)(0/1.8V)	GND	33
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
22	UART TXD (O)(0/1.8V)	SDIO RESET#/TX_BLANKING (I)(0/1.8V)	23
20	UART WAKE# (O)(0/3.3V)	SDIO WAKE# (O)(0/1.8V)	21
18	GND	SDIO DATA3(I/O)(0/1.8V)	19
16	LED2# (O)(OD)	SDIO DATA2(I/O)(0/1.8V)	17
14	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO DATA1(I/O)(0/1.8V)	15
12	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DATA0(I/O)(0/1.8V)	13
10	PCM_SYNC/I2S WS (I/O)(0/1.8V)	SDIO CMD(I/O)(0/1.8V)	11
8	PCM_CLK/I2S SCK (I/O)(0/1.8V)	SDIO CLK/ SYSCLK (I)(0/1.8V)	9
6	LED1# (O)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

Change Table 45 as follows:

Table 45. Socket 1-SD Pin-Out Diagram (Mechanical Key E) (Platform

		GND	75
74	3.3V	RESERVED/REFCLKn1	73
72	3.3V	RESERVED/REFCLKp1	71
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	GND	69
68	UIM_POWER_SNK/CLKREQ1#	RESERVED/PERn1	67
66	UIM_SWP/PERST1#	RESERVED/PERp1	65
64	RESERVED	GND	63
62	ALERT# (I)(0/3.3V)	RESERVED/PETn1	61
60	I2C_CLK (O)(0/3.3V)	RESERVED/PETp1	59
58	I2C_DATA (I/O)(0/3.3V)	GND	57
56	W_DISABLE1# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
54	W_DISABLE2# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
52	PERST0# (O)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (O)(0/3.3V)	REFCLKn0	49
48	COEX1 (I/O)(0/1.8V)	REFCLKp0	47
46	COEX2(I/O)(0/1.8V)	GND	45
44	COEX3(I/O)(0/1.8V)	PERn0	43
42	VENDOR DEFINED	PERp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PETn0	37
36	UART RTS (O)(0/1.8V)	PETp0	35
34	UART CTS (I)(0/1.8V)	GND	33
32	UART TXD (O)(0/1.8V)	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	SDIO RESET#/TX_BLANKING (O)(0/1.8V)	23
22	UART RXD (I)(0/1.8V)	SDIO WAKE# (I)(0/1.8V)	21
20	UART WAKE# (I)(0/3.3V)	SDIO DATA3(I/O)(0/1.8V)	19
18	GND	SDIO DATA2(I/O)(0/1.8V)	17
16	LED2# (I)(OD)	SDIO DATA1(I/O)(0/1.8V)	15
14	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DATA0(I/O)(0/1.8V)	13
12	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO CMD(I/O)(0/1.8V)	11
10	PCM_SYNC/I2S WS (O/I)(0/1.8V)	SDIO CLK/SYSCLK (O)(0/1.8V)	9
8	PCM_CLK/I2S SCK (O/I)(0/1.8V)	GND	7
6	LED1# (I)(OD)	USB_D-	5
4	3.3V	USB_D+	3
2	3.3V	GND	1

Update the Type 2226 pinout diagram in Figure 87 as follows:

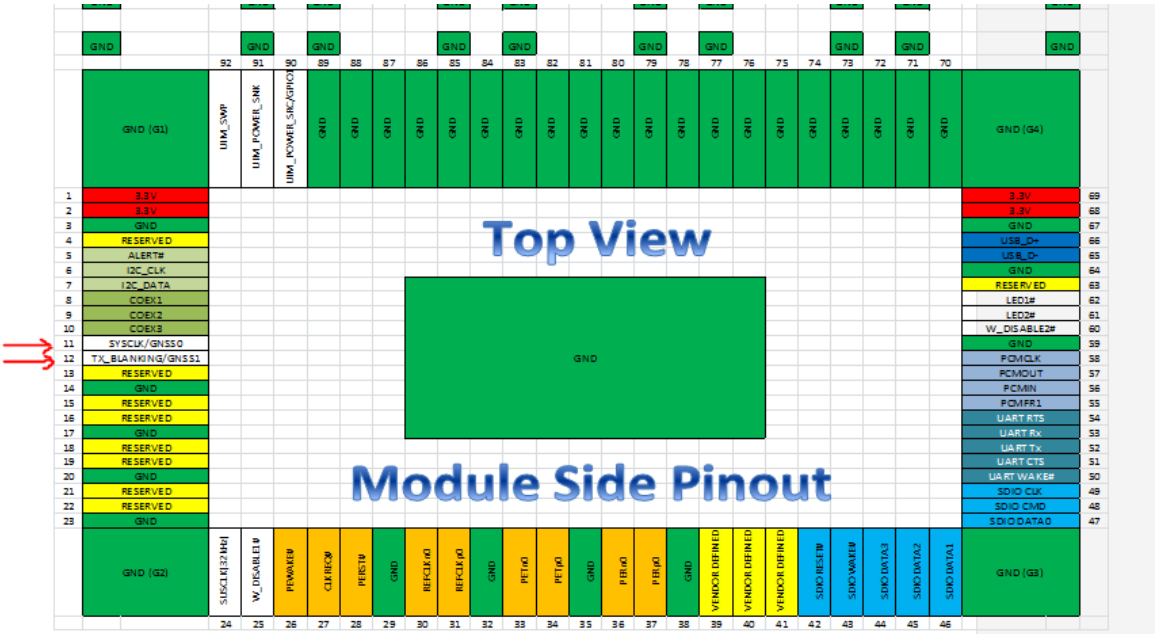

Figure 87. Type 2226 SDIO Based Module-Side Pin-Out

Update the Type 3026 pinout diagram in Figure 89 as follows:

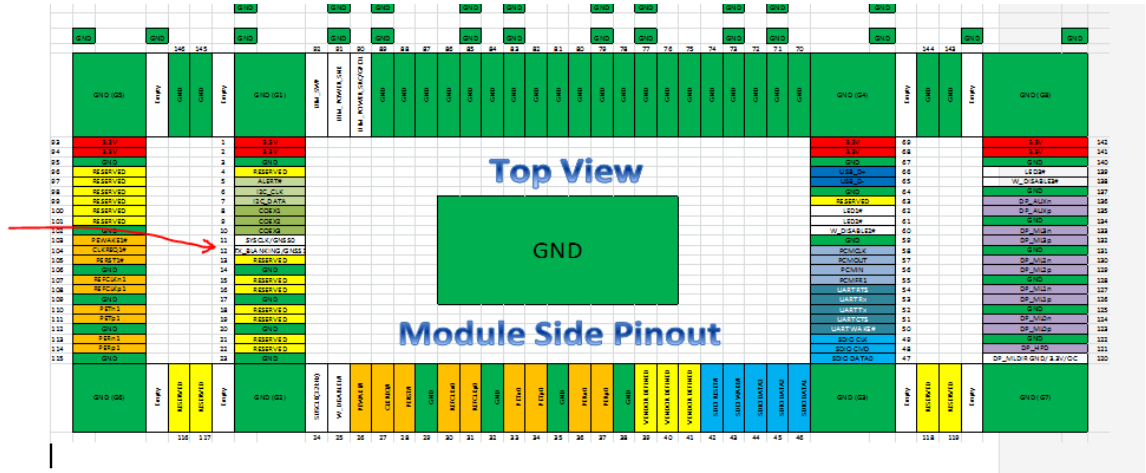

Figure 89. Type 3026 Display Port Pinout Extension Over an SDIO Based Module-Side Pin-Out

Changes to pins 11 & 12

Updated the Text description in Chapter 3.2.10.3.1 to better define the source and usage of the signals as seen in the below:

3.2.10.3.1. GNSS Signals

- **GNSS_SCL**
  Input clock for I2C interface for transfer of location data. External device is bus master. For use as a low power interface for location data when host CPU is in low power mode.
- **GNSS_SDA**
  Bi-directional data interface for I2C. For transfer of location data to/from external device (such as a sensor hub).
- **GNSS_IRQ**
  Interrupt signal – bi directional to provide on demand GNSS data to/from external device (such as a sensor hub). Goal is provide a low power interface for location data when host CPU is in low power mode.
- **SYSCLK**
  A clock generated by the WWAN module to provide a means to synchronize the internal WWAN sub system on the WWAN module to an external GNSS device that may reside on the Connectivity module (e.g. Socket 1) or elsewhere on the platform. Used in conjunction with TX_BLANKING signal. Frequency of operation (and clock type) will be dependent on the specific implementation to be used. This is outside the scope of this standard and must be determined as a BTO feature.
- **TX_BLANKING**
  This signal is active high and will be asserted to ~~signal~~ indicate when the WWAN sub system is engaged in radio transmission activity which would swamp the GNSS signal being received by an off WWAN module GNSS~~external~~ device. This signal is used in conjunction with SYSCLK signal – specific operation will be dependent on the specific implementation to be used. This is outside the scope of this standard and must be determined as a BTO feature.
- **GNSS0..1**
  These are pins reserved for proprietary GNSS functions which will be part of BTO on a vendor specific basis.

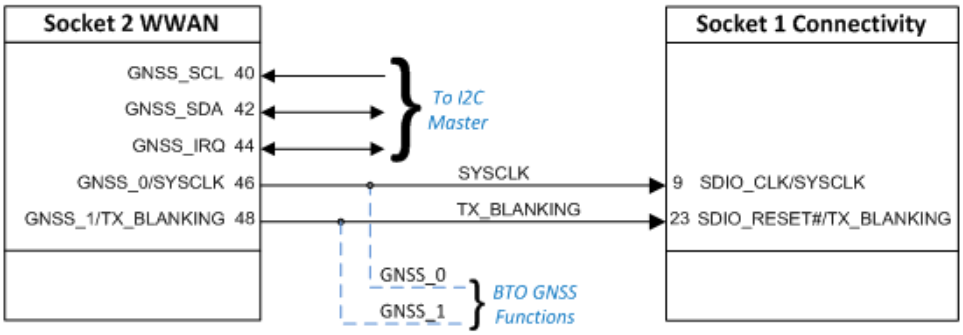

Figure 91. Example Connection of the GNSS Signals in a Platform Using M.2 Modules

Add a complementary diagram showing an example of the connections of the GNSS signals in a platform system as shown above.

All subsequint figure numbers would need to be updated till the end of the document.

Update the Platform sidepinouts for the soldered down solutions. Update Figure 94 (was 93) as follows:

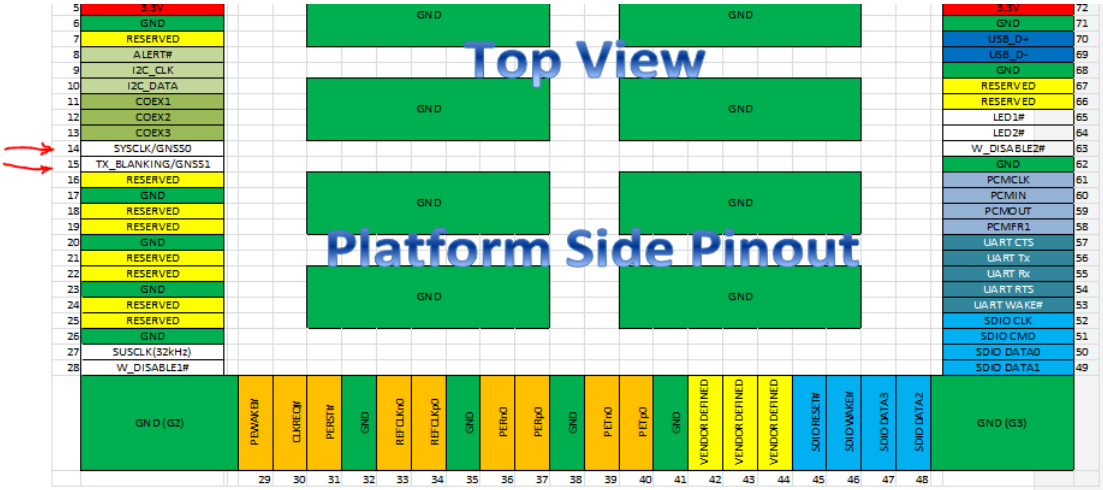

Figure 9493. Type 1216 LGA Pin-Out Using Socket 1-SD Based Pin-Out on Platform

And update Figure 95 (was 94) as follows:

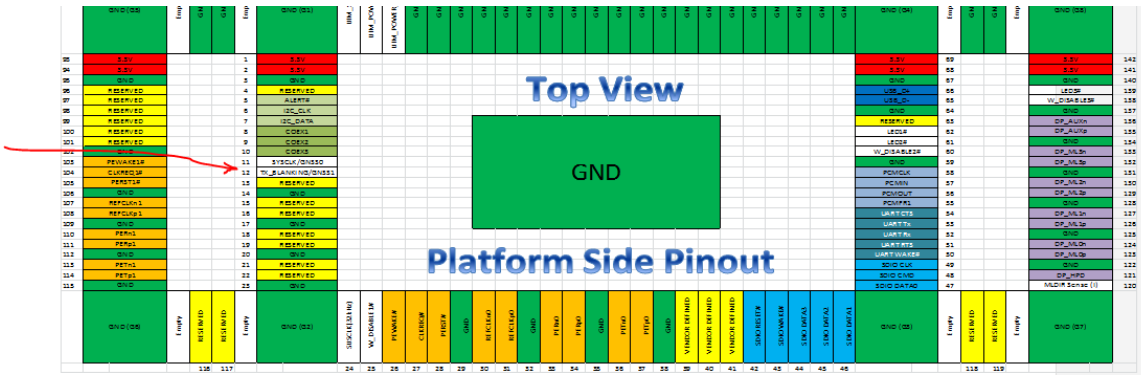

Figure 9594. Type 3026 LGA Pin-Out Using Socket 1-SD & 1-DP Based Pin-Out on Platform