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# PCI-SIG ENGINEERING CHANGE NOTICE

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|---|---|
| **TITLE:** | OCuLink Wiring Chart ECN |
| **DATE:** | September 15, 2017 |
| **AFFECTED DOCUMENT:** | OCuLink 1.0 |
| **SPONSOR:** | Alex Haser (Molex), Jay Neer (Molex) |

## Part I:

### 1. Summary of the Functional Changes

a. The connector and cable assembly pinout tables have been revised to show the complete OCuLink pinout assignments in all cases.
b. The two left-most columns in the cable pinout tables have been combined for clarity.
c. Due to the fact that the pinout tables span multiple pages, P1/P2 designations have been included in the appropriate column titles of the cable pinout tables to make it easier to follow which end of the cable is being addressed on each page in each table.

### 2. Benefits as a Result of the Changes

The changes provided will make it much easier for users to follow the pinouts for the plugs at each end of the cable interface.

### 3. Assessment of the Impact

Less chance of connection errors provides better quality

### 4. Analysis of the Hardware Implications

Less chance of connection errors during design and/or assembly. VSP lines that are recommended for use with REFCLK must be differentially coupled through the cable.

### 5. Analysis of the Software Implications

None

**NOTE:** This ECR incorporates changes from the BP Type and CPRSNT# ECRs.

**Part II:** Sections 2.3, 3.2, 3.3, and 6.7

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# 2.3. Signal Description

## Table 2-1. Signal Description

| Signal | Description |
|---|---|
| … | … |
| 5 V Power | External applications have optional end to end implementations for +5 V supplied by the root only. |
| … | … |

# 3.2. Internal Connector Pinouts

- See Table 6-9 for the Full Crossover Internal Cable wiring.
- The sideband signal assignment differs between the Downstream Port and Upstream Port.
- The Fixed side must provide the 3.3 V to support the optional active cable.

## 3.2.1 Pinout for x4 Fixed Internal Connector (Downstream Port)

**Table 3-1. Pinout for x4 Fixed Internal Connectors (Downstream Port)**

| Mating Level | Description | Pin # | | Description | Mating Level |
|---|---|---|---|---|---|
| Row offset- no pin this side | | | B1 | POWER 5V #1 (see Note 1) | 2nd |
| 2nd | POWER 3.3 Vact #1 (see Note 2) | A1 | B2 | GROUND | 1st |
| 1st | GROUND | A2 | B3 | PETp0 | 2nd |
| 2nd | PERp0 | A3 | B4 | PETn0 | 2nd |
| 2nd | PERn0 | A4 | B5 | GROUND | 1st |
| 1st | GROUND | A5 | B6 | PETp1 | 2nd |
| 2nd | PERp1 | A6 | B7 | PETn1 | 2nd |
| 2nd | PERn1 | A7 | B8 | GROUND | 1st |
| 1st | GROUND | A8 | B9 | 2-WIRE CLOCK | 2nd |
| 2nd | BP TYPE/ VSP (see Note 3) | A9 | B10 | 2-WIRE DATA | 2nd |
| 2nd | CWAKE# (see Note 4) | A10 | B11 | GROUND | 1st |
| 1st | GROUND | A11 | B12 | PERST# | 2nd |
| 2nd | VSP (see Note 5) | A12 | B13 | CPRSNT# | 2nd |
| 2nd | VSP (see Note 5) | A13 | B14 | GROUND | 1st |
| 1st | GROUND | A14 | B15 | PETp2 | 2nd |
| 2nd | PERp2 | A15 | B16 | PETn2 | 2nd |
| 2nd | PERn2 | A16 | B17 | GROUND | 1st |
| 1st | GROUND | A17 | B18 | PETp3 | 2nd |
| 2nd | PERp3 | A18 | B19 | PETn3 | 2nd |
| 2nd | PERn3 | A19 | B20 | GROUND | 1st |
| 1st | GROUND | A20 | B21 | POWER 3.3 Vact #2 (see Note 2) | 2nd |
| 2nd | POWER 5V #2 (see Note 1) | A21 | Row offset- no pin this side | | |

Notes:

1. Option for 5 V power not permitted for internal cables; this pin must not be reassigned.
2. Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.
3. This pin is assigned to report Backplane Type; however, once Backplane Type has been determined, the Controller/Root may use this pin for some other user/ vendor-specific purpose.
4. This pin is permitted to support OBFF in addition to CWAKE#. Refer to the Card Electromechanical (CEM) specification for more information on OBFF.
5. These pins may be used to implement clocking architecture. For information on implementation, refer to Table 2-2.

## 3.2.2 Pinout for x4 Fixed Internal Connector (Upstream Port)

**Table 3-2. Pinout for x4 Fixed Internal Connectors (Upstream Port)**

| Mating Level | Description | Pin # | | Description | Mating Level |
|---|---|---|---|---|---|
| Row offset- no pin this side | | | B1 | POWER 5V #1 (see Note 1) | 2nd |
| 2nd | POWER 3.3 Vact #1 (see Note 2) | A1 | B2 | GROUND | 1st |
| 1st | GROUND | A2 | B3 | PETp0 | 2nd |
| 2nd | PERp0 | A3 | B4 | PETn0 | 2nd |
| 2nd | PERn0 | A4 | B5 | GROUND | 1st |
| 1st | GROUND | A5 | B6 | PETp1 | 2nd |
| 2nd | PERp1 | A6 | B7 | PETn1 | 2nd |
| 2nd | PERn1 | A7 | B8 | GROUND | 1st |
| 1st | GROUND | A8 | B9 | BP TYPE/ VSP (see Note 3) | 2nd |
| 2nd | 2-WIRE CLOCK | A9 | B10 | CWAKE# (see Note 4) | 2nd |
| 2nd | 2-WIRE DATA | A10 | B11 | GROUND | 1st |
| 1st | GROUND | A11 | B12 | VSP (see Note 5) | 2nd |
| 2nd | PERST# | A12 | B13 | VSP (see Note 5) | 2nd |
| 2nd | CPRSNT# | A13 | B14 | GROUND | 1st |
| 1st | GROUND | A14 | B15 | PETp2 | 2nd |
| 2nd | PERp2 | A15 | B16 | PETn2 | 2nd |
| 2nd | PERn2 | A16 | B17 | GROUND | 1st |
| 1st | GROUND | A17 | B18 | PETp3 | 2nd |
| 2nd | PERp3 | A18 | B19 | PETn3 | 2nd |
| 2nd | PERn3 | A19 | B20 | GROUND | 1st |
| 1st | GROUND | A20 | B21 | POWER 3.3 Vact #2 (see Note 2) | 2nd |
| 2nd | POWER 5V #2 (see Note 1) | A21 | Row offset- no pin this side | | |

Notes:

1. Option for 5 V power not permitted for internal cables; this pin must not be reassigned.
2. Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.
3. This pin is assigned to report Backplane Type; however, once Backplane Type has been determined, the Controller/Root may use the pin for some other user/ vendor-specific purpose.
4. This pin is permitted to support OBFF in addition to CWAKE#. Refer to the Card Electromechanical (CEM) specification for more information on OBFF.
5. These pins may be used to implement clocking architecture. For information on implementation, refer to Table 2-2.

# 3.3 External Connector Pinouts

- See Table 6-10 for x4 Free External Passive and Active Cable wiring.
- The sideband signal assignment is the same on the Downstream Port and Upstream Port.
- The Fixed side must provide the 3.3 V to support the optional active cable.
- The Fixed side must provide the 5 V for to support optional Power.

## 3.3.1 Pinout for x4 Fixed External Connectors (Upstream Port & Downstream Port)

**Table 3-3. Pinout for x4 Fixed External Connector (Upstream Port & Downstream Port)**

| Mating Level | Description | Pin # | | Description | Mating Level |
|---|---|---|---|---|---|
| Row offset- no pin this side | | | B1 | POWER 5V #1 (see Note 1) | 2nd |
| 2nd | POWER 3.3 Vact #1 (see Note 2) | A1 | B2 | GROUND | 1st |
| 1st | GROUND | A2 | B3 | PETp0 | 2nd |
| 2nd | PERp0 | A3 | B4 | PETn0 | 2nd |
| 2nd | PERn0 | A4 | B5 | GROUND | 1st |
| 1st | GROUND | A5 | B6 | PETp1 | 2nd |
| 2nd | PERp1 | A6 | B7 | PETn1 | 2nd |
| 2nd | PERn1 | A7 | B8 | GROUND | 1st |
| 1st | GROUND | A8 | B9 | 2-WIRE CLOCK | 2nd |
| 2nd | UNASSIGNED | A9 | B10 | 2-WIRE DATA | 2nd |
| 2nd | CWAKE# (see Note 3) | A10 | B11 | GROUND | 1st |
| 1st | GROUND | A11 | B12 | PERST# | 2nd |
| 2nd | VSP (see Note 4) | A12 | B13 | CPRSNT# | 2nd |
| 2nd | VSP (see Note 4) | A13 | B14 | GROUND | 1st |
| 1st | GROUND | A14 | B15 | PETp2 | 2nd |
| 2nd | PERp2 | A15 | B16 | PETn2 | 2nd |
| 2nd | PERn2 | A16 | B17 | GROUND | 1st |
| 1st | GROUND | A17 | B18 | PETp3 | 2nd |
| 2nd | PERp3 | A18 | B19 | PETn3 | 2nd |
| 2nd | PERn3 | A19 | B20 | GROUND | 1st |
| 1st | GROUND | A20 | B21 | POWER 3.3 Vact #2 (see Note 2) | 2nd |
| 2nd | POWER 5V #2 (see Note 1) | A21 | Row offset- no pin this side | | |

Notes:

1. Assigned for optional 5V power only; reassignment of this pin is not permitted. Pins must not be commoned; e.g., pins must be able to operate independently of each other.
2. Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.
3. This pin is permitted to support OBFF in addition to CWAKE#. Refer to the Card Electromechanical (CEM) specification for more information on OBFF.
4. These pins may be used to implement clocking architecture. For information on implementation, refer to Table 2-2.

# 6.7 Free Cable Assembly Wiring Charts

Internal and External cable assemblies are not interchangeable; refer to sections 6.7.1 and 6.7.2 for details regarding Internal and External cables, respectively.

## 6.7.1. Wiring Chart for x4 Internal Cables

- See Table 3-1 and Table 3-2 for Internal cable pinouts.
- Passive and Active cable assemblies are the same; they are crossover cables.
- Active cables are defined as having active components only within the cable plug.
- The Fixed side must provide the 3.3 V to support optional active cable plugs (no wire passes down the cable).

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## Table 6-9. Wiring Chart for x4 Internal Passive and Active Crossover Cables

| P1 Row Position | Downstream Port | Cable Termination & Signal Direction | Upstream Port | P2 Row Position |
|---|---|---|---|---|
| A1 (Bevel) | POWER 3.3 Vact #1 (see Note 1) | NO WIRE | POWER 5V #1 (see Note 5) | B1 |
| A2 | GROUND | ——— | GROUND | B2 |
| A3 | PERp0 | ← | PETp0 | B3 |
| A4 | PERn0 | ← | PETn0 | B4 |
| A5 | GROUND | ——— | GROUND | B5 |
| A6 | PERp1 | ← | PETp1 | B6 |
| A7 | PERn1 | ← | PETn1 | B7 |
| A8 | GROUND | ——— | GROUND | B8 |
| A9 | BP TYPE/ VSP (see Note 2) | <-------- | BP TYPE/ VSP (see Note 2) | B9 |
| A10 | CWAKE# (see Note 3) | <-------- | CWAKE# (see Note 3) | B10 |
| A11 | GROUND | ——— | GROUND | B11 |
| A12 | VSP (see Note 4) | ——— | VSP | B12 |
| A13 | VSP (see Note 4) | ——— | VSP | B13 |
| A14 | GROUND | ——— | GROUND | B14 |
| A15 | PERp2 | ← | PETp2 | B15 |
| A16 | PERn2 | ← | PETn2 | B16 |
| A17 | GROUND | ——— | GROUND | B17 |
| A18 | PERp3 | ← | PETp3 | B18 |
| A19 | PERn3 | ← | PETn3 | B19 |
| A20 | GROUND | ——— | GROUND | B20 |
| A21 | POWER 5V #2 (see Note 5) | NO WIRE | POWER 3.3 Vact #2 (see Note 1) | B21 |

*Table continued on next page.*

## Table 6-9. Wiring Chart for x4 Internal Passive and Active Crossover Cables (continued from previous page)

| P1 Row Position | Downstream Port | Cable Termination & Signal Direction | Upstream Port | P2 Row Position |
|---|---|---|---|---|
| B1 | POWER 5V #1 (see Note 5) | NO WIRE | POWER 3.3 Vact #1 (see Note 1) | A1 (Bevel) |
| B2 | GROUND | — | GROUND | A2 |
| B3 | PETp0 | → | PERp0 | A3 |
| B4 | PETn0 | → | PERn0 | A4 |
| B5 | GROUND | — | GROUND | A5 |
| B6 | PETp1 | → | PERp1 | A6 |
| B7 | PETn1 | → | PERn1 | A7 |
| B8 | GROUND | — | GROUND | A8 |
| B9 | 2-WIRE CLOCK | ↔ | 2-WIRE CLOCK | A9 |
| B10 | 2-WIRE DATA | ↔ | 2-WIRE DATA | A10 |
| B11 | GROUND | — | GROUND | A11 |
| B12 | PERST# | → | PERST# | A12 |
| B13 | CPRSNT# | ← | CPRSNT# | A13 |
| B14 | GROUND | — | GROUND | A14 |
| B15 | PETp2 | → | PERp2 | A15 |
| B16 | PETn2 | → | PERn2 | A16 |
| B17 | GROUND | — | GROUND | A17 |
| B18 | PETp3 | → | PERp3 | A18 |
| B19 | PETn3 | → | PERn3 | A19 |
| B20 | GROUND | — | GROUND | A20 |
| B21 | POWER 3.3 Vact #2 (see Note 1) | NO WIRE | POWER 5V #2 (see Note 5) | A21 |

Notes:

1. Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.
2. If this pin is used for BP Type, the signal direction is from Upstream Port to Downstream Port. If this pin is used for VSP, the signal direction is defined by the vendor.
3. If this pin is used for CWAKE#, the signal direction is from Upstream Port to Downstream Port. If this pin is used for OBFF and both ends support OBFF, the signal becomes bidirectional. Refer to the Card Electromechanical (CEM) specification for more information on OBFF.
4. These wires must be built to support the transmission of low speed, differential signals. They may be used to implement clocking architecture; for information on implementation, refer to Table 2-2.
5. Option for 5 V power not permitted for internal cables; this pin must not be reassigned.

# 6.7.2. Wiring Chart for x4 External Cables

- See External Connector Pinout Table 3-3.
- This is not a full crossover cable; only the high speed lines crossover.
- The wiring charts for Passive and Active cable assemblies are the same.
- Active cables are defined as having active components only within the cable plug.
- The Fixed side must provide the 3.3 V to support optional active cable plugs (no wire passes down the cable).
- The Fixed side must provide the 5 V for Optional Power cables.

### Table 6-10. Wiring Chart for x4 External Passive and Active Cables; with and without Power

| P1 Row Position | Downstream Port | Cable Termination & Signal Direction | Upstream Port | P2 Row Position |
|---|---|---|---|---|
| A1 (Bevel) | POWER 3.3 Vact #1 (see Note 1) | NO WIRE | POWER 3.3 Vact #1 (see Note 1) | A1 (Bevel) |
| A2 | GROUND | ——— | GROUND | B2 |
| A3 | PERp0 | ←——— | PETp0 | B3 |
| A4 | PERn0 | ←——— | PETn0 | B4 |
| A5 | GROUND | ——— | GROUND | B5 |
| A6 | PERp1 | ←——— | PETp1 | B6 |
| A7 | PERn1 | ←——— | PETn1 | B7 |
| A8 | GROUND | ——— | GROUND | B8 |
| A9 | UNASSIGNED | ——— | UNASSIGNED | A9 |
| A10 | CWAKE# (see Note 2) | <-------- | CWAKE# (see Note 2) | A10 |
| A11 | GROUND | ——— | GROUND | B11 |
| A12 | VSP (see Note 4) | ——— | VSP (see Note 4) | A12 |
| A13 | VSP (see Note 4) | ——— | VSP (see Note 4) | A13 |
| A14 | GROUND | ——— | GROUND | B14 |
| A15 | PERp2 | ←——— | PETp2 | B15 |
| A16 | PERn2 | ←——— | PETn2 | B16 |
| A17 | GROUND | ——— | GROUND | B17 |
| A18 | PERp3 | ←——— | PETp3 | B18 |
| A19 | PERn3 | ←——— | PETn3 | B19 |
| A20 | GROUND | ——— | GROUND | B20 |
| A21 | POWER 5V #2 (see Note 3) | AS NEEDED | POWER 5V #2 (see Note 3) | A21 |

*Table continued on next page.*

## Table 6-10. Wiring Chart for x4 External Passive and Active Crossover Cables, with and without Power (continued from previous page)

| P1 Row Position | Downstream Port | Cable Termination & Signal Direction | Upstream Port | P2 Row Position |
|---|---|---|---|---|
| B1 | POWER 5V #1 (see Note 3) | AS NEEDED | POWER 5V #1 (see Note 3) | B1 |
| B2 | GROUND | ——— | GROUND | A2 |
| B3 | PETp0 | ——→ | PERp0 | A3 |
| B4 | PETn0 | ——→ | PERn0 | A4 |
| B5 | GROUND | ——— | GROUND | A5 |
| B6 | PETp1 | ——→ | PERp1 | A6 |
| B7 | PETn1 | ——→ | PERn1 | A7 |
| B8 | GROUND | ——— | GROUND | A8 |
| B9 | 2-WIRE CLOCK | AS NEEDED | 2-WIRE CLOCK | B9 |
| B10 | 2-WIRE DATA | AS NEEDED | 2-WIRE DATA | B10 |
| B11 | GROUND | ——— | GROUND | A11 |
| B12 | PERST# | ——→ | PERST# | B12 |
| B13 | CPRSNT# | ←—— | CPRSNT# | B13 |
| B14 | GROUND | ——— | GROUND | A14 |
| B15 | PETp2 | ——→ | PERp2 | A15 |
| B16 | PETn2 | ——→ | PERn2 | A16 |
| B17 | GROUND | ——— | GROUND | A17 |
| B18 | PETp3 | ——→ | PERp3 | A18 |
| B19 | PETn3 | ——→ | PERn3 | A19 |
| B20 | GROUND | ——— | GROUND | A20 |
| B21 | POWER 3.3 Vact #2 (see Note 1) | NO WIRE | POWER 3.3 Vact #2 (see Note 1) | B21 |

Notes:

1. Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.
2. If this pin is used for CWAKE#, the signal direction is from Upstream Port to Downstream Port. If this pin is used for OBFF and both ends support OBFF, the signal becomes bidirectional. Refer to the Card Electromechanical (CEM) specification for more information on OBFF.
3. Assigned for use with optional 5V power only; reassignment of this pin is not permitted. Pins must not be commoned; e.g., pins must be able to operate independently of each other.
4. These wires must be built to support the transmission of low speed, differential signals. They may be used to implement clocking architecture; for information on implementation, refer to Table 2-2.