



PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	OCuLink Wiring Chart ECN
DATE:	September 15, 2017
AFFECTED DOCUMENT:	OCuLink 1.0
SPONSOR:	Alex Haser (Molex), Jay Neer (Molex)

Part I:

1. Summary of the Functional Changes

- a. The connector and cable assembly pinout tables have been revised to show the complete OCuLink pinout assignments in all cases.
- b. The two left-most columns in the cable pinout tables have been combined for clarity.
- c. Due to the fact that the pinout tables span multiple pages, P1/P2 designations have been included in the appropriate column titles of the cable pinout tables to make it easier to follow which end of the cable is being addressed on each page in each table.

2. Benefits as a Result of the Changes

The changes provided will make it much easier for users to follow the pinouts for the plugs at each end of the cable interface.

3. Assessment of the Impact

Less chance of connection errors provides better quality

4. Analysis of the Hardware Implications

Less chance of connection errors during design and/or assembly. VSP lines that are recommended for use with REFCLK must be differentially coupled through the cable.

5. Analysis of the Software Implications

None

NOTE: This ECR incorporates changes from the BP Type and CPRSNT# ECRs.

Part II: Sections 2.3, 3.2, 3.3, and 6.7

2.3. Signal Description

Table 2-1. Signal Description

Signal	Description
...	...
5 V Power	External applications have optional end to end implementations for +5 V supplied by the root only.
...	...

3.2. Internal Connector Pinouts

- [□ See Table 6-9 for the Full Crossover Internal Cable wiring.](#)
- [□ The sideband signal assignment differs between the Downstream Port and Upstream Port.](#)
- [□ The Fixed side must provide the 3.3 V to support the optional active cable.](#)

3.2.1 Pinout for x4 Fixed Internal Connector (Downstream Port~~root~~)

- ~~□ See Table 6-9 for the Full Crossover Internal Cable wiring.~~
- ~~□ The sideband signal assignment differs between the root and end point.~~
- ~~□ The Fixed side must provide the 3.3 V to support the optional active cable~~

Table 3-1. Pinout for x4 Fixed Internal Connectors (Downstream Port~~root~~)

Pin #	Description	Mating Sequence of cable to board		Pin #	Description
Row Offset — no pin this side			2nd	B1	RESERVED
A1	POWER 3.3 Vact RX	2nd	1st	B2	GROUND
A2	GROUND	1st	2nd	B3	PETp0
A3	PERp0	2nd	2nd	B4	PETn0
A4	PERn0	2nd	1st	B5	GROUND
A5	GROUND	1st	2nd	B6	PETp1
A6	PERp1	2nd	2nd	B7	PETn1
A7	PERn1	2nd	1st	B8	GROUND
A8	GROUND	1st	2nd	B9	2-WIRE CLOCK
A9	BP TYPE	2nd	2nd	B10	2-WIRE DATA
A10	CWAKE#	2nd	1st	B11	GROUND
A11	GROUND	1st	2nd	B12	-PERST#
A12	VSP	2nd	2nd	B13	CPRSNT#
A13	VSP	2nd	1st	B14	GROUND
A14	GROUND	1st	2nd	B15	PETp2
A15	PERp2	2nd	2nd	B16	PETn2
A16	PERn2	2nd	1st	B17	GROUND
A17	GROUND	1st	2nd	B18	PETp3
A18	PERp3	2nd	2nd	B19	PETn3
A19	PERn3	2nd	1st	B20	GROUND
A20	GROUND	1st	2nd	B21	POWER 3.3 Vact TX
A21	-RESERVED	2nd	Row Offset — no pin this side		

NOTICE NOTICE NOTICE NOTICE NOTICE

<u>Mating Level</u>	<u>Description</u>	<u>Pin #</u>		<u>Description</u>	<u>Mating Level</u>
	<u>Row offset- no pin this side</u>		<u>B1</u>	<u>POWER 5V #1 (see Note 1)</u>	<u>2nd</u>
<u>2nd</u>	<u>POWER 3.3 Vact #1 (see Note 2)</u>	<u>A1</u>	<u>B2</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A2</u>	<u>B3</u>	<u>PETp0</u>	<u>2nd</u>
<u>2nd</u>	<u>PERp0</u>	<u>A3</u>	<u>B4</u>	<u>PETn0</u>	<u>2nd</u>
<u>2nd</u>	<u>PERn0</u>	<u>A4</u>	<u>B5</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A5</u>	<u>B6</u>	<u>PETp1</u>	<u>2nd</u>
<u>2nd</u>	<u>PERp1</u>	<u>A6</u>	<u>B7</u>	<u>PETn1</u>	<u>2nd</u>
<u>2nd</u>	<u>PERn1</u>	<u>A7</u>	<u>B8</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A8</u>	<u>B9</u>	<u>2-WIRE CLOCK</u>	<u>2nd</u>
<u>2nd</u>	<u>BP TYPE/ VSP (see Note 3)</u>	<u>A9</u>	<u>B10</u>	<u>2-WIRE DATA</u>	<u>2nd</u>
<u>2nd</u>	<u>CWAKE# (see Note 4)</u>	<u>A10</u>	<u>B11</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A11</u>	<u>B12</u>	<u>PERST#</u>	<u>2nd</u>
<u>2nd</u>	<u>VSP (see Note 5)</u>	<u>A12</u>	<u>B13</u>	<u>CPRSNT#</u>	<u>2nd</u>
<u>2nd</u>	<u>VSP (see Note 5)</u>	<u>A13</u>	<u>B14</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A14</u>	<u>B15</u>	<u>PETp2</u>	<u>2nd</u>
<u>2nd</u>	<u>PERp2</u>	<u>A15</u>	<u>B16</u>	<u>PETn2</u>	<u>2nd</u>
<u>2nd</u>	<u>PERn2</u>	<u>A16</u>	<u>B17</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A17</u>	<u>B18</u>	<u>PETp3</u>	<u>2nd</u>
<u>2nd</u>	<u>PERp3</u>	<u>A18</u>	<u>B19</u>	<u>PETn3</u>	<u>2nd</u>
<u>2nd</u>	<u>PERn3</u>	<u>A19</u>	<u>B20</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A20</u>	<u>B21</u>	<u>POWER 3.3 Vact #2 (see Note 2)</u>	<u>2nd</u>
<u>2nd</u>	<u>POWER 5V #2 (see Note 1)</u>	<u>A21</u>	<u>Row offset- no pin this side</u>		

Notes:

1. Option for 5 V power not permitted for internal cables; this pin must not be reassigned.
2. Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.
3. This pin is assigned to report Backplane Type; however, once Backplane Type has been determined, the Controller/Root may use this pin for some other user/ vendor-specific purpose.
4. This pin is permitted to support OBFF in addition to CWAKE#. Refer to the Card Electromechanical (CEM) specification for more information on OBFF.
5. These pins may be used to implement clocking architecture. For information on implementation, refer to Table 2-2.

3.2.2 Pinout for x4 Fixed Internal Connector (Upstream Port ~~end point~~)

- ~~□ See Table 6-9 for the Full-Crossover Internal Cable wiring.~~
- ~~□ The sideband signal assignment differs between the root and end point.~~
- ~~□ The Fixed side must provide the 3.3 V to support the optional active cable.~~

Table 3-2. Pinout for x4 Fixed Internal Connectors (Upstream Port ~~end point~~)

Mating Level	Description	Pin #		Description	Mating Level
	Row offset- no pin this side		B1	POWER 5V #1 (see Note 1)	2 nd
2 nd	POWER 3.3 Vact #1 (see Note 2)	A1	B2	GROUND	1 st
1 st	GROUND	A2	B3	PETp0	2 nd
2 nd	PERp0	A3	B4	PETn0	2 nd
2 nd	PERn0	A4	B5	GROUND	1 st
1 st	GROUND	A5	B6	PETp1	2 nd
2 nd	PERp1	A6	B7	PETn1	2 nd
2 nd	PERn1	A7	B8	GROUND	1 st
1 st	GROUND	A8	B9	BP TYPE/ VSP (see Note 3)	2 nd
2 nd	2-WIRE CLOCK	A9	B10	CWAKE# (see Note 4)	2 nd
2 nd	2-WIRE DATA	A10	B11	GROUND	1 st
1 st	GROUND	A11	B12	VSP (see Note 5)	2 nd
2 nd	PERST#	A12	B13	VSP (see Note 5)	2 nd
2 nd	CPRSNT#	A13	B14	GROUND	1 st
1 st	GROUND	A14	B15	PETp2	2 nd
2 nd	PERp2	A15	B16	PETn2	2 nd
2 nd	PERn2	A16	B17	GROUND	1 st
1 st	GROUND	A17	B18	PETp3	2 nd
2 nd	PERp3	A18	B19	PETn3	2 nd
2 nd	PERn3	A19	B20	GROUND	1 st
1 st	GROUND	A20	B21	POWER 3.3 Vact #2 (see Note 2)	2 nd
2 nd	POWER 5V #2 (see Note 1)	A21	Row offset- no pin this side		

Notes:

1. Option for 5 V power not permitted for internal cables; this pin must not be reassigned.
2. Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.

NOTICE NOTICE NOTICE NOTICE NOTICE

3. [This pin is assigned to report Backplane Type; however, once Backplane Type has been determined, the Controller/Root may use the pin for some other user/ vendor-specific purpose.](#)
4. [This pin is permitted to support OBFF in addition to CWAKE#. Refer to the Card Electromechanical \(CEM\) specification for more information on OBFF.](#)
5. [These pins may be used to implement clocking architecture. For information on implementation, refer to Table 2-2.](#)

Pin #	Description	Mating Sequence of cable to board		Pin #	Description
Row-Offset — no pin this side		2nd		B1	RESERVED
A1	POWER 3.3 Vact-RX	2nd	1st	B2	GROUND
A2	GROUND	1st	2nd	B3	PETp0
A3	PERp0	2nd	2nd	B4	PETn0
A4	PERn0	2nd	1st	B5	GROUND
A5	GROUND	1st	2nd	B6	PETp1
A6	PERp1	2nd	2nd	B7	PETn1
A7	PERn1	2nd	1st	B8	GROUND
A8	GROUND	1st	2nd	B9	BP-TYPE
A9	2-WIRE-CLOCK	2nd	2nd	B10	CWAKE#
A10	2-WIRE-DATA	2nd	1st	B11	GROUND
A11	GROUND	2nd	2nd	B12	VSP
A12	PERST#	2nd	2nd	B13	VSP
A13	CPRSNT#	2nd	1st	B14	GROUND
A14	GROUND	1st	2nd	B15	PETp2
A15	PERp2	2nd	2nd	B16	PETn2
A16	PERn2	2nd	1st	B17	GROUND
A17	GROUND	1st	2nd	B18	PETp3
A18	PERp3	2nd	2nd	B19	PETn3
A19	PERn3	2nd	1st	B20	GROUND
A20	GROUND	1st	2nd	B21	POWER 3.3 Vact-TX
A21	RESERVED	2nd	Row-Offset — no pin this side		

3.3 External Connector Pinouts

- [□ See Table 6-10 for x4 Free External Passive and Active Cable wiring.](#)
- [□ The sideband signal assignment is the same on the Downstream Port and Upstream Port.](#)
- [□ The Fixed side must provide the 3.3 V to support the optional active cable.](#)
- [□ The Fixed side must provide the 5 V for to support optional Power.](#)

3.3.1 Pinout for x4 Fixed External Connectors (Upstream Port & Downstream Port~~root and end point~~)

- ~~□ See Table 6-10 for x4 Free External Passive and Active Cable wiring.~~
- ~~□ The sideband signal assignment is the same on the root and end point.~~
- ~~□ The Fixed side must provide the 3.3 V to support the optional active cable.~~
- ~~□ The Fixed side must provide the 5 V for optional Power.~~

Table 3-3. Pinout for x4 Fixed External Connector (~~root and end point~~Upstream Port & Downstream Port)

Pin #	Description Root	Mating Sequence of cable to board		Pin #	Description
Row Offset — no pin this side			—2nd	B1	POWER 5-V #1
A1	POWER 3.3-Vact RX	2nd	1st	B2	GROUND
A2	GROUND	1st	2nd	B3	PETp0
A3	PERp0	2nd	2nd	B4	PETn0
A4	PERn0	2nd	1st	B5	GROUND
A5	GROUND	1st	2nd	B6	PETp1
A6	PERp1	2nd	2nd	B7	PETn1
A7	PERn1	2nd	1st	B8	GROUND
A8	GROUND	1st	2nd	B9	2-WIRE CLOCK
A9	UNASSIGNED	2nd	2nd	B10	2-WIRE DATA
A10	CWAKE#	2nd	1st	B11	GROUND
A11	GROUND	1st	2nd	B12	PERST#
A12	VSP	2nd	2nd	B13	CPRSNT#
A13	VSP	2nd	1st	B14	GROUND
A14	GROUND	1st	2nd	B15	PETp2
A15	PERp2	2nd	2nd	B16	PETn2
A16	PERn2	2nd	1st	B17	GROUND
A17	GROUND	1st	2nd	B18	PETp3
A18	PERp3	2nd	2nd	B19	PETn3
A19	PERn3	2nd	1st	B20	GROUND
A20	GROUND	1st	2nd	B21	POWER 3.3-Vact TX
A21	POWER 5-V #2	2nd	Row Offset — no pin this side		

NOTICE NOTICE NOTICE NOTICE NOTICE

<u>Mating Level</u>	<u>Description</u>	<u>Pin #</u>		<u>Description</u>	<u>Mating Level</u>
	Row offset- no pin this side		<u>B1</u>	<u>POWER 5V #1 (see Note 1)</u>	<u>2nd</u>
<u>2nd</u>	<u>POWER 3.3 Vact #1 (see Note 2)</u>	<u>A1</u>	<u>B2</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A2</u>	<u>B3</u>	<u>PETp0</u>	<u>2nd</u>
<u>2nd</u>	<u>PERp0</u>	<u>A3</u>	<u>B4</u>	<u>PETn0</u>	<u>2nd</u>
<u>2nd</u>	<u>PERn0</u>	<u>A4</u>	<u>B5</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A5</u>	<u>B6</u>	<u>PETp1</u>	<u>2nd</u>
<u>2nd</u>	<u>PERp1</u>	<u>A6</u>	<u>B7</u>	<u>PETn1</u>	<u>2nd</u>
<u>2nd</u>	<u>PERn1</u>	<u>A7</u>	<u>B8</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A8</u>	<u>B9</u>	<u>2-WIRE CLOCK</u>	<u>2nd</u>
<u>2nd</u>	<u>UNASSIGNED</u>	<u>A9</u>	<u>B10</u>	<u>2-WIRE DATA</u>	<u>2nd</u>
<u>2nd</u>	<u>CWAKE# (see Note 3)</u>	<u>A10</u>	<u>B11</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A11</u>	<u>B12</u>	<u>PERST#</u>	<u>2nd</u>
<u>2nd</u>	<u>VSP (see Note 4)</u>	<u>A12</u>	<u>B13</u>	<u>CPRSNT#</u>	<u>2nd</u>
<u>2nd</u>	<u>VSP (see Note 4)</u>	<u>A13</u>	<u>B14</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A14</u>	<u>B15</u>	<u>PETp2</u>	<u>2nd</u>
<u>2nd</u>	<u>PERp2</u>	<u>A15</u>	<u>B16</u>	<u>PETn2</u>	<u>2nd</u>
<u>2nd</u>	<u>PERn2</u>	<u>A16</u>	<u>B17</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A17</u>	<u>B18</u>	<u>PETp3</u>	<u>2nd</u>
<u>2nd</u>	<u>PERp3</u>	<u>A18</u>	<u>B19</u>	<u>PETn3</u>	<u>2nd</u>
<u>2nd</u>	<u>PERn3</u>	<u>A19</u>	<u>B20</u>	<u>GROUND</u>	<u>1st</u>
<u>1st</u>	<u>GROUND</u>	<u>A20</u>	<u>B21</u>	<u>POWER 3.3 Vact #2 (see Note 2)</u>	<u>2nd</u>
<u>2nd</u>	<u>POWER 5V #2 (see Note 1)</u>	<u>A21</u>	Row offset- no pin this side		

Notes:

1. [Assigned for optional 5V power only; reassignment of this pin is not permitted. Pins must not be commoned; e.g., pins must be able to operate independently of each other.](#)
2. [Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.](#)
3. [This pin is permitted to support OBFF in addition to CWAKE#. Refer to the Card Electromechanical \(CEM\) specification for more information on OBFF.](#)
4. [These pins may be used to implement clocking architecture. For information on implementation, refer to Table 2-2.](#)

6.7 Free Cable Assembly Wiring Charts

~~All Internal ribbon cables are to be wired as complete crossovers.~~

~~Internal unassigned pins to be wired to enable crossover functionality~~

Internal and External cable assemblies are not interchangeable; [refer to sections 6.7.1 and 6.7.2 for details regarding Internal and External cables, respectively.](#)

~~External 5 V power does not crossover~~

6.7.1. Wiring Chart for x4 Internal Cables

- See ~~Internal Connector Pinout~~ Table 3-1 and Table 3-2 [for Internal cable pinouts](#).
- ~~The wiring charts for~~ Passive and Active cable assemblies are the same; [they are crossover cables](#).
- Active cables are defined as having active components only within the cable plug.
- The Fixed side must provide the 3.3 V to support optional active cable plugs (no wire passes down the cable).

Table 6-9. Wiring Chart for x4 Internal Passive and Active Crossover Cables

<u>P1 Row Position</u>	<u>Downstream Port</u>	<u>Cable Termination & Signal Direction</u>	<u>Upstream Port</u>	<u>P2 Row Position</u>
<u>A1 (Bevel)</u>	<u>POWER 3.3 Vact #1 (see Note 1)</u>	<u>NO WIRE</u>	<u>POWER 5V #1 (see Note 5)</u>	<u>B1</u>
<u>A2</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B2</u>
<u>A3</u>	<u>PERp0</u>	←————	<u>PETp0</u>	<u>B3</u>
<u>A4</u>	<u>PERn0</u>	←————	<u>PETn0</u>	<u>B4</u>
<u>A5</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B5</u>
<u>A6</u>	<u>PERp1</u>	←————	<u>PETp1</u>	<u>B6</u>
<u>A7</u>	<u>PERn1</u>	←————	<u>PETn1</u>	<u>B7</u>
<u>A8</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B8</u>
<u>A9</u>	<u>BP TYPE/ VSP (see Note 2)</u>	←-----	<u>BP TYPE/ VSP (see Note 2)</u>	<u>B9</u>
<u>A10</u>	<u>CWAKE# (see Note 3)</u>	←-----	<u>CWAKE# (see Note 3)</u>	<u>B10</u>
<u>A11</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B11</u>
<u>A12</u>	<u>VSP (see Note 4)</u>	—————	<u>VSP</u>	<u>B12</u>
<u>A13</u>	<u>VSP (see Note 4)</u>	—————	<u>VSP</u>	<u>B13</u>
<u>A14</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B14</u>
<u>A15</u>	<u>PERp2</u>	←————	<u>PETp2</u>	<u>B15</u>
<u>A16</u>	<u>PERn2</u>	←————	<u>PETn2</u>	<u>B16</u>
<u>A17</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B17</u>
<u>A18</u>	<u>PERp3</u>	←————	<u>PETp3</u>	<u>B18</u>
<u>A19</u>	<u>PERn3</u>	←————	<u>PETn3</u>	<u>B19</u>
<u>A20</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B20</u>
<u>A21</u>	<u>POWER 5V #2 (see Note 5)</u>	<u>NO WIRE</u>	<u>POWER 3.3 Vact #2 (see Note 1)</u>	<u>B21</u>

Table continued on next page.

NOTICE NOTICE NOTICE NOTICE NOTICE

	Row	ROOT/ Downstream	Cable Termination & Signal Direction	Row	END POINT/ Upstream
1	A1	POWER 3.3 Vact RX	NO-WIRE	B1	RESERVED
2	A2	GROUND	=====	B2	GROUND
3	A3	PERp0	←=====	B3	PETp0
4	A4	PERn0	←=====	B4	PETn0
5	A5	GROUND	=====	B5	GROUND
6	A6	PERp1	←=====	B6	PETp1
7	A7	PERn1	←=====	B7	PETn1
8	A8	GROUND	=====	B8	GROUND
9	A9	BP-TYPE	←=====	B9	BP-TYPE
10	A10	CWAKE# (Note 1)	←=====	B10	CWAKE#
11	A11	GROUND	=====	B11	GROUND
12	A12	VSP	=====	B12	VSP
13	A13	VSP	=====	B13	VSP
14	A14	GROUND	=====	B14	GROUND
15	A15	PERp2	←=====	B15	PETp2
16	A16	PERn2	←=====	B16	PETn2
17	A17	GROUND	=====	B17	GROUND
18	A18	PERp3	←=====	B18	PETp3
19	A19	PERn3	←=====	B19	PETn3
20	A20	GROUND	=====	B20	GROUND
21	A21	RESERVED	NO-WIRE	B21	POWER 3.3 Vact TX

Note:

CWAKE# is permitted to also be used for OBFF and if both ends support OBFF the signal becomes bidirectional.

Table 6-9. ~~(Cont'd)~~ Wiring Chart for x4 Internal Passive and Active Crossover Cables (continued from previous page).

P1 Row Position	Downstream Port	Cable Termination & Signal Direction	Upstream Port	P2 Row Position
B1	POWER 5V #1 (see Note 5)	NO WIRE	POWER 3.3 Vact #1 (see Note 1)	A1 (Bevel)
B2	GROUND	—————	GROUND	A2
B3	PETp0	—————→	PERp0	A3
B4	PETn0	—————→	PERn0	A4
B5	GROUND	—————	GROUND	A5
B6	PETp1	—————→	PERp1	A6
B7	PETn1	—————→	PERn1	A7
B8	GROUND	—————	GROUND	A8
B9	2-WIRE CLOCK	↔	2-WIRE CLOCK	A9
B10	2-WIRE DATA	↔	2-WIRE DATA	A10
B11	GROUND	—————	GROUND	A11
B12	PERST#	—————→	PERST#	A12
B13	CPRSNT#	←—————	CPRSNT#	A13
B14	GROUND	—————	GROUND	A14
B15	PETp2	—————→	PERp2	A15
B16	PETn2	—————→	PERn2	A16
B17	GROUND	—————	GROUND	A17
B18	PETp3	—————→	PERp3	A18
B19	PETn3	—————→	PERn3	A19
B20	GROUND	—————	GROUND	A20
B21	POWER 3.3 Vact #2 (see Note 1)	NO WIRE	POWER 5V #2 (see Note 5)	A21

Notes:

1. Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.
2. If this pin is used for BP Type, the signal direction is from Upstream Port to Downstream Port. If this pin is used for VSP, the signal direction is defined by the vendor.
3. If this pin is used for CWAKE#, the signal direction is from Upstream Port to Downstream Port. If this pin is used for OBFF and both ends support OBFF, the signal becomes bidirectional. Refer to the Card Electromechanical (CEM) specification for more information on OBFF.
4. These wires must be built to support the transmission of low speed, differential signals. They may be used to implement clocking architecture; for information on implementation, refer to Table 2-2.
5. Option for 5 V power not permitted for internal cables; this pin must not be reassigned.

	Rew	ROOT/ Downstream	Cable Termination & Signal Direction	Rew	END-POINT/ Upstream
1	B1	RESERVED	NO WIRE	A1	POWER 3.3 Vact RX
2	B2	GROUND	—————	A2	GROUND
3	B3	PETp0	—————>	A3	PERp0
4	B4	PETn0	—————>	A4	PERn0
5	B5	GROUND	—————	A5	GROUND
6	B6	PETp1	—————>	A6	PERp1
7	B7	PETn1	—————>	A7	PERn1
8	B8	GROUND	—————	A8	GROUND
9	B9	2-WIRE-CLOCK	<—————>	A9	2-WIRE-CLOCK
10	B10	2-WIRE-DATA	<—————>	A10	2-WIRE-DATA
11	B11	GROUND	—————	A11	GROUND
12	B12	PERST#	—————>	A12	PERST#
13	B13	CPRSNT#	<—————	A13	CPRSNT#
14	B14	GROUND	—————	A14	GROUND
15	B15	PETp2	—————>	A15	PERp2
16	B16	PETn2	—————>	A16	PERn2
17	B17	GROUND	—————	A17	GROUND
18	B18	PETp3	—————>	A18	PERp3
19	B19	PETn3	—————>	A19	PERn3
20	B20	GROUND	—————	A20	GROUND
21	B21	POWER 3.3 Vact TX	NO WIRE	A21	RESERVED

6.7.2. Wiring Chart for [x4](#) External Cables

□ See External Connector Pinout Table 3-3.

NOTICE NOTICE NOTICE NOTICE NOTICE

- This is not a full crossover cable; only the high speed lines crossover.
- The wiring charts for Passive and Active cable assemblies are the same.
- Active cables are defined as having active components only within the cable plug.
- The Fixed side must provide the 3.3 V to support ~~an~~ optional active cable [plugs \(no wire passes down the cable\)](#).
- The Fixed side must provide the 5 V for Optional Power [cables](#).

Table 6-10. Wiring Chart for x4 External Passive and Active Cables; with and without Power

	Row	ROOT/ Downstream	Cable Termination & Signal Direction	Row	END POINT/ Upstream
1	A1	POWER 3.3 Vact-RX	NO WIRE	A1	POWER 3.3 Vact-RX
2	A2	GROUND	—————	B2	GROUND
3	A3	PERp0	←—————	B3	PETp0
4	A4	PERn0	←—————	B4	PETn0
5	A5	GROUND	—————	B5	GROUND
6	A6	PERp1	←—————	B6	PETp1
7	A7	PERn1	←—————	B7	PETn1
8	A8	GROUND	—————	B8	GROUND
9	A9	UNASSIGNED	—————	A9	UNASSIGNED
10	A10	CWAKE# (Note 1)	←—————	A10	CWAKE#
11	A11	GROUND	—————	B11	GROUND
12	A12	VSP	—————	A12	VSP
13	A13	VSP	—————	A13	VSP
14	A14	GROUND	—————	B14	GROUND
15	A15	PERp2	←—————	B15	PETp2
16	A16	PERn2	←—————	B16	PETn2
17	A17	GROUND	—————	B17	GROUND
18	A18	PERp3	←—————	B18	PETp3
19	A19	PERn3	←—————	B19	PETn3
20	A20	GROUND	—————	B20	GROUND
21	A21	POWER 5-V #2	AS REQUIRED	A21	POWER 5-V #2

Note:

1. — CWAKE# is permitted to also be used for OBFF and if both ends support OBFF the signal becomes bidirectional.

NOTICE NOTICE NOTICE NOTICE NOTICE

<u>P1 Row Position</u>	<u>Downstream Port</u>	<u>Cable Termination & Signal Direction</u>	<u>Upstream Port</u>	<u>P2 Row Position</u>
<u>A1 (Bevel)</u>	<u>POWER 3.3 Vact #1 (see Note 1)</u>	<u>NO WIRE</u>	<u>POWER 3.3 Vact #1 (see Note 1)</u>	<u>A1 (Bevel)</u>
<u>A2</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B2</u>
<u>A3</u>	<u>PERp0</u>	←————	<u>PETp0</u>	<u>B3</u>
<u>A4</u>	<u>PERn0</u>	←————	<u>PETn0</u>	<u>B4</u>
<u>A5</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B5</u>
<u>A6</u>	<u>PERp1</u>	←————	<u>PETp1</u>	<u>B6</u>
<u>A7</u>	<u>PERn1</u>	←————	<u>PETn1</u>	<u>B7</u>
<u>A8</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B8</u>
<u>A9</u>	<u>UNASSIGNED</u>	—————	<u>UNASSIGNED</u>	<u>A9</u>
<u>A10</u>	<u>CWAKE# (see Note 2)</u>	←-----	<u>CWAKE# (see Note 2)</u>	<u>A10</u>
<u>A11</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B11</u>
<u>A12</u>	<u>VSP (see Note 4)</u>	—————	<u>VSP (see Note 4)</u>	<u>A12</u>
<u>A13</u>	<u>VSP (see Note 4)</u>	—————	<u>VSP (see Note 4)</u>	<u>A13</u>
<u>A14</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B14</u>
<u>A15</u>	<u>PERp2</u>	←————	<u>PETp2</u>	<u>B15</u>
<u>A16</u>	<u>PERn2</u>	←————	<u>PETn2</u>	<u>B16</u>
<u>A17</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B17</u>
<u>A18</u>	<u>PERp3</u>	←————	<u>PETp3</u>	<u>B18</u>
<u>A19</u>	<u>PERn3</u>	←————	<u>PETn3</u>	<u>B19</u>
<u>A20</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>B20</u>
<u>A21</u>	<u>POWER 5V #2 (see Note 3)</u>	<u>AS NEEDED</u>	<u>POWER 5V #2 (see Note 3)</u>	<u>A21</u>

Table continued on next page.

Table 6-10. ~~(Cont'd)~~ Wiring Chart for x4 External Passive and Active Crossover Cables, with and without Power [\(continued from previous page\)](#)

	Row	ROOT/ Downstream	Cable Termination & Signal Direction	Row	END POINT/ Upstream
1	B1	POWER 5-V #1	AS REQUIRED	B1	POWER 5-V #1
2	B2	GROUND	=====	A2	GROUND
3	B3	PETp0	=====>	A3	PERp0
4	B4	PETn0	=====>	A4	PERn0
5	B5	GROUND	=====	A5	GROUND
6	B6	PETp1	=====>	A6	PERp1
7	B7	PETn1	=====>	A7	PERn1
8	B8	GROUND	=====	A8	GROUND
9	B9	2-WIRE CLOCK	AS REQUIRED	B9	2-WIRE CLOCK
10	B10	2-WIRE DATA	AS REQUIRED	B10	2-WIRE DATA
11	B11	GROUND	=====	A11	GROUND
12	B12	PERST#	=====>	B12	PERST#
13	B13	CPRSNT#	=====<	B13	CPRSNT#
14	B14	GROUND	=====	A14	GROUND
15	B15	PETp2	=====>	A15	PERp2
16	B16	PETn2	=====>	A16	PERn2
17	B17	GROUND	=====	A17	GROUND
18	B18	PETp3	=====>	A18	PERp3
19	B19	PETn3	=====>	A19	PERn3
20	B20	GROUND	=====	A20	GROUND
21	B21	POWER 3.3-Vact-TX	NO WIRE	B21	POWER 3.3-Vact-TX

NOTICE NOTICE NOTICE NOTICE NOTICE

<u>P1 Row Position</u>	<u>Downstream Port</u>	<u>Cable Termination & Signal Direction</u>	<u>Upstream Port</u>	<u>P2 Row Position</u>
<u>B1</u>	<u>POWER 5V #1 (see Note 3)</u>	<u>AS NEEDED</u>	<u>POWER 5V #1 (see Note 3)</u>	<u>B1</u>
<u>B2</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>A2</u>
<u>B3</u>	<u>PETp0</u>	—————→	<u>PERp0</u>	<u>A3</u>
<u>B4</u>	<u>PETn0</u>	—————→	<u>PERn0</u>	<u>A4</u>
<u>B5</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>A5</u>
<u>B6</u>	<u>PETp1</u>	—————→	<u>PERp1</u>	<u>A6</u>
<u>B7</u>	<u>PETn1</u>	—————→	<u>PERn1</u>	<u>A7</u>
<u>B8</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>A8</u>
<u>B9</u>	<u>2-WIRE CLOCK</u>	<u>AS NEEDED</u>	<u>2-WIRE CLOCK</u>	<u>B9</u>
<u>B10</u>	<u>2-WIRE DATA</u>	<u>AS NEEDED</u>	<u>2-WIRE DATA</u>	<u>B10</u>
<u>B11</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>A11</u>
<u>B12</u>	<u>PERST#</u>	—————→	<u>PERST#</u>	<u>B12</u>
<u>B13</u>	<u>CPRSNT#</u>	←—————	<u>CPRSNT#</u>	<u>B13</u>
<u>B14</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>A14</u>
<u>B15</u>	<u>PETp2</u>	—————→	<u>PERp2</u>	<u>A15</u>
<u>B16</u>	<u>PETn2</u>	—————→	<u>PERn2</u>	<u>A16</u>
<u>B17</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>A17</u>
<u>B18</u>	<u>PETp3</u>	—————→	<u>PERp3</u>	<u>A18</u>
<u>B19</u>	<u>PETn3</u>	—————→	<u>PERn3</u>	<u>A19</u>
<u>B20</u>	<u>GROUND</u>	—————	<u>GROUND</u>	<u>A20</u>
<u>B21</u>	<u>POWER 3.3 Vact #2 (see Note 1)</u>	<u>NO WIRE</u>	<u>POWER 3.3 Vact #2 (see Note 1)</u>	<u>B21</u>

Notes:

1. [Assigned for use with optional active cables only. Pins must not be commoned; e.g., pins must be able to operate independently of each other.](#)
2. [If this pin is used for CWAKE#, the signal direction is from Upstream Port to Downstream Port. If this pin is used for OBFF and both ends support OBFF, the signal becomes bidirectional. Refer to the Card Electromechanical \(CEM\) specification for more information on OBFF.](#)
3. [Assigned for use with optional 5V power only; reassignment of this pin is not permitted. Pins must not be commoned; e.g., pins must be able to operate independently of each other.](#)
4. [These wires must be built to support the transmission of low speed, differential signals. They may be used to implement clocking architecture; for information on implementation, refer to Table 2-2.](#)