PCI-SIG Releases PCIe® 4.0, Version 1.0
By Al Yanes

I'm pleased to share that PCI-SIG has released the PCIe 4.0 Specification Version 1.0 and it is now available for download on our website. We had previously announced in June this year at our annual DevCon event that the Version 0.9 specification was feature complete and undergoing member IP review. The final published spec describes the PCI Express® architecture, interconnect attributes, fabric management, and the programming interface required to design and build systems and peripherals that are compliant.

The delivery of the PCIe 4.0 specification to the industry is an important addition to our spec library as it delivers high performance 16GT/s data rates with flexible lane width configurations, while continuing to meet the industry's requirements for low power. Additional functional enhancements include:

- Extended tags and credits for service devices
- Reduced system latency
- Lane margining
- Superior RAS capabilities
- Scalability for added lanes and bandwidth
- Improved I/O virtualization and platform integration

And we've seen unprecedented early adoption! Prior to publication, we've had numerous vendors confirmed with 16GT/s PHYs in silicon and IP vendors already offering 16GT/s controller. Given the interest, we held a pre-publication Compliance Workshop with preliminary FYI Testing Only for PCIe 4.0 architecture that attracted dozens of solutions. We're continuing to conduct FYI testing in our workshops throughout the remainder of the year.

PCI-SIG members are welcome to access the PCIe 4.0 spec online at no cost through the PCI-SIG Specification Library. Non-members may purchase the specification here.

PCIe 4.0 is a significant milestone, but we're not resting. We've already released the Version 0.3 of the forthcoming PCIe 5.0 specification, targeted for Q2 2019, which will increase speeds to 32GT/s. For more information on PCI-SIG or PCIe technology, visit our website at www.pcisig.com.