Celebrating 20 Years of the PCIe® Specification

PCI-SIG® Webinar Series

April 2024

Panelists

Mihaela Erler (Moderator)

Industry Enabling Manager, Intel
PCI-SIG® Marketing Work Group Co-Chair

Debendra Das Sharma

Senior Fellow and Co-GM of Memory and I/O Technologies in Data Platforms and Artificial Intelligence Group, Intel
PCI-SIG Board of Directors member

David Harriman

Distinguished Architect, Ampere Computing
PCI-SIG Protocol Work Group Chair and Automotive Work Group Co-Chair

Manisha Nilange

I/O Architect and Analog Engineering Manager, Intel
PCI-SIG ElectroMechanical, Mini and SFF Connector Work Group Chair, Compliance Co-Chair

Richard Solomon

Technical Marketing Manager, PCIe® Controller IP, Synopsys
PCI-SIG Vice President and Compliance Co-Chair

PCI-SIG®: An Open Industry Consortium

- PCI-SIG: Organization that defines the PCI Express® (PCIe®) specifications and related form factors
- Established in 1992 – 32 years and growing stronger – THANK YOU!!
- **975+** member companies worldwide
- Creating specifications and mechanisms to **support compliance** and **interoperability**

Board of Directors
2023 – 2024

AMD, arm, DELL Technologies, IBM, intel, KEYSIGHT TECHNOLOGIES, NVIDIA, Qualcomm, SYNOPSYS® Silicon to Software™

Evolution of PCI Express® Specification: Speeds and Feeds

- Doubles data rate with full backward compatibility every three years **over seven generations**
  - A x16 PCIe® 5.0 device interoperates with a x1 PCIe 1.0 device!
  - Encoding changes when essential
- Ubiquitous I/O across the compute continuum
  - PC, Hand-held, Workstation, Server, Cloud, Enterprise, HPC, Embedded, IoT, Automotive and AI
- One stack / same silicon across all segments; supporting
  - Different form-factors, widths (x1/ x2/ x4/ x8/ x16) and data rates

PCIe® Specification	Data Rate(Gb/s) (Encoding)	x16 B/W per direction**	Year
1.0	2.5 (8b/10b)	32 Gb/s	2003
2.0	5.0 (8b/10b)	64 Gb/s	2007
3.0	8.0 (128b/130b)	126 Gb/s	2010
4.0	16.0 (128b/130b)	252 Gb/s	2017
5.0	32.0 (128b/130b)	504 Gb/s	2019
6.0	64.0 (PAM4, Flit)	1024 Gb/s	2022
7.0	128.0 (PAM4, Flit)	2048 Gb/s	2025*

* - Projected ** - bandwidth after encoding overhead

The PCIe specification – Seven generations spanning two decades!

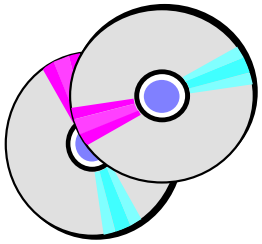
Q&A

Thank you for attending a PCI-SIG® 2024 Webinar

For more information, please visit www.pcisig.com

Backup Slides

PCI-SIG®: From Spec to Compliance



PCI-SIG Specs
Describes
Requirements

Base specification and Form Factor specs

C&I (Compliance and Interop) Test Specs
Describes
Test criteria based on spec requirements
- Test Definitions
- Pass/Fail Criteria

Test Tools, Fixtures And Procedures

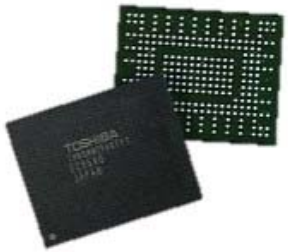
Test H/W & S/W
Validates
Test criteria
- Compliance
- Interoperability

Clear Test Output
Maps
- Directly to Test Spec

Predictable path to design compliance

PCIe® Architecture: One Base Specification, Multiple Form Factors

BGA



16x20 mm
small and thin
platforms

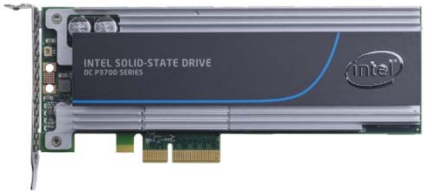
M.2

42, 80, and 110mm
Smallest footprint of
PCIe connector form
factors, use for boot or
for max storage density

U.2 2.5in (aka SFF-8639)

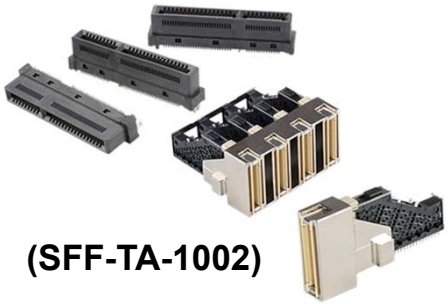
Majority of SSDs sold
Ease of deployment,
hotplug, serviceability
Single-Port x4 or Dual-Port x2

CEM Add-in-Card



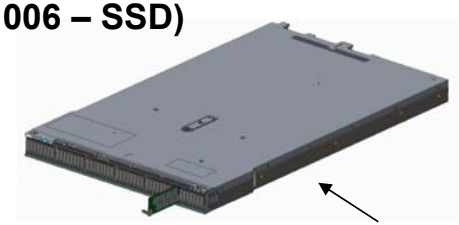
Add-in-card (AIC) has maximum
system compatibility with existing
servers and most reliable compliance
program. Higher power envelope,
and options for height and length

High B/W with
PCIe 3.0
Prevalent in
hand-held, IoT,
automotive

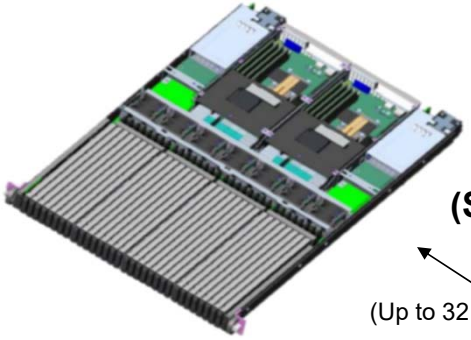


(SFF-TA-1002)

(SFF-TA-1006 – SSD)



(Up to 36 Modules)



(SFF-TA-1007 – SSD)

(Up to 32 Modules)

Source: Intel Corporation

Multiple form-factors from the same silicon to meet the needs of different segments

Protocol Evolution to Meet New Usage Models

- I/O Virtualization
- Data Movement Efficiency across the system
  - Transaction Processing Hints, Atomics, Translated vs Untranslated address
- Scalability as system sizes increases:
  - Unordered I/O: support fabrics with multi-path while maintaining producer-consumer model
  - Increased number of outstanding transactions, etc.
- Reliability, Availability, and Serviceability
  - Hierarchical Timeout, Advanced Error Reporting, (enhanced) Downstream Port Containment, etc.
- Power Management Enhancements
  - Dynamic Power Allocation, L1 Sub-state, L0p, etc.
- Security Enhancements
  - Authentication, Encryption, etc.
- And many more …

Protocol enhancements to meet the (r)evolution in compute landscape over the last two decades