



PCIe® Technology for Long and Short Reach in Automotive Applications

PCI-SIG® Educational Automotive Webinar Series

Presented by

Anwar Sadat (Texas Instruments), Edo Cohen (Valens) and Hope Bovenzi (Aster Labs)

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Speakers

Hope Bovenzi

Head of Marketing, Astera Labs



Hope Bovenzi is the Head of Marketing at Astera Labs. She is responsible for the marketing team at Astera Labs

Prior to Astera Labs, she ran the Automotive Infotainment Systems team at Texas Instruments. She has extensive experience in defining disruptive systems for the future connected car and its infotainment systems. She has defined seamless user-experiences within the digital cockpit and analyzed market trajectory to develop go-to-market strategy for revenue growth in emerging automotive technologies.

Anwar Sadat

Product definer, Texas Instruments



Anwar Sadat is a product definer at TI's high speed signal conditioning team. He is with TI for 15 years and held various individual and management positions developing high speed products for PCIe, USB and Video interfaces. Prior to TI he worked as an analog designer at Conexant Systems.

He earned his MS and PhD in electrical engineering from University of Central Florida.

He is on USB-IF board of directors.

Edo Cohen

Director Strategic Innovation, Valens Semiconductor



Edo is Valens' Director for Strategic Innovation, spearheading automotive standardization. Edo brings more than 25 years of experience as a senior system engineer, with extensive knowledge in system architecture, technical specifications, definition and execution.

Prior to Valens, Edo held Senior System Architect positions in Intel Corporation and at Marvell Cellular Division, and held engineering managerial positions at NAMS, Alvarion, and Floware. Edo holds an MBA and a B.Sc. in Electrical Engineering from Tel Aviv University.



Agenda

- Overview of Automotive PCIe® Technology Opportunities
- Automotive PCIe Technology Long Reach – Inter ECU connectivity over Cables
 - Protocol advantages
 - Inter ECU connectivity
 - Automotive connectivity challenges
- Automotive PCIe Technology Short Reach – Intra-ECU connectivity
- Signal conditioning
- Summary

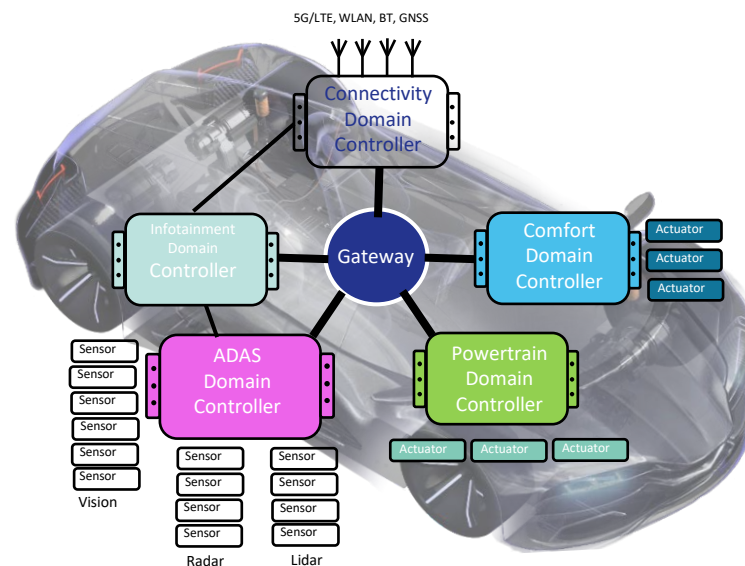
Overview

Market Dynamics: Zonal Architecture Reshaping Automotive Architecture



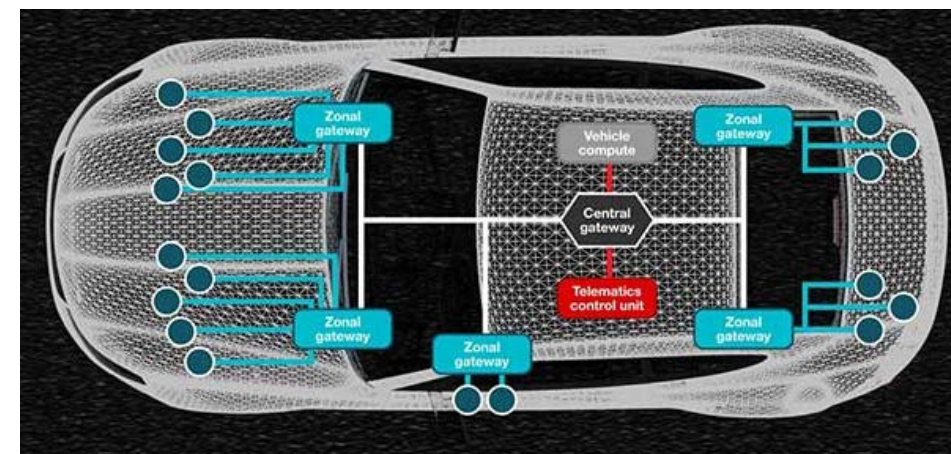
Yesterday
30- 100+ ECUs in a car

Mainstream MCUs



Today
Domain Logical Architecture

Consolidating of ECUs
Integration of Functions, AI & ICs



Tomorrow/Future
Zonal Physical Architecture

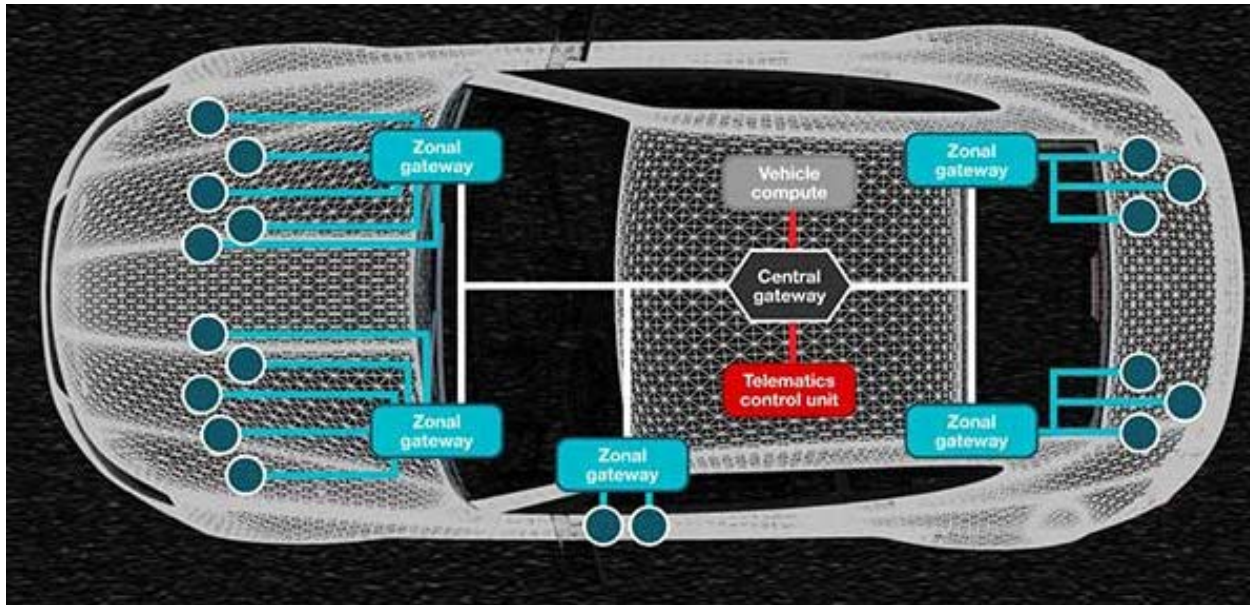
Multi-Applications Central Processing
Multi-Chip & Higher
Complexity/Performance

Source [//e2e.ti.com/blogs_/b/behind_the_wheel/posts/processing-the-advantages-of-zone-architecture-in-automotive](https://e2e.ti.com/blogs_/b/behind_the_wheel/posts/processing-the-advantages-of-zone-architecture-in-automotive)

Server-Class Connectivity for Automotive with PCIe® Infrastructure

High-bandwidth, low-latency, open, scalable, secure “data-pipe”

Vehicle Zonal Architecture



Source [//e2e.ti.com/blogs_/b/behind the wheel/posts/processing-the-advantages-of-zone-architecture-in-automotive](https://e2e.ti.com/blogs_/b/behind_the_wheel/posts/processing-the-advantages-of-zone-architecture-in-automotive)

- The amount of Data and Information is **growing exponentially (10s of Gbps)** while latency requirements become more stringent (**10s of ns**)
- Existing domain vehicle architectures **can't meet performance requirements, too complex to maintain and inefficient** - driving a need for **new architectural approaches**.
- Advancements in Processing capabilities and High-Speed Vehicle Networking drive transition to more effective **Central Computing** and low latency **Zonal Vehicle Architectures**

PCIe® Technology Over Long Reach Cable

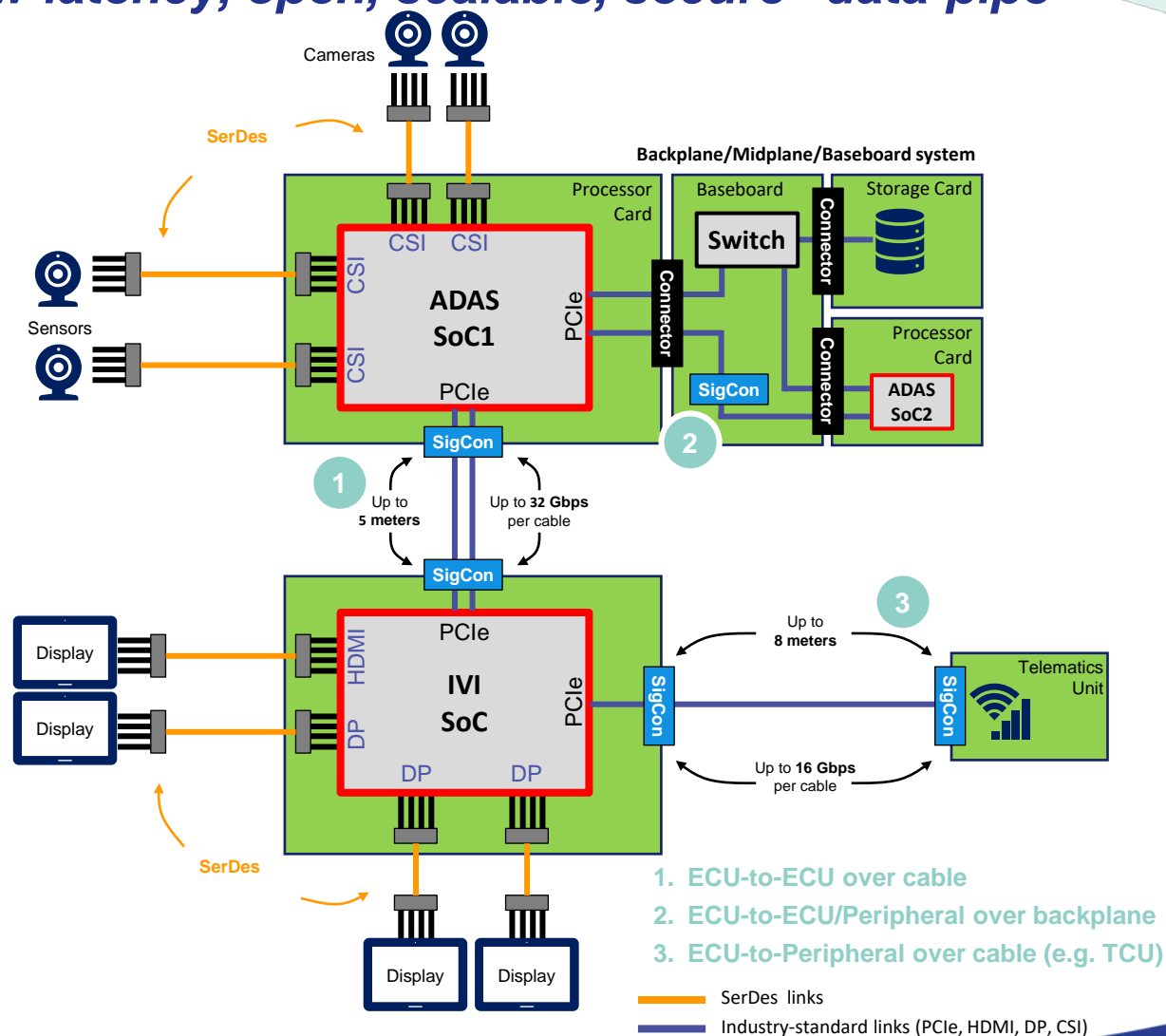
- PCIe technology-based connectivity in automotive inter-ECU networks
- Protocol advantages of PCIe technology
- Long Channel Challenges

Server-Class Connectivity for Automotive

PCIe® technology offers high-bandwidth, low-latency, open, scalable, secure “data-pipe”

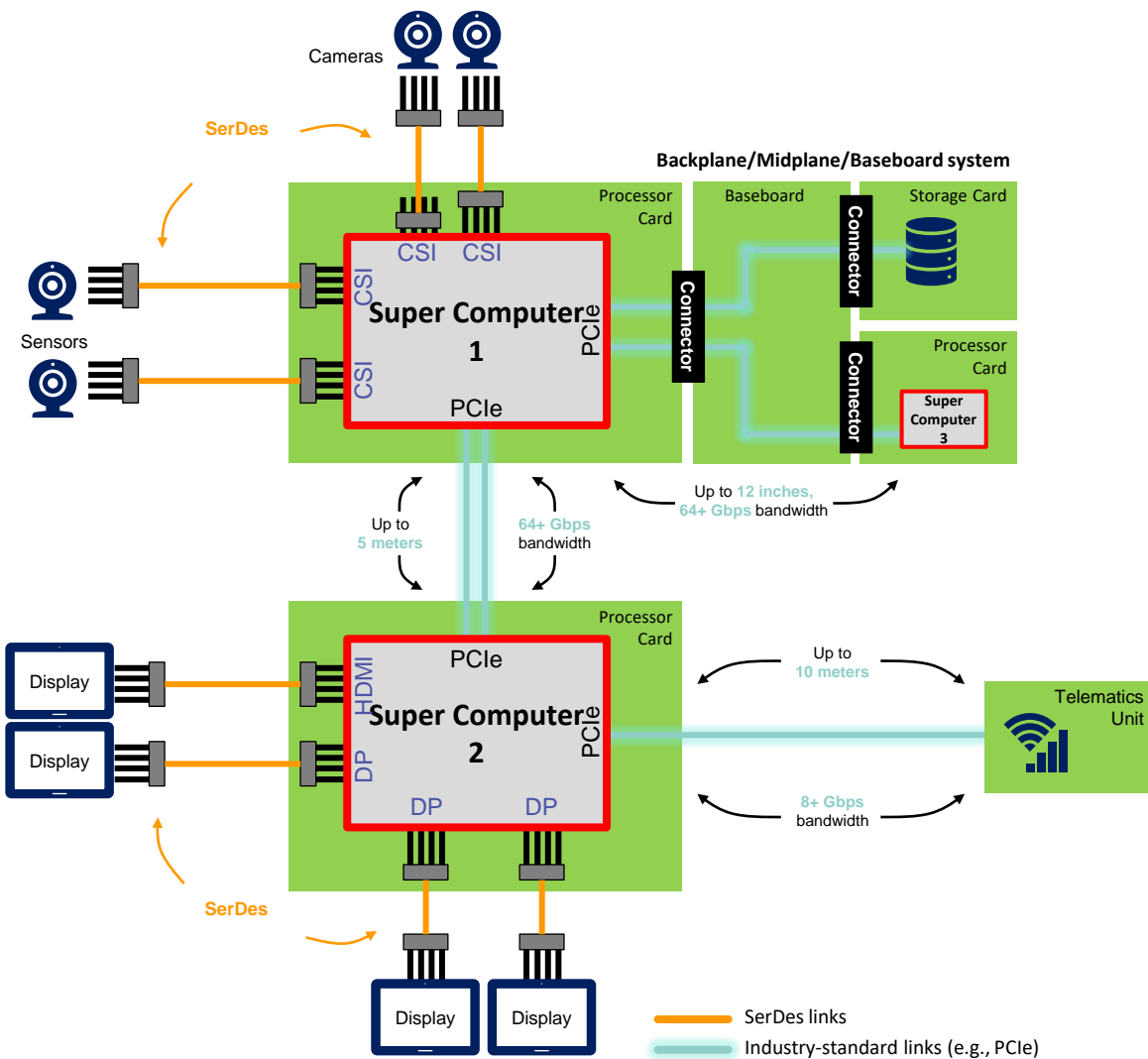
Why PCIe infrastructure as connectivity backbone for automotive?

- “Natural” I/O bus – Already available on most SoCs, Controllers
- Open standard with a huge ecosystem, multiple vendors
- Extremely low latency – 100s of ns
- Reliable transport protocol + New security extensions
- Scalable Bandwidth – 8/16/32 Gbps per lane, Up to 16 lanes
- Support multiple topologies – Chip-to-Chip, Backplane, Cables
- Point-to-Point or Switched architecture
- Expanding from I/O interface to System interface (example NVMe SSDs) – No protocol/bus converters required
- New PCIe-based [Compute Express Link](#) unifies interconnect for I/O, Cache, and Memory. Important for multi-CPU systems



Enable Robust, Low-Latency High-Bandwidth Connectivity

PCIe® technology signal conditioning supports 64+ Gbps bandwidth, 10m+ cable reach

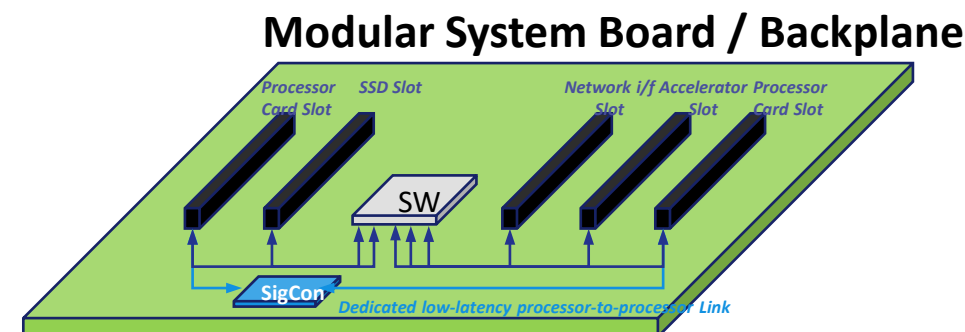
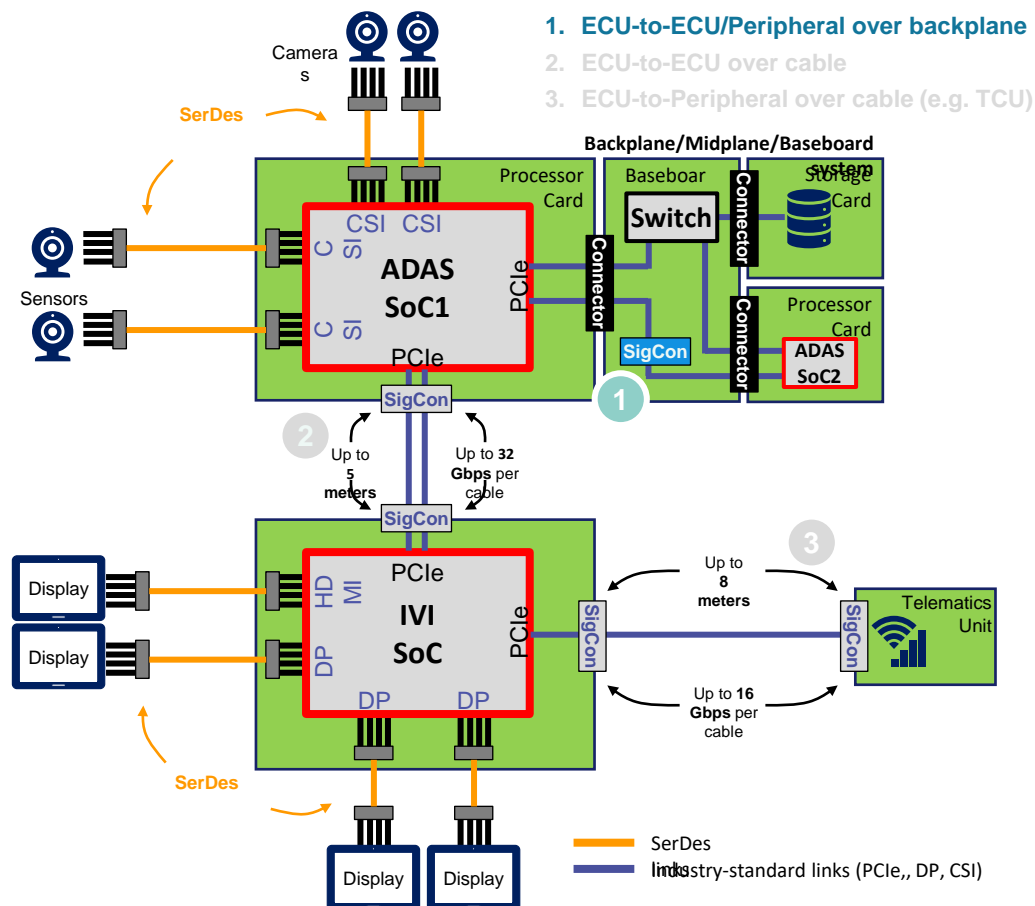


High-Bandwidth Links Stress Link Budget in Complex, Multi-Connector Topologies

| Application | ECU → Switch/ Storage over PCB | ECU → ECU over Cable | ECU → Peripheral over Cable |
|-----------------------|--|---|--|
| Physical topology | ECU → ~4 inches PCB → Connector → 6 (to 10) inches PCB → Connector → ~4 inches PCB → ECU | ECU → ~4 inches PCB → Connector → 3 (to 10) meter cable → Connector → ~4 inches PCB → ECU | ECU → ~4 inches PCB → Connector → 10 meter cable → Connector → ~4 inches PCB → ECU |
| Bandwidth per Lane | 16 Gbps (PCIe 4.0) 32 Gbps (PCIe 5.0) | 16 Gbps (PCIe 4.0) 32 Gbps (PCIe 5.0) | 8 Gbps (PCIe 3.0) 16 Gbps (PCIe 4.0) |
| Physical channel loss | 5 + 4 + 1 + 6 (to 10) + 1 + 4 + 5 = 26 (to 30) dB | 5 + 4 + 1 + 9 (to 30) + 1 + 4 + 5 = 29 (to 50) dB | 3.5 + 2.5 + 1 + 15 + 1 + 2.5 + 3.5 = ~29 dB |
| Loss budget | 28 dB | 28 dB | 22 dB |

Use Case 1: ECU-to-ECU/Peripheral Over Backplane

Enable modular designs with standard PCIe® interface

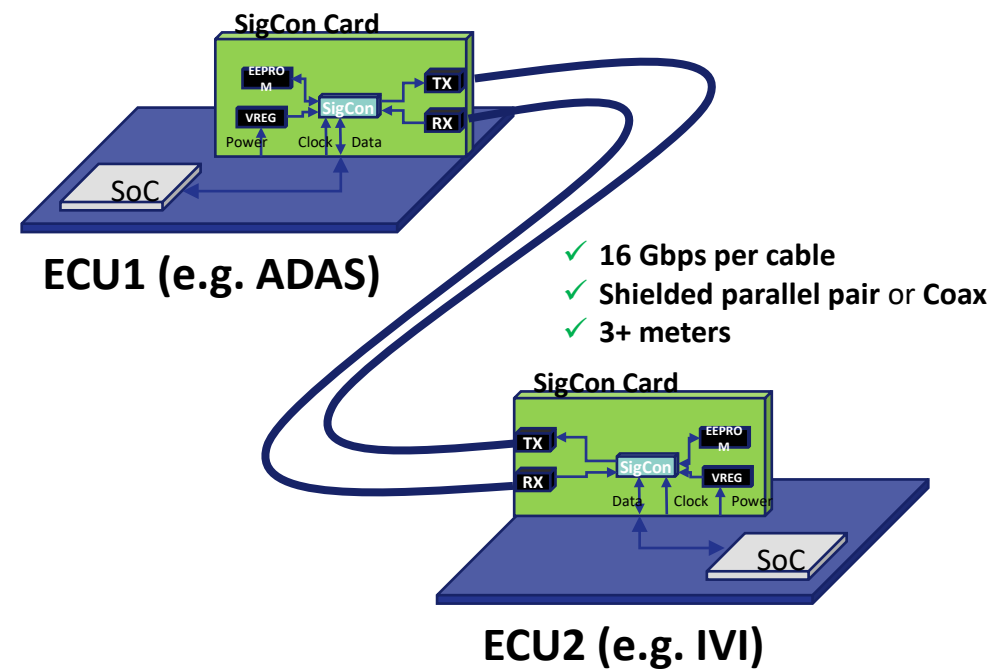
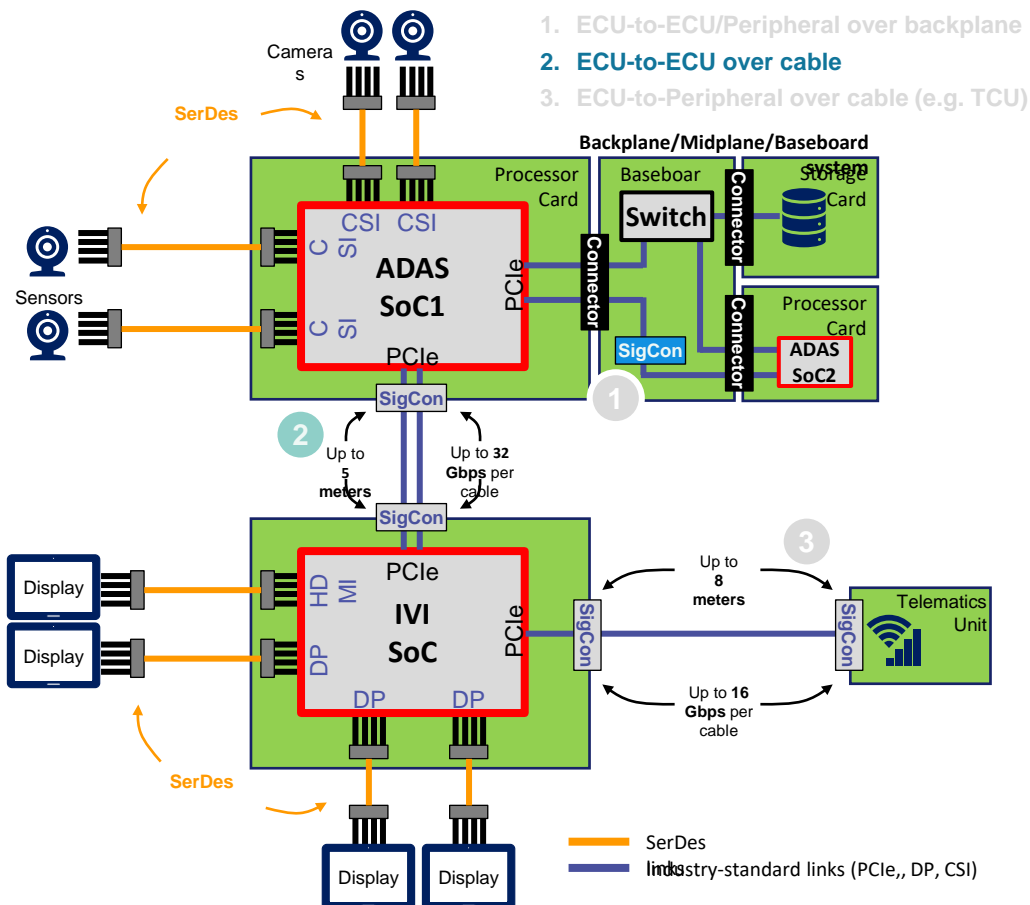


PCIe Protocol + SigCon Solution Benefits

- ▶ Low-latency path
- ▶ Enables multi-connector topologies
- ▶ Scalable bandwidth
- ▶ Industry standard
- ▶ Large ecosystem of native-PCIe device

Use Case 2: ECU-to-ECU Over Cable

High-bandwidth, low-latency processor interconnect

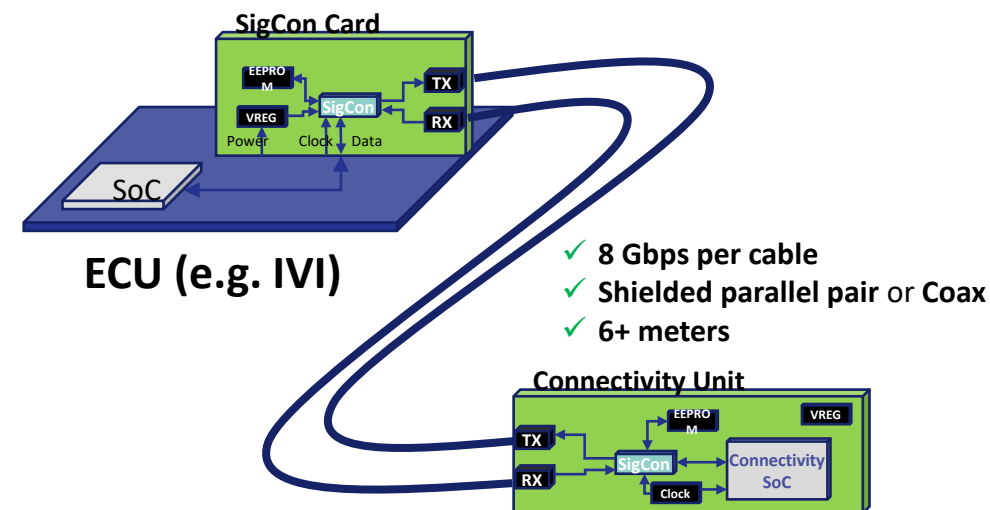
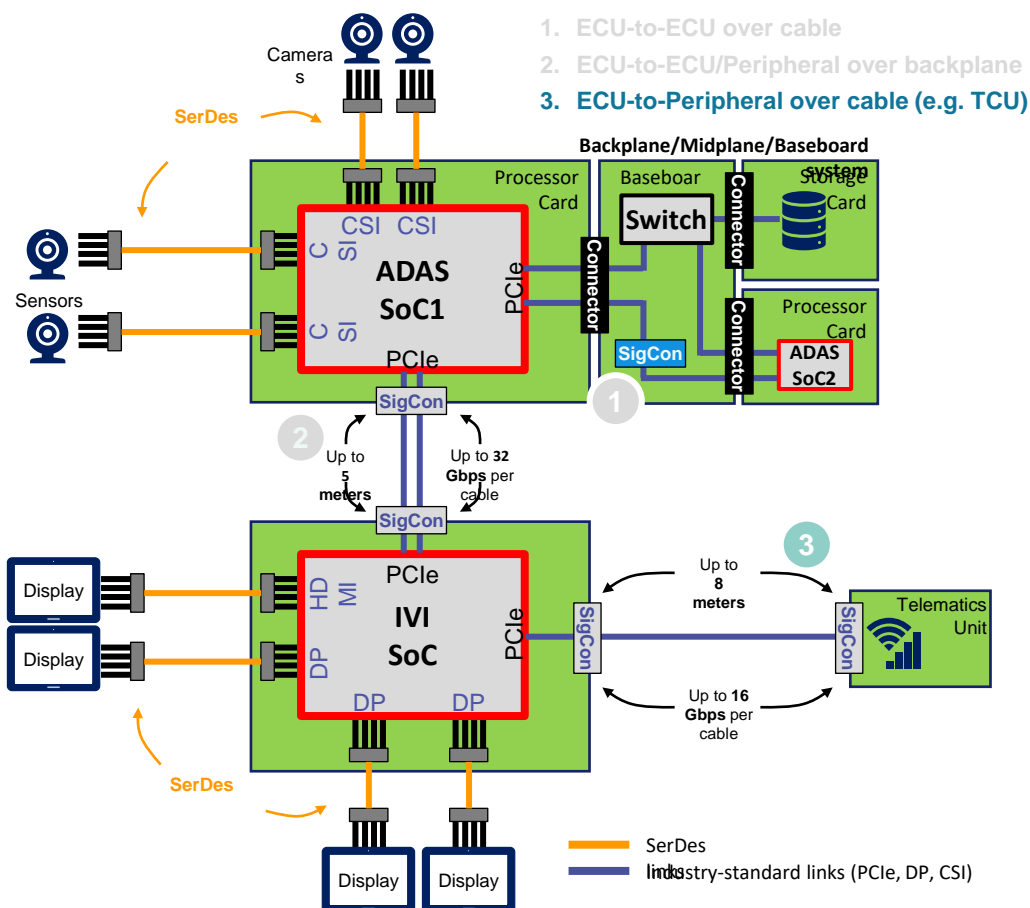


PCIe® Protocol + SigCon Solution Benefits

- ▶ Low-latency path
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- ▶ Scalable bandwidth
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Use Case 3: ECU-to-Peripheral Over Cable

Achieve high-speed & symmetric bandwidth with minimum cabling

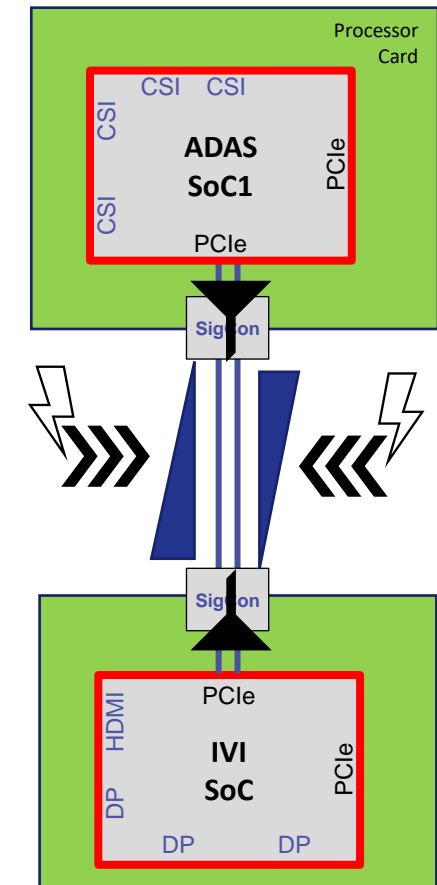


PCIe® Protocol + SigCon Solution Benefits

- ▶ Low-latency path
- ▶ Enables multi-connector topologies
- ▶ Scalable bandwidth
- ▶ Industry standard
- ▶ Large ecosystem of native-PCIe device

Automotive PCIe® Long Reach Challenges

- Automotive PCIe long reach Channel challenges have three main elements
 - Automotive harness/cables and connectors (including inline)
 - Higher channel loss
 - Inline connectors reflection
 - Shielding effectiveness degradation due to vehicle life span
 - Automotive noise environment
 - Dynamic external noise profile
 - Noise bursts
 - PCIe Sideband signals handling
 - Sideband signals can be either left unconnected or to be multiplexed



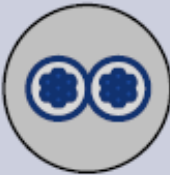



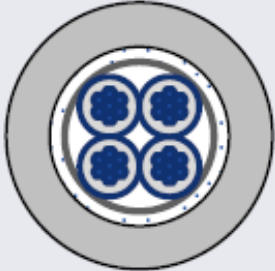

Automotive Wiring Harness

- Wiring harness is considered as the 2nd highest cost and 3rd heaviest component, after the engine and chassis.
- A complex wiring harness as in the picture here can reach up to 50% of a vehicle labor cost.



Source: <http://www.videantis.com/biggest-myth-in-automotive-ethernet-wont-work-for-adas.html>

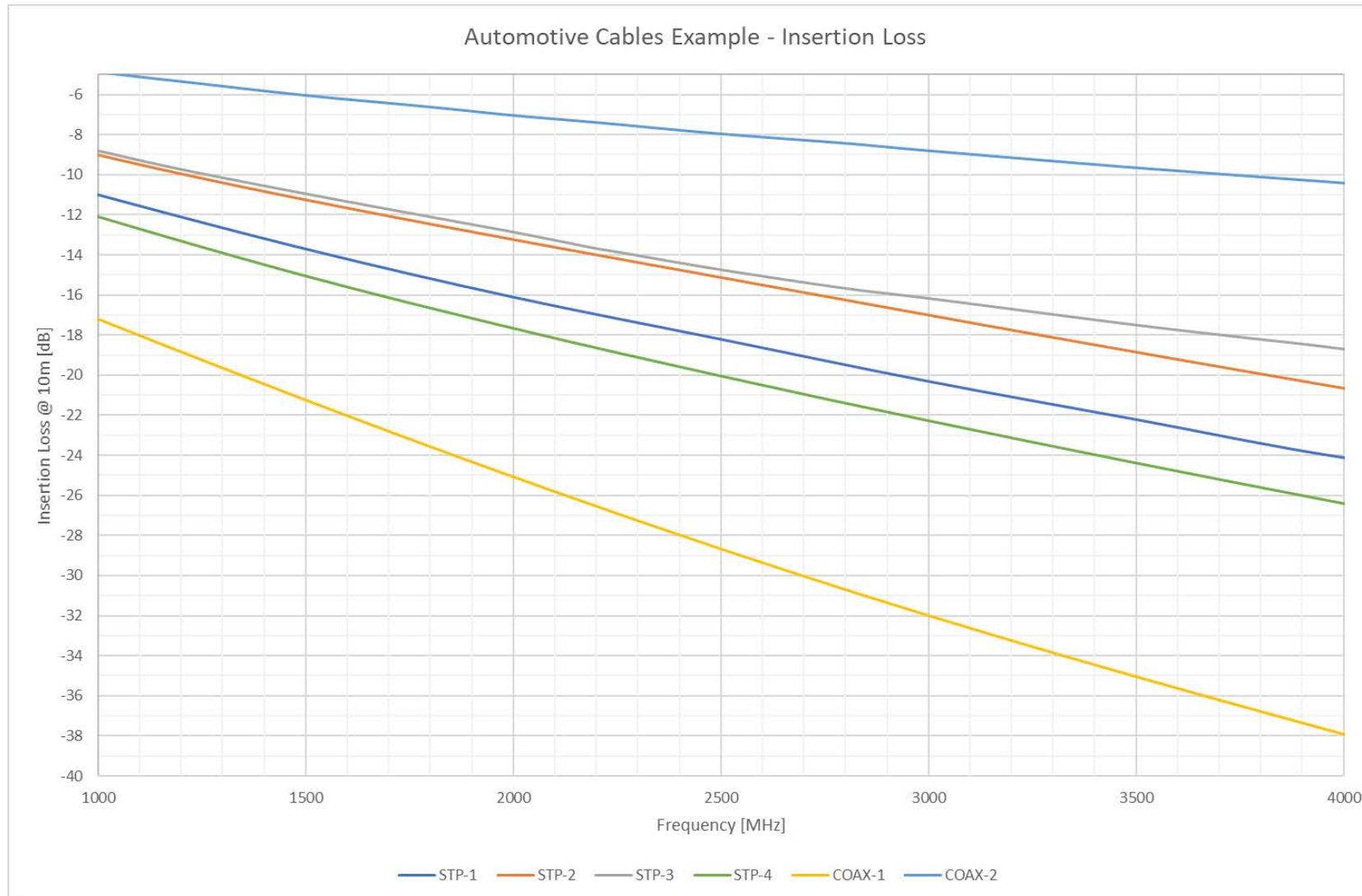
Automotive Cable types

| Lanes | UTP | STP STQ | SPP (Parallel Pair) | Coaxial |
|---|---|--|--|---|
| One |  |  |  |  |
| Two | |  |  | |
| Notes: Typically conductors are stranded Typically air filled for shielded cables | | | | |

Source: mueller_NGAuto_1a_0217

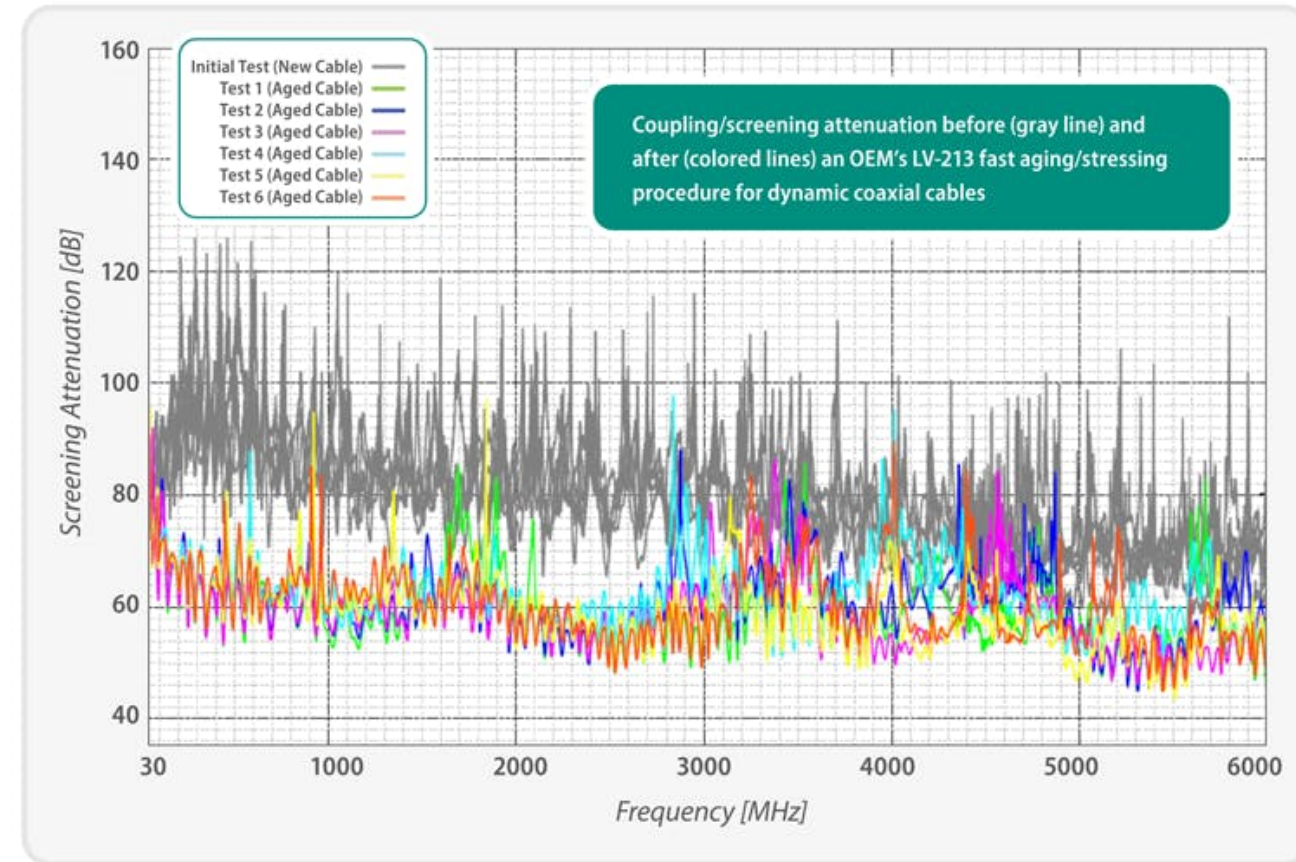


Cable IL examples



Shielding effectiveness over vehicle lifetime

- During the lifetime of a vehicle, the shielding effectiveness is degraded due to aging, temperature and stress.
- This degradation impact the amount of noise penetrating the transmitted signal and should be taken into account when designing a system.
- Screening attenuation before (gray) and after (colors), LV-213-1 fast aging/stressing procedure for dynamic coax cables (with only half of the cycle-count defined for the test)



Source: <https://www.mwrf.com/markets/automotive/article/21168119/mipi-alliance-mipi-aphy-a-resilient-asymmetric-data-transport-for-a-vehicles-lifespan>

Automotive Noise Environment

- The vehicle has a harsh and dynamically changing noise environment
- EMC requirements are driven from the UNECE Regulation 10, and these are the main tests that are mandated by all major OEM
 - Radiated Emission
 - Conducted Immunity
 - Transient Immunity
- The baseline of these tests is defined in relevant ISO specification, and it is common for OEM to define its own limits based on goals and experience
 - There is a large variety in the different OEM requirements

Automotive EMC Requirements – Examples

| Test Type | Base Specification | Common Levels | Comment |
|--------------------|--------------------|-------------------|---------|
| Radiated Immunity | ISO 11452-2 | 200 V/m – 400 V/m | |
| Conducted Immunity | ISO 11452-4 | 100 mA – 200mA | |
| Transient immunity | ISO 7637-3 | 150V or 220V | |

- **Radiated Immunity**

- Radiated electromagnetic immunity model based on the ALSE method (ISO 11452-2), using multiple modulation schemes (i.e., CW, AM, PM; see Figure below) testing instant attacks over the cable.

- **Conducted Emissions**

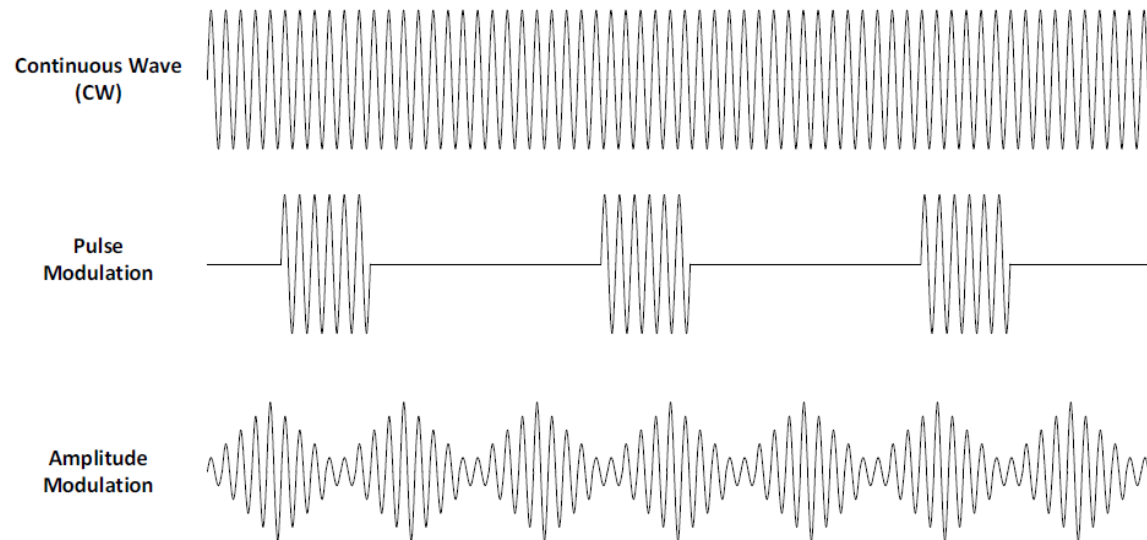
- Conducted electromagnetic immunity model based on ISO 11452-4 using multiple modulation schemes (i.e., CW and AM testing instant attacks over the cable.

- **Transient Immunity**

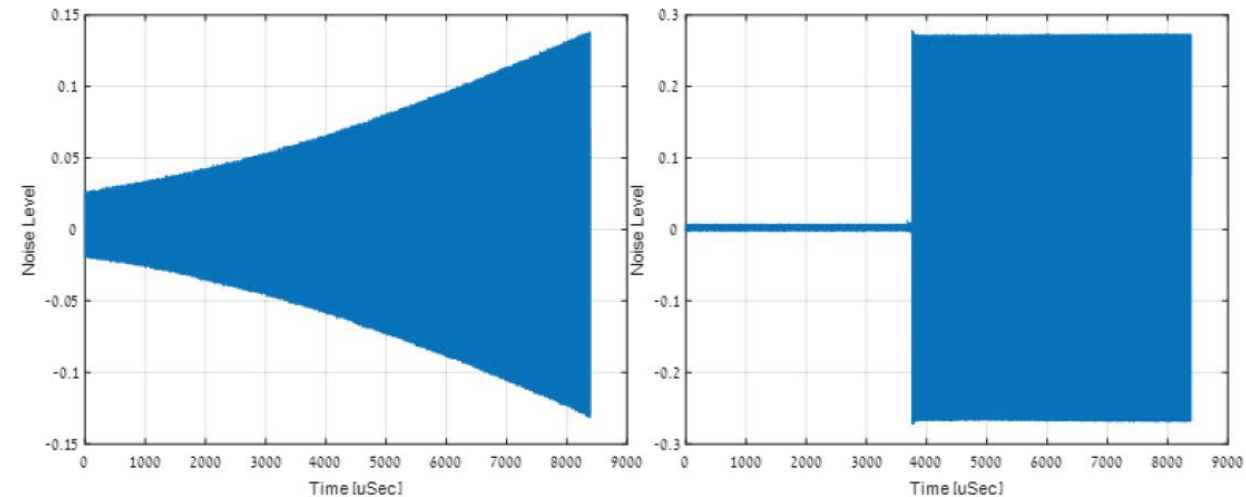
- Transient immunity to fast and slow pulses based on ISO7637-2/3

Modulation Schemes Used in RF Immunity

Modulation Examples



Actual testing lab pulse example



Low-speed side-band signals

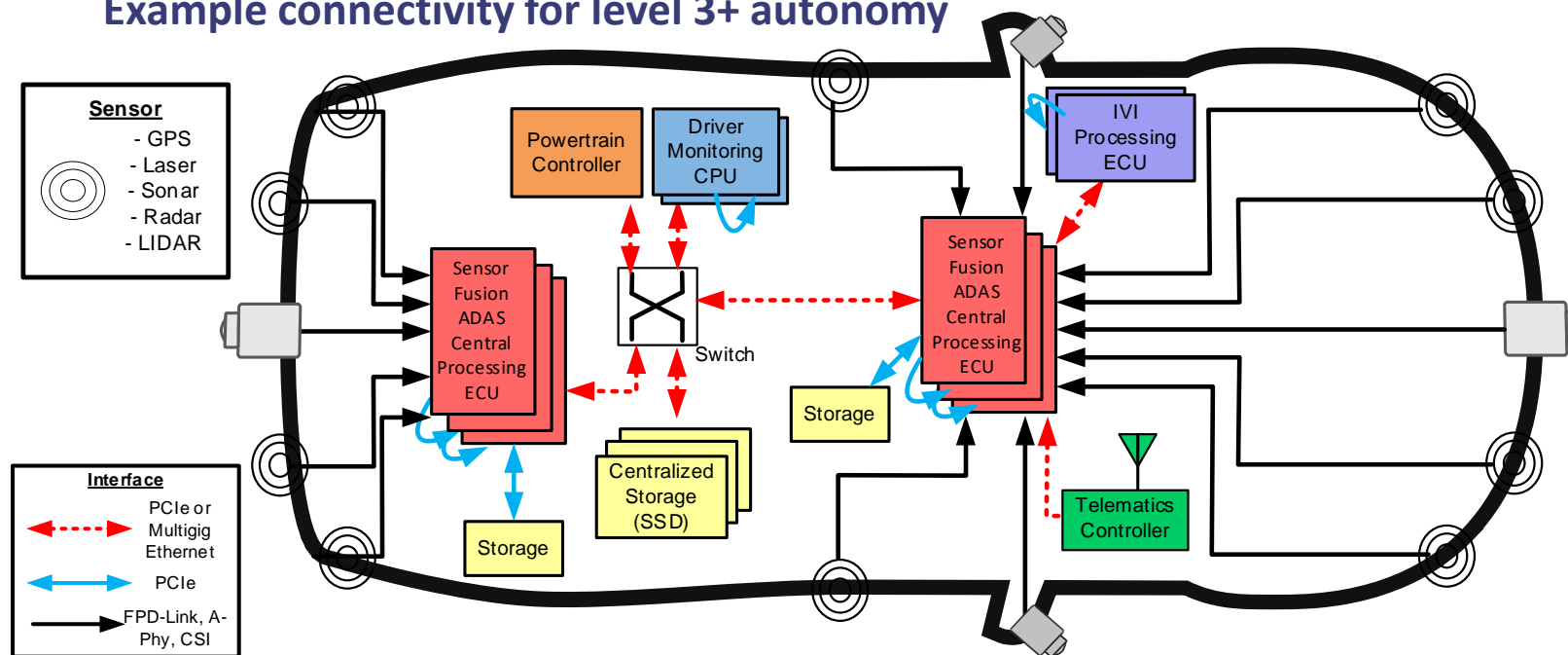
- Automotive cables (as shown above) require signals multiplexing in order to reduce cable count and its implications (e.g. weight, maintenance complexity)
- Essential high-speed in-band PCIe[®] signals must be connected over automotive cable
- Low speed side-band signals should be either left unconnected or use packetization methods over the automotive cable
- PCIe reference clock may not be shared to avoid possible EMI implications

Automotive PCIe[®] Technology – Short Reach

- Automotive wired connectivity
- Intra-ECU connectivity
- Storage connectivity
- Scalable compute power

Automotive Wired Connectivity – Short Reach

Example connectivity for level 3+ autonomy

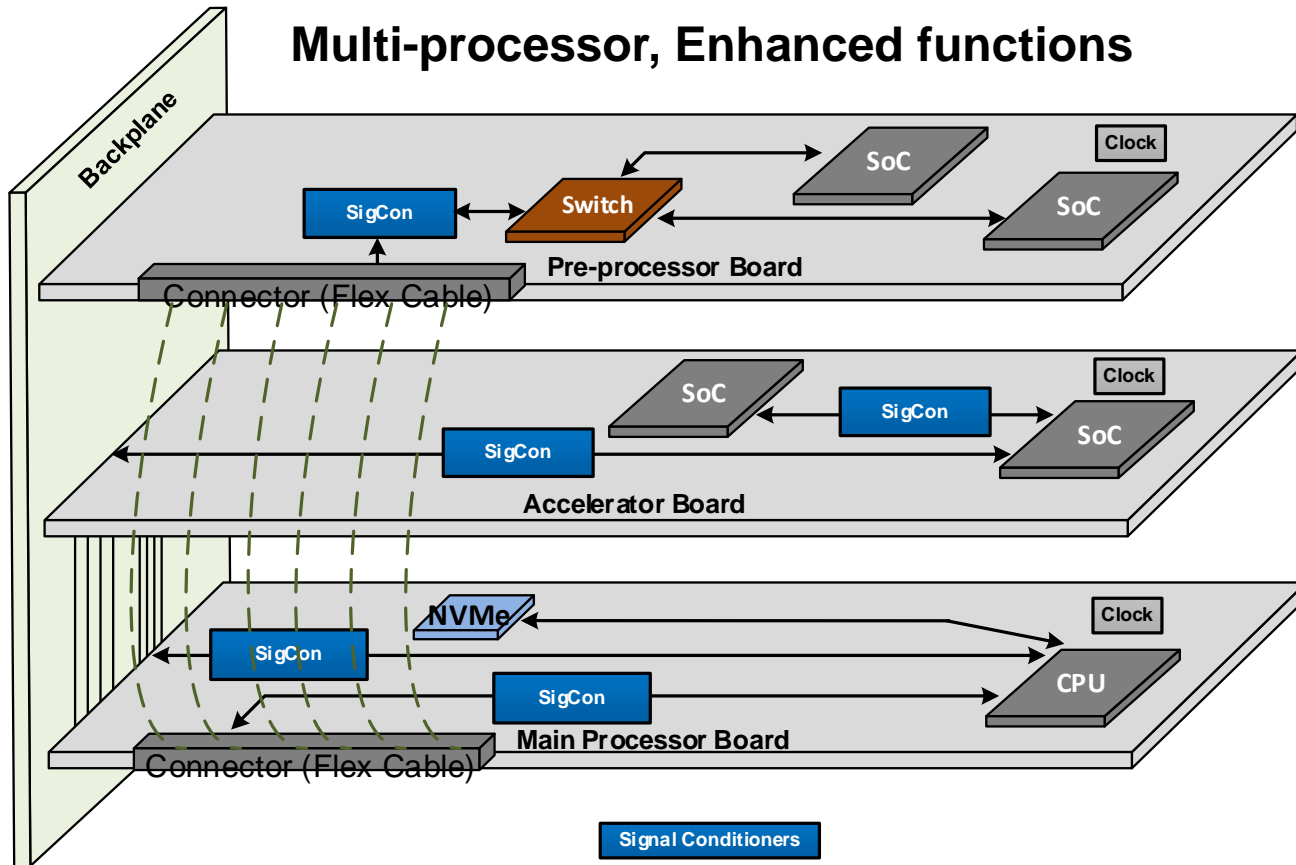


Advantage of using PCIe® technology:

- Native PCIe support by CPUs, SOC, FPGAs
- **Organic interface for intra-ECU short and mid range connectivity**
- Shared/coherent memory/ storage for distributed processing
- Direct PCIe connectivity to SSD storage
- Scalable compute power
- Software flexibility

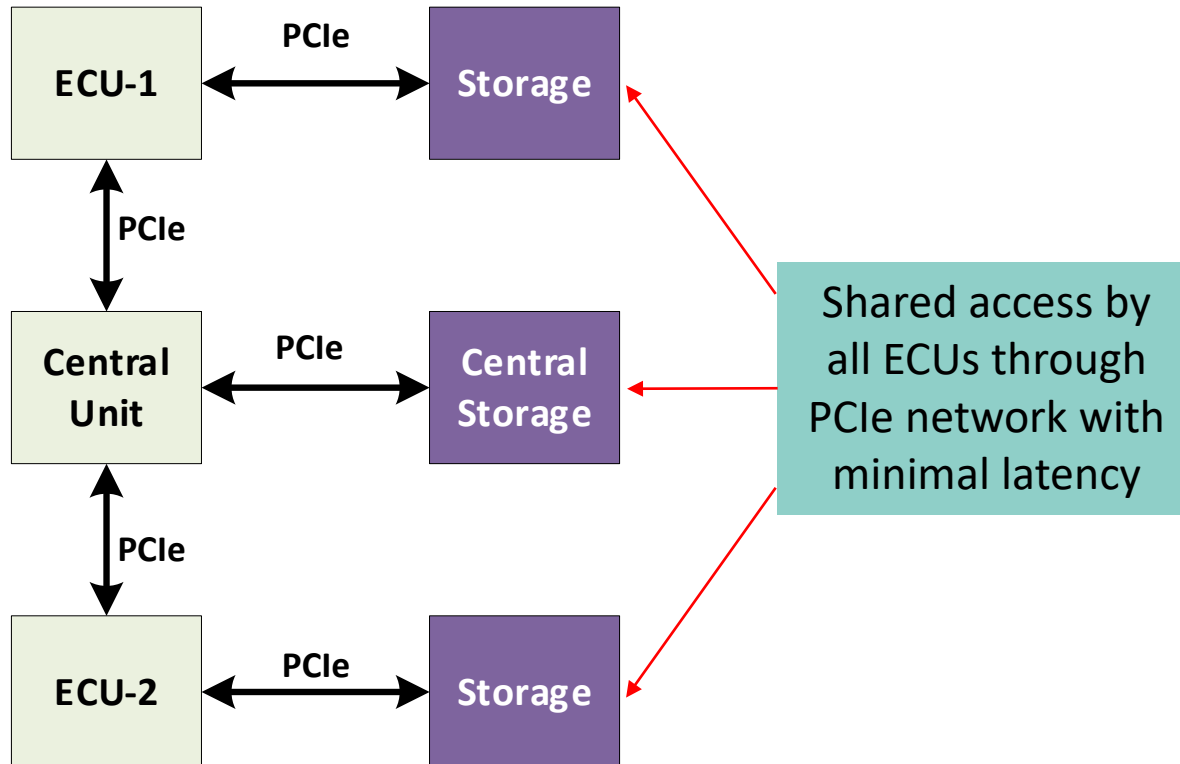
| Use Cases | Application |
|--------------------|--|
| Storage | BlackBox, ADAS/AV mapping, infotainment |
| Multi-processor | ADAS & IVI domain controllers, autonomous vehicle (AV), zonal arch. - central processing |
| Enhanced functions | ADAS & IVI domain controllers, autonomous vehicle (AV) |

PCIe® Technology for Intra-ECU Connectivity



- PCIe architecture provides most efficient connection between CPUs/SOCs/FPGAs
- Enables scalable compute power with added cards into the backplane
- PCIe links are contained within the ECU – short and medium range links
- Traditional channel interconnects – board traces, flex cables, backplane – known link loss
- Some links may require signal conditioning (redriver or retimer) device to extend reach

PCIe® Technology for Storage Connectivity



Applications:

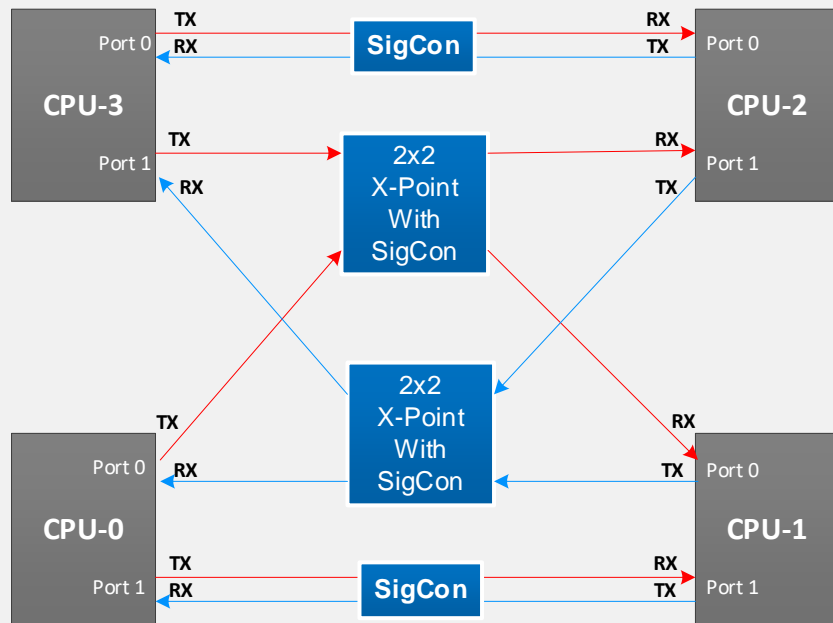
- Blackbox Recorders
- Mapping for Navigation & Real-Time Mapping for AVs
- Cockpit/Infotainment
- Central Processing

Storage Elements:

- Automotive Storage moving toward SSDs
- Spinning HD not as reliable
- SSD based storage moving from eMMC/UFS to PCIe/NVMe SSDs

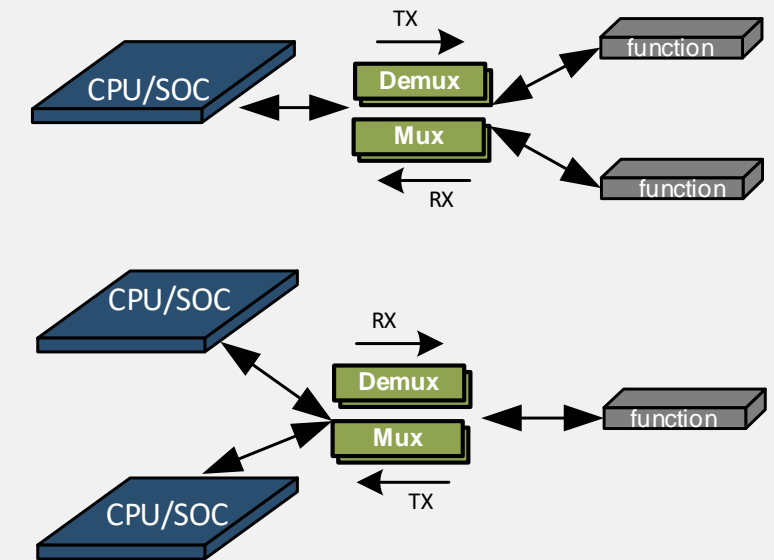
Scalable Compute Power Using PCIe® Network

- Higher level of autonomy driving compute horsepower needs
- Automotive platforms' need vary from one to another
- A common architecture with scalable compute power desired – with flexible CPU count and connectivity
- Redundancy and diagnostics critical for automotive applications



Flexible CPU to CPU connectivity

- Multiple CPUs allows simultaneous processing
- Increased reliability with CPU redundancy
- Modern computers have multiple CPUs with multiple cores each
- Low latency is critical
- Loss well defined



- Redundant connections for reliability
- Bypass connections for diagnostics

Signal Conditioning

- PCIe® link budget
- Redrivers and retimers
- Reach extension

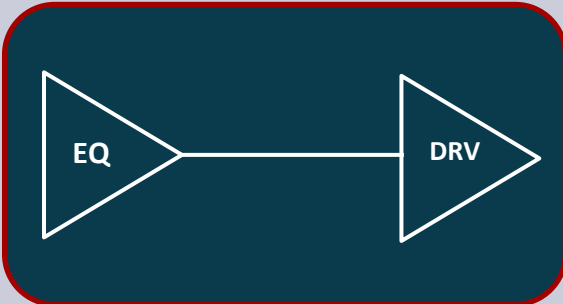
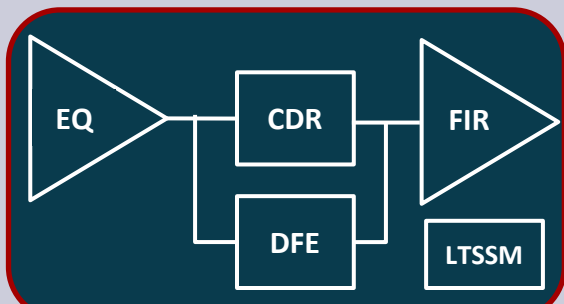
PCIe® Link Loss Budget

Typical PCIe Link Loss Budget:

| PCIe Rev | Total Loss Budget | Root Package | CEM Connector | Add-in Card (AIC) | System Base Board |
|---------------|-------------------|--------------|---------------|-------------------|-------------------|
| 3.0 (8 GT/s) | 22 dB | 3.5 dB | 1.7 dB | 6.5 dB | 10.3 dB |
| 4.0 (16 GT/s) | 28 dB | 5.0 dB | 1.5 dB | 8.0 dB | 13.5 dB |
| 5.0 (32 GT/s) | 36 dB | 9.0 dB | 1.5 dB | 9.5 dB | 16.0 dB |

- PCIe link training optimizes TX/RX equalization of root complex (RC) and End Point (EP) to achieve best electrical link
- PCIe link budget calculations are done mostly for server & PC platforms
 - Automotive use cases can be different
- Signal integrity challenge for short and medium range intra-ECU links are similar to server/PC platforms
 - PCIe technology's inherent reach enough for many very short reach intra-ECU links
 - Where reach extension needed, redrivers typically suitable. Retimers are also option
- Retimers are typically required for long range inter-ECU using automotive cables

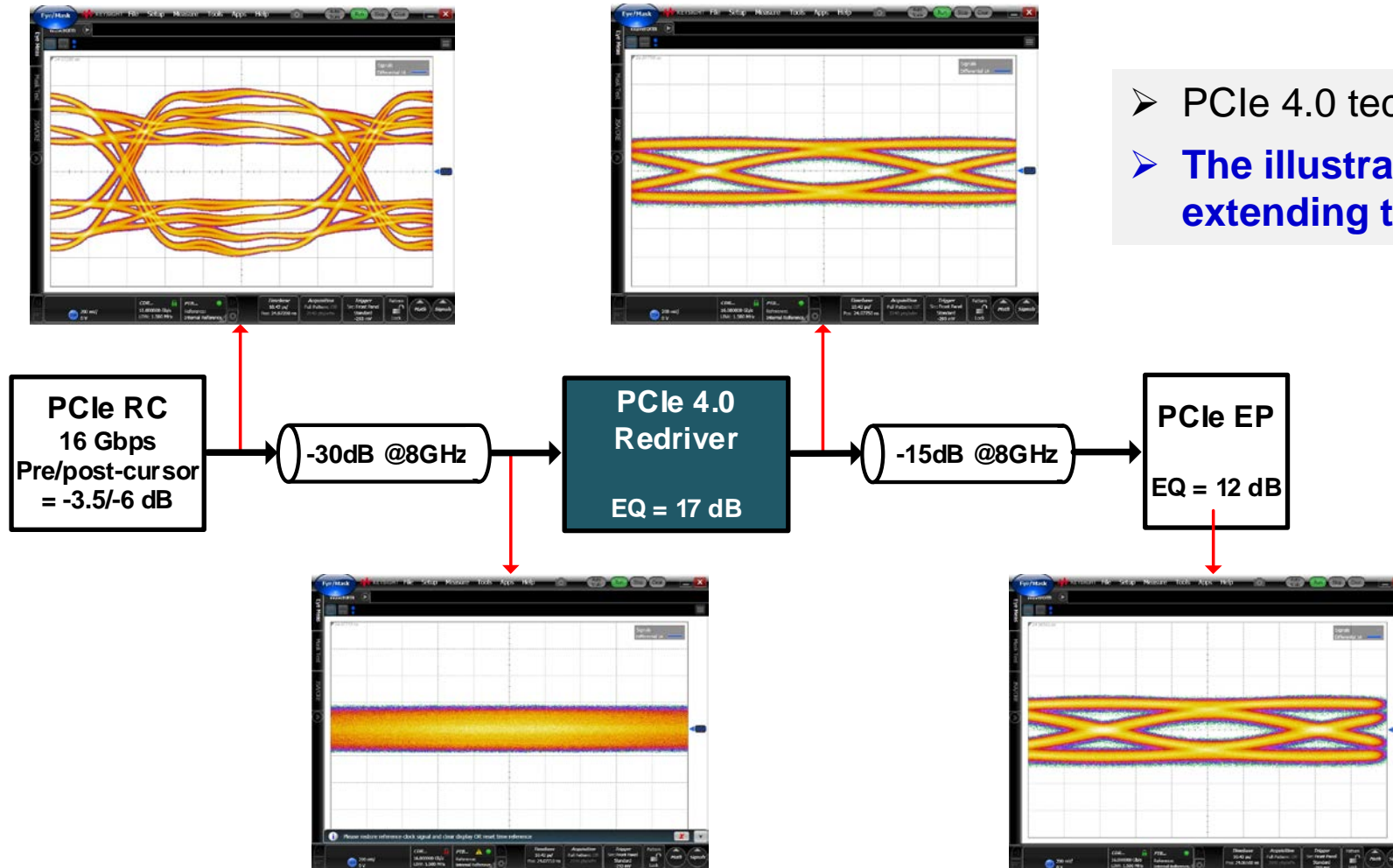
Linear Redriver and Retimer for Signal Conditioning

| Linear Redriver – for short/medium range | Retimer – for long range links |
|--|---|
| <p>Latency critical use cases such as CPU/SOC to CPU/SOC connectivity</p>  | <p>Links with jitter, crosstalk, reflections & lane-to-lane skew issues</p>  |

| | Advantages | Disadvantages |
|------------------------|---|--|
| Linear Redriver | <ul style="list-style-type: none"> Typically 50% reach extension - helps with insertion loss Protocol-agnostic and allow link training un-hindered Simple component in the link, ref clock not required Ultra-low latency, low power, low cost option | <ul style="list-style-type: none"> Reach extension is limited and can only be used in moderate loss links Manual CTLE tuning is often needed, unsuitable for applications with topology uncertainty |
| Retimer | <ul style="list-style-type: none"> Provide 2X reach extension - helps with insertion loss, jitter, crosstalk, reflections & skew - resets jitter budget Protocol aware - fully participates in link training Typically includes adaptive CTLE/DFE, diagnostic features | <ul style="list-style-type: none"> Complex element in the link, ref clock is required Higher power, increased latency (still lower than alternate solutions), and more expensive option |

PCIe® 4.0 Specification Reach Extension using Signal Conditioning

- PCIe 4.0 technology link budget 28dB
- The illustration shows a SigCon device extending the reach from 28dB to 45dB



Summary

Summary

- PCIe® technology offers many advantages for automotive applications that include:
 - Native to CPUs, SOCs and FPGAs
 - Ultra low latency, reliability, scalability
 - Efficient shared memory access
 - Availability of software
- In this webinar:
 - We discussed opportunities and challenges for PCIe technology as interface for automotive backbone and inter-ECU connectivity
 - We also discussed how PCIe technology suits well for intra-ECU CPU-to-CPU and storage connectivity
- PCIe architecture is expected to have key role in automotive connectivity revolution, but we have many challenges to overcome
- Please join PCIe Automotive Working Group (AWG) to share your opinions and expertise

Questions?

**Thank you for attending the third entry in the
PCI-SIG® Automotive Webinar series**

**Information about upcoming webinars will be
available soon**

**For more information or to download these
slides, please visit www.pcisig.com**