PCI Express® Electrical Basics

Rick Eads
Keysight Technologies
Topics

- PCI Express® Overview
- Enhancements for 8GT/s
- Target channels for the specification
- Electrical signaling
- Transmitter
- Receiver
- SEASIM
Electrical Features

- Data rates 2.5GT/s, 5GT/s and 8GT/s
- $10^{-12}$ bit error ratio
- AC coupled
- Link widths 1, 2, 4, 8, 16, 32 lanes
- Hot swap capable
- 2.5 and 5GT/s scrambled + 8b10b
- 8GT/s scrambled + 128/130
- Power management
Doubling from 5GT/s

- Major goal was to make PCIe® 3.0 evolutionary
  - Support existing usage models
  - Preserve Common Reference Clock and Data Clocked modes
  - Re-use of 5GT/s reference clock generators
  - Re-use of silicon PHY architectures

- Evaluated channels at 10GT/s and 8GT/s
  - 10GT/s would have allowed 8b10b coding to be preserved

- Shown that a non-linear increase in difficulty to reach 10GT/s
  - Increased channel improvement cost
  - Increased power in silicon
  - Increased difficulty for eco-system

- Concluded the cost of changing encoding acceptable
  - A new scrambled encoding scheme was developed
  - Efficiency 20% better than 8b10b
8GT/s Enablers

- Receiver equalization required
- Introduce statistical channel analysis
  - Channel compliance & simulation with behavioral Tx/Rx
- Mitigate baseline wander & crosstalk
  - Polynomial choice of 128/130 code on individual lanes
  - Baseline wander:
    - LFSR offsets between adjacent lanes reduces simultaneous switching

Red: vict+2aggr; pink: vict+1aggr; black: vict only
Target Channels
PCI Express Channels

- Channel specification
  - No formal spec for 2.5 and 5GT/s
    - Channel budget implied
  - 8GT/s introduces time domain spec
  - Card Electromechanical (CEM) spec sets limits and measurement points

- Two worst case models assumed
  - Client CEM
    - Short to medium length (3-12”), reflection and crosstalk dominated
  - Server CEM
    - Medium to long (20”) loss dominated
Typical Client Topology

4-layer microstrip 3-7” with PTH via stubs

Add in card 3-4”
Typical Server Topology

6-8 layers, 20”, 1 or 2 connectors
Stripline with via stubs
Bidir TDR of 2-Connector Server Channel

Connector transitions clearly visible in TDR data
8.0GT/s Statistical Channel Analysis

- Tx Clock
- Rx Sampling Clock
- Lossy Channel
- Channel impulse response
- Statistical ISI Analysis Tool
- Tx jitter distribution
- Equalization coefficients
- Xtalk impulse responses
- Rx sample timing & voltage uncertainty distributions
- Pre-aperture BER eye
- Post-aperture BER eye

8.0GT/s specification plane
Electrical Signaling
Optional on-die AC coupling for 8b10b
8GT/s allows floating Rx common-mode

Tx

Rx Detect

AC Coupled Channel

Tunable Rx EQ 8GT/s

Rx

Vcm

Rx term

Optional on-die AC coupling for 8b10b
8GT/s allows floating Rx common-mode

Tx EQ 2-tap 2.5/5GT/s,
3-tap 8GT/s
Transmit De-Emphasis

Transmitter circuits use De-Emphasis to equalize the frequency response of the channel in order to minimize inter-symbol interference.

Available Equalization Settings:
- 2.5GT/s: [-3.5dB]
- 5.0GT/s: [-3.5dB, -6dB]
- 8.0GT/s: [-3.5dB, -6dB, pre-cursor]
  * 10-presets
  * coefficient tuning space
De-Emphasis Pulse & Frequency Domain Response

Inter Symbol Interference

Reduced smearing into next symbol UI

Flatened “equalized” response

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\[ V_{TX} = V_{PK} \sum_{n=0}^{k} c_n d_{m-n} \quad \text{and} \quad \sum_{n=0}^{k} |c_n| = 1 \]

\( V_{TX} \) is output voltage and \( V_{PK} \) the peak voltage
\( k \) is number of Tx coefficients
\( d \) is vector of +1 and -1 for logic 1 and 0
\( m \) is the index into the bit stream
For a 3 tap Gen3 FIR \( c_1 \) is positive and \( c_0 \) and \( c_2 \) are negative
data is delayed by 1UI

For data stream 00010111
\( V_{PK} = 1 \) and \( t_0 = -c_0; \quad t_1 = c_1; \quad t_2 = -c_2 \)

000 → \(+t_0 - t_1 + t_2\)
001 → \(-t_0 - t_1 + t_2\)
011 → \(-t_0 + t_1 + t_2 \rightarrow V_a\)
111 → \(-t_0 + t_1 - t_2 \rightarrow V_b\)
110 → \(+t_0 + t_1 - t_2 \rightarrow V_c\)

\[ \text{deemphasis} = 20\log_{10} \frac{V_b}{V_a} \]
\[ \text{preshoot} = 20\log_{10} \frac{V_c}{V_b} \]

Fully specified by
\( V_{TX-DE-RATIO} \) (0 to -8dB)
\( V_{TX-PS-RATIO} \) (0 to +3dB)
Transmitter
Transmitter Reference Plane

- Reference plane is DUT pin
  - Most convenient manufacturing boundary
- For 2.5 and 5GT/s
  - Package losses are part of Tx performance
- For 8GT/s die pad, package route and package pin interactions are more significant
  - Makes fixture de-embedding inaccurate
  - Tx EQ and jitter measurements inaccurate
- Use data-dependent jitter separation
  - Effectively measure Tx jitter at die pad
  - Use LF measurement technique for presets at pin
Transmitter

- Differential ~100ohm transmitter
  - FS: 800-1200mV, HS: 400-800mV
  - 0.75UI eye opening
- 2.5/5GT/s 2-tap EQ
  - FS: -3.5dB and -6dB, HS: 0dB
- 8GT/s 3-tap EQ
  - 10 presets, min boost 8dB, coefficient tuning space
- AC coupled channel series capacitor
  - 2.5/5GT/s 75-265nF
  - 2.5/5/8GT/s (Rev 3.0) 176-265nF
- Return Loss
  - SDD11 -10dB 2.5GT/s, -8dB 5GT/s, -4dB 8GT/s (differential)
  - SCC11 -6dB, -3dB 8GT/s (common-mode)
PCle 3.0 Tx Jitter

- PCIe 3.0 Tx jitter is separated into two categories
  - Data Dependent: package loss, reflections, ISI
  - Uncorrelated Jitter: PLL jitter, power supply, duty cycle error

- Pulse Width Jitter (PWJ)
  - PWJ is a subset of uncorrelated jitter
  - PWJ is amplified by channel loss
  - Edges are assumed to be independent

- Relationship between pulse width jitter and edge jitter
  - Important for measurement and channel simulation tools

\[
PWJ = PW_{\text{max}} - PW_{\text{min}}
\]

\[
\text{Edge Jitter DJ} = \frac{PWJ_{\text{DJ}}}{2}
\]

\[
\text{Edge Jitter RJ} = \frac{PWJ_{\text{RJ}}}{\sqrt{2}}
\]
Receiver
### Receiver

- **2.5/5GT/s open eye specification, validated at device pin, package included in device budget**
  - Eye height 175/120mV 2.5/5GT/s
  - Eye width 0.4/0.32UI 2.5/5GT/s
  - AC common-mode 300mV pk-pk

- **8GT/s closed eye at pin, specified after applying behavioral receiver**
  - Defines minimum Rx EQ performance
  - Used for both Rx stressed eye calibration and channel compliance
  - Eye height 25mV 8GT/s
  - Eye width 0.3UI 8GT/s
  - AC common-mode 150mV pk-pk (EH<100mV) 250mV (EH>=100mV)
Receiver Cont.

- **Termination**
  - ✔ 100ohm differential
  - ✔ 50ohm common-mode
    - 0v common-mode for detect
    - At 8GT/s Rx allowed to float common-mode
      - Requires LTSSM changes to avoid dead-locks

- **Differential-mode return loss**
  - ✔ 10dB 2.5GT/s, 8dB 5GT/s, 5dB 8GT/s

- **Common-mode return loss**
  - ✔ 6dB 2.5/5GT/s, 5dB 8GT/s
Behavioral Rx DFE

Block diagram of CTLE and 1-tap DFE

\[ Y_k = X_k - d_1 \times \text{sgn}(Y_k - 1) \Rightarrow \text{DFE summer Vdiff output} \]
\[ Y^*_k \Rightarrow \text{Decision Fn output voltage} \Rightarrow |Y^*_k| = 1 \]
\[ X_k \Rightarrow \text{DFE Vdiff output voltage} \]
\[ d_1 \Rightarrow \text{DFE feedback coefficient} \quad K \Rightarrow \text{sample index} \]
Rx Linear EQ

\[ H(s) = \frac{sC_1R_1R_2 + R_2}{sC_1R_1R_2 + R_1 + R_2} \cdot \frac{1}{sC_2R_3 + 1} \]

\[ H(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{s}{\omega_z + 1} \cdot \frac{1}{s + \frac{s}{\omega_{p_1}} + 1} \]

\[ G_{DC} = \frac{R_2}{R_1 + R_2} \]

\[ \omega_{p_1} = \frac{R_1 + R_2}{C_1R_1R_2} \]

\[ \omega_z = \frac{1}{C_1R_1} = G_{DC} \omega_{p_1} \]

\[ \omega_{p_2} = \frac{1}{C_2R_3} \]

Closer pole1 is to 4GHz the more attenuation at bit rate

8GT/s Tuning Range
1dB step size

Fully specified by DC\textsubscript{Gain} (dB)
\( F\textsubscript{Pole1} \) (Hz)
\( F\textsubscript{Pole2} \) (Hz)
Stressed eye calibrated at pin reference plane
Error rate measured using loopback
Pass BER $10^{-12}$
Frequency domain mask used for ISI stress to match tuning range of Rx EQ
Validates that Rx can track LF jitter from refclk and Tx
Seasim
High Speed Channel Simulation Challenges

- Channel response at >4GHz is affected by large number of features in the channel
  - Pre-layout evaluation of topology choices is a complicated multi-dimensional problem
  - Need to be able to quickly build and test many different options
  - Large number of HVM permutations need to be evaluated to determine robustness of solution
- Seasim has been developed to allow EWG members to efficiently evaluate these options
Seasim Introduction

- A GUI form based interface
  - Underlying config file interface to seasim provides spec jitter parameters for channel simulations
  - A simple form based dialogue tool added
  - Tab based interface to group config controls by context
  - Ability to save and load configurations
  - Launch (and kill) seasim from GUI

- Touchstone channel modeling
  - A set of Touchstone files can be cascaded to form die-pad to die-pad channel
  - A vector of left hand and right hand ports define connections between S-parameters
  - Rx port and set of Tx ports define step responses to be generated
  - Tx amplitude and Gaussian bandwidth can be specified
Seasim Channel Analysis

- Allows what-if analysis on the channel components by changing the Touchstone files that are concatenated together for the channel.
- Different analyses can be selected as the channel is ‘tuned’.
- Either a pre-saved config can be loaded or the pcie-gen3.inc for normal sim conditions.
- The other tabs allow simulation conditions to be changed from the default config.
Seasim Port Definitions

- Touchstone tuple port definitions
  - Reflects the S-parameter models intrapair net order
  - Provides pair-to-pair (victim/aggressor) relationship for crosstalk inclusion

- Transmitter ports
  - Allows renormalization of port impedance by providing a list of terminal impedance values
  - Define transmitter pad differential voltage amplitude
  - Transmitter bandwidth defined by Gaussian filter setting

- Receiver port
  - Provide custom port renormalization impedance
Seasim Jitter Configuration

- **Jitter**
  - Consistent jitter definitions with the PCIe base spec
  - Default jitter settings can be loaded with the default configuration file
  - Jitter values can also be customized using the field in the GUI and saved

- **Noise**
  - Random low frequency noise can be defined in addition to the aggressor-victim coupling present in the Touchstone file
Seasim Equalization

- **Tx FIR Filter**
  - Can either fix pre-shoot and de-emphasis or set coefficient search space for adaptation

- **Rx Linear Equalizer**
  - Define pole/zero value or range of values for adaptation
  - May cascade multiple continuous time LEQ filters

- **Decision Fed Equalizer**
  - Can enable multiple DFE taps beyond defaults
  - Can vary dynamic range of taps independently
Seasim Step Responses

- Channel Step Response
  - Alternative simulation method to providing channel S-parameter models
  - Measured or simulated voltage-time records of channel step responses can be used directly for statistical simulation

- Crosstalk
  - Independent waveforms can be supplied for the inclusion of aggressor coupling to the victim receiver
  - Can optionally offset the aggressor-to-victim alignment
Seasim Sweep

- Seasim can be used to define HVM sweeps
- The channel model can be swept to represent manufacturing variations of impedance or loss
- To consider the impact of different PCB layout the length of different channel segments can be swept
- Seasim will launch jobs in parallel then collect results and plot them
Seasim Channel Simulation
Frequency Response & Bidir TDR
Seasim Sweep Results Analysis Plots
PCIe 2.x simulation requires calibrating the transmitter De-emphasis and signal amplitude at the package pin (i.e. -6dB/0.8V/0.9UI)
Waveform simulated at the receiver pin of the 8GT/s compliance channel.

Simulated at the receiver pin of the 8GT/s compliance channel. PCIe 2.x min is 120mV/0.4UI.

Simulated at the receiver pad using the 8GT/s spec Tx pkg + spec channel + spec Rx pkg.
Eye distortions are calibrated independently to mitigate the noise floor of the test equipment.
Three Phases to Calibration

- Channel ISI and behavioral Rx EQ
  - Calibrate loss from TP1 to TP2
    - Fine adjustment with generator equalization
  - Use base spec PDA search for CTLE and DFE settings
    - Constrained to be no better than what’s used in channel compliance
- Phase jitter, differential voltage noise and common-mode noise
  - Use Seasim to calculate required RJ & VN
  - Set and measure RJ & SJ at TP1
    - Assumes jitter amplification in channel is negligible
  - Set and measure VN & CMN at TP2
    - VN de-embedded from ideal Rx-latch back to TP2
- Cumulative eye measurement
  - All distortions applied, extrapolate and interpolate to $10^{-12}$ & $10^{-6}$
VNA Measurement TP1 to TP2

Needs to include all cables used for measurement.
- Scope averaged and interpolated step response at TP2
- 128 UI 1/0 clock waveform
- 1ps time steps
- Pad waveform is TP1 channel extended by behavioral package to Rx die pad

- Difference between TP2P and TP2 (-4.1dB) at 2.1GHz used to de-embed VN to TP1
*May need to iteratively tune generator amplitude and VN to get $EW > 0.3\text{UI}$ and $EH = 25\text{mV}$
Thank you for attending the PCIe Technology Seminar

For more information please go to

www.pcisig.com
Backup
Derivation of Coefficients

\[ DE = \frac{V_b}{V_a}; \quad PS = \frac{V_c}{V_b} \]

\[ t_0 + t_1 + t_2 = 1; \quad t_1 = 1 - t_0 - t_2 \]

\[ DE = \frac{V_{pk}(t_0 + t_1 - t_2)}{V_{pk}(-t_0 + t_1 + t_2)} = \frac{1 - 2t_0 - 2t_2}{1 - 2t_0} \]

\[ PS = \frac{V_{pk}(t_0 + t_1 - t_2)}{V_{pk}(-t_0 + t_1 + t_2)} = \frac{1 - 2t_2}{1 - 2t_0 - 2t_2} \]

\[ DE \cdot PS = \frac{1 - 2t_2}{1 - 2t_0} \]

\[ 2t_2 = 1 - DE \cdot PS(1 - 2t_0) \]

\[ 2t_2 = 1 - DE \cdot PS + 2DE \cdot PS t_0 \]

\[ 2t_2 = 1 - DE \cdot PS + DE \cdot PS \cdot \frac{DE(PS - 1)}{1 + DE(PS - 1)} \]

\[ 2t_2 = \frac{(1 + DE(PS - 1))(1 - DE \cdot PS) + DE^2 \cdot PS(PS - 1)}{1 + DE(PS - 1)} \]

\[ 2t_2 = \frac{1 - DE \cdot PS + DE (PS - 1) - DE^2 \cdot PS(PS - 1) + DE^2 \cdot PS(PS - 1)}{1 + DE(PS - 1)} \]

\[ 2t_2 = \frac{1 - DE \cdot PS + DE \cdot PS - DE}{1 + DE(PS - 1)} \]

\[ t_2 = \frac{1 - DE}{2 + 2DE(PS - 1)} \]

## Tx FIR Coefficients

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