# PCI SIG

## **PCI Express® Electrical Basics**

#### Rick Eads Keysight Technologies







- PCI Express<sup>®</sup> Overview
- Enhancements for 8GT/s
- Target channels for the specification
- Electrical signaling
- Transmitter
- Receiver
- SEASIM



## **Electrical Features**

- Data rates 2.5GT/s, 5GT/s and 8GT/s
- 10<sup>-12</sup> bit error ratio
- AC coupled

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- Link widths 1, 2, 4, 8, 16, 32 lanes
- Hot swap capable
- 2.5 and 5GT/s scrambled + 8b10b
- 8GT/s scrambled + 128/130
- Power management



## Doubling from 5GT/s

- Major goal was to make PCIe<sup>®</sup> 3.0 evolutionary
  - ✓ Support existing usage models
  - Preserve Common Reference Clock and Data Clocked modes
  - ✓ Re-use of 5GT/s reference clock generators
  - ✓ Re-use of silicon PHY architectures
- Evaluated channels at 10GT/s and 8GT/s
  - 10GT/s would have allowed 8b10b coding to be preserved

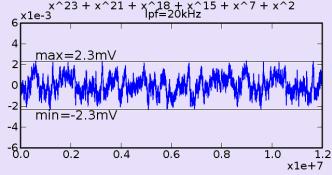
#### Shown that a non-linear increase in difficulty to reach 10GT/s

- Increased channel improvement cost
- Increased power in silicon
- ✓ Increased difficulty for eco-system
- Concluded the cost of changing encoding acceptable
  - ✓ A new scrambled encoding scheme was developed
  - ✓ Efficiency 20% better than 8b10b



# **8GT/s Enablers**

- Receiver equalization required
- Introduce statistical channel analysis
  - Channel compliance & simulation with behavioral Tx/Rx
- Mitigate baseline wander & crosstalk
  - Polynomial choice of 128/130 code on individual lanes
  - ✓ Baseline wander:



LFSR offsets between adjacent lanes reduces simultaneous switching







## **Target Channels**

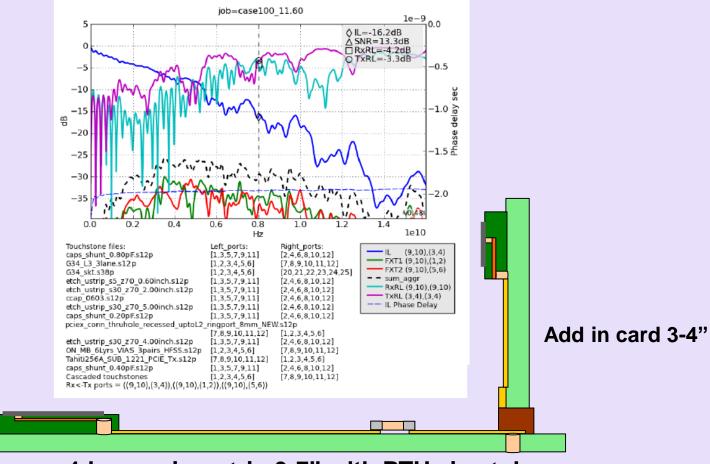


- Channel specification
  - ✓ No formal spec for 2.5 and 5GT/s
    - Channel budget implied
  - ✓ 8GT/s introduces time domain spec
  - Card Electromechanical (CEM) spec sets limits and measurement points
- Two worst case models assumed
  - ✓ Client CEM
    - Short to medium length (3-12"), reflection and crosstalk dominated
  - ✓ Server CEM
    - Medium to long (20") loss dominated





#### **Typical Client Topology**

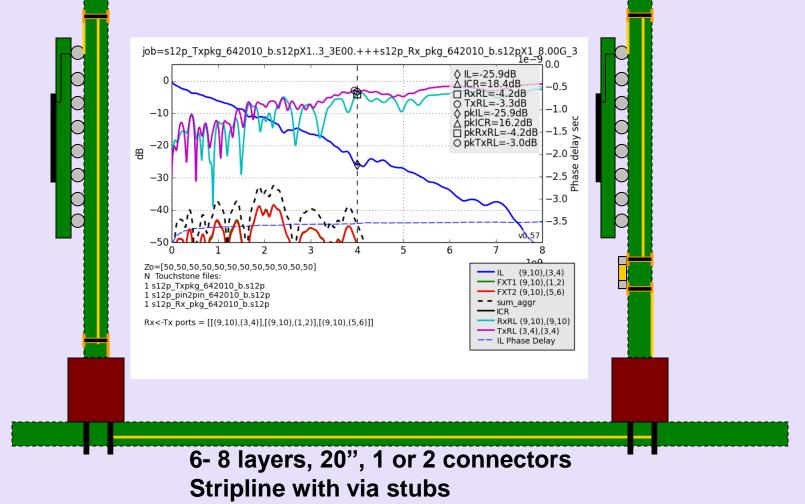


4-layer microstrip 3-7" with PTH via stubs



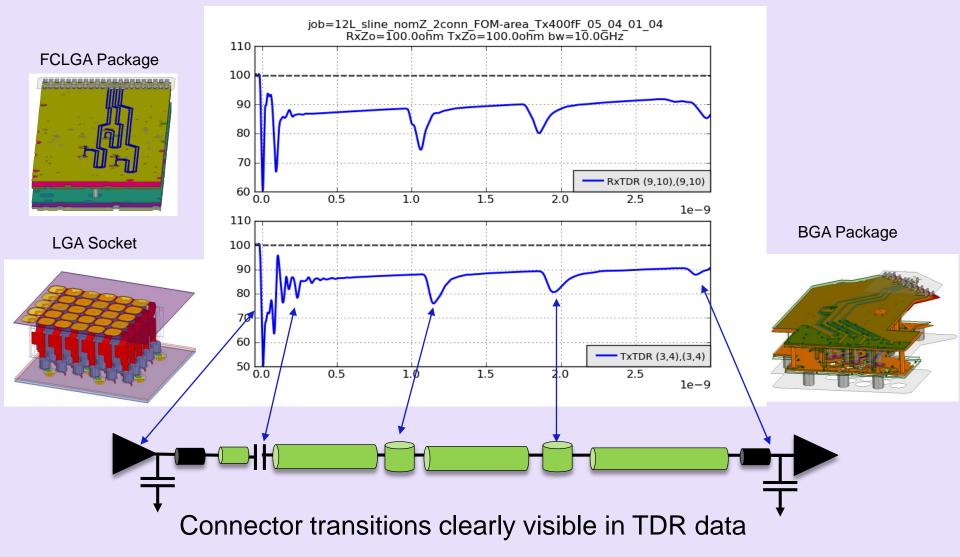
# Server Channel

#### **Typical Server Topology**

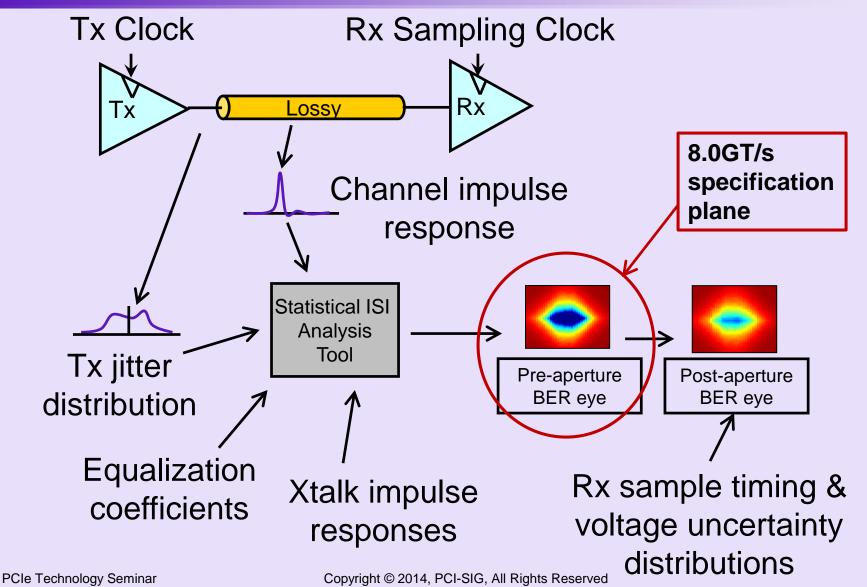


### Bidir TDR of 2-Connector Server Channel





### 8.0GT/s Statistical Channel Analysis

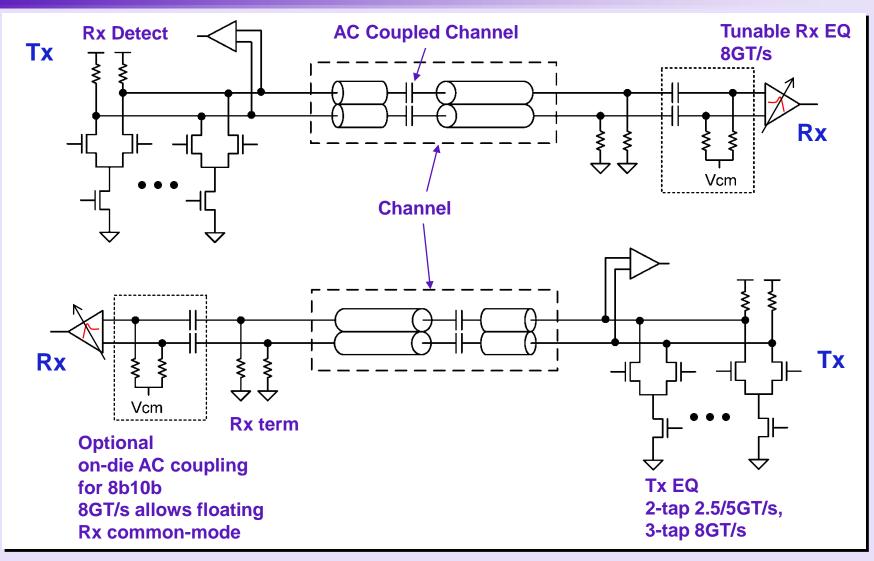




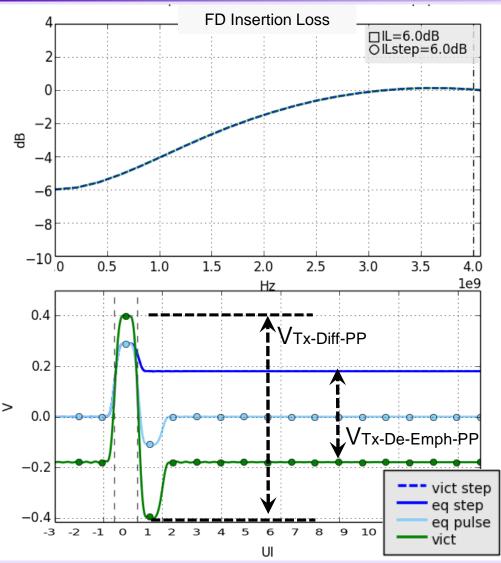


## **Electrical Signaling**

# Transceiver and Channel







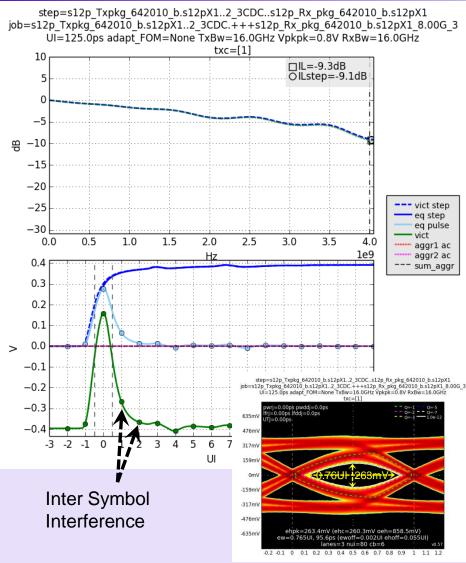
Transmitter circuits use De-Emphasis to equalize the frequency response of the channel in order to minimize intersymbol interference

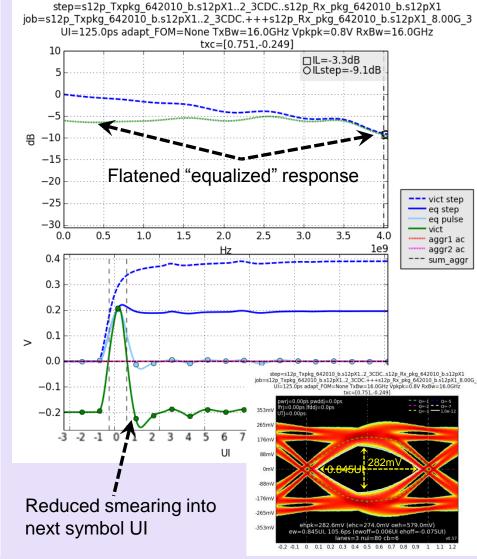
Available Equalization Settings:

2.5GT/s: [-3.5dB]

- 5.0GT/s: [-3.5dB, -6dB]
- 8.0GT/s: [-3.5dB, -6dB, pre-cursor]
  - \* 10-presets
  - \* coefficient tuning space

# De-Emphasis Pulse & Files Frequency Domain Response



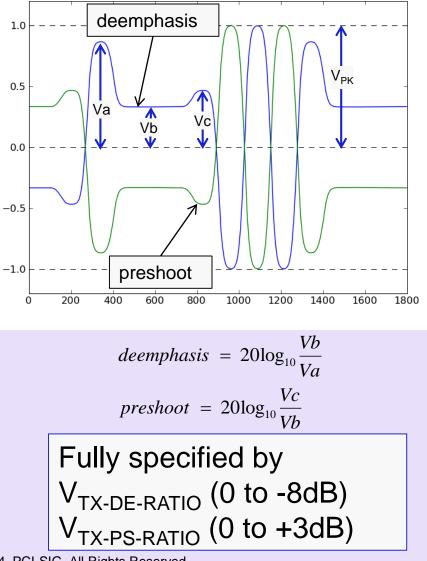




$$V_{TX} = V_{PK} \sum_{n=0}^{k} c_n d_{m-n}$$
 and  $\sum_{n=0}^{k} |c_n| = 1$ 

 $V_{TX}$  is output voltage and  $V_{PK}$  the peak voltage k is number of Tx coefficients d is vector of +1 and -1 for logic 1 and 0 m is the index into the bit stream For a 3 tap Gen3 FIR  $c_1$  is positive and  $c_0$  and  $c_2$  are negative data is delayed by 1UI

For data stream 00010111  $V_{PK} = 1 \text{ and } t_0 = -c_0; \quad t_1 = c_1; \quad t_2 = -c_2$   $000 \rightarrow +t_0 - t_1 + t_2$   $001 \rightarrow -t_0 - t_1 + t_2$   $011 \rightarrow -t_0 + t_1 + t_2 \rightarrow Va$   $111 \rightarrow -t_0 + t_1 - t_2 \rightarrow Vb$  $110 \rightarrow +t_0 + t_1 - t_2 \rightarrow Vc$ 







### **Transmitter**

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**Transmitter Reference Plane** 

- Reference plane is DUT pin
  - Most convenient manufacturing boundary
- For 2.5 and 5GT/s
  - ✓ Package losses are part of Tx performance
- For 8GT/s die pad, package route and package pin interactions are more significant
  - Makes fixture de-embedding inaccurate
  - Tx EQ and jitter measurements inaccurate
- Use data-dependent jitter separation
  - Effectively measure Tx jitter at die pad
  - Use LF measurement technique for presets at pin

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- Differential ~100ohm transmitter
  - ✓ FS: 800-1200mV, HS: 400-800mV
  - ✓ 0.75UI eye opening
- 2.5/5GT/s 2-tap EQ
  - ✓ FS: -3.5dB and -6dB, HS: 0dB
- 8GT/s 3-tap EQ
  - ✓ 10 presets, min boost 8dB, coefficient tuning space
- AC coupled channel series capacitor
  - ✓ 2.5/5GT/s 75-265nF
  - ✓ 2.5/5/8GT/s (Rev 3.0) 176-265nF
- Return Loss
  - ✓ SDD11 -10dB 2.5GT/s, -8dB 5GT/s, -4dB 8GT/s (differential)
  - ✓ SCC11 -6dB, -3dB 8GT/s (common-mode)

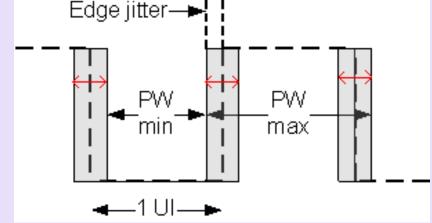


## **PCIe 3.0 Tx Jitter**

- PCIe 3.0 Tx jitter is separated into two categories
  - Data Dependent: package loss, reflections, ISI
  - Uncorrelated Jitter: PLL jitter, power supply, duty cycle error
- Pulse Width Jitter (PWJ)
  - PWJ is a subset of uncorrelated jitter
  - PWJ is amplified by channel loss
  - Edges are assumed to be independent

#### Relationship between pulse width jitter and edge jitter

Important for measurement and channel simulation tools



 $PWJ = PW_{max}-PW_{min}$ Edge Jitter DJ= PWJ\_DJ/2 Edge Jitter RJ = PWJ\_RJ/ $\sqrt{2}$ 

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#### Receiver

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- 2.5/5GT/s open eye specification, validated at device pin, package included in device budget
  - ✓ Eye height 175/120mV 2.5/5GT/s
  - ✓ Eye width 0.4/0.32UI 2.5/5GT/s
  - ✓ AC common-mode 300mV pk-pk
- 8GT/s closed eye at pin, specified after applying behavioral receiver
  - ✓ Defines minimum Rx EQ performance
  - Used for both Rx stressed eye calibration and channel compliance
  - ✓ Eye height 25mV 8GT/s
  - ✓ Eye width 0.3UI 8GT/s
  - AC common-mode 150mV pk-pk (EH<100mV) 250mV (EH>=100mV)



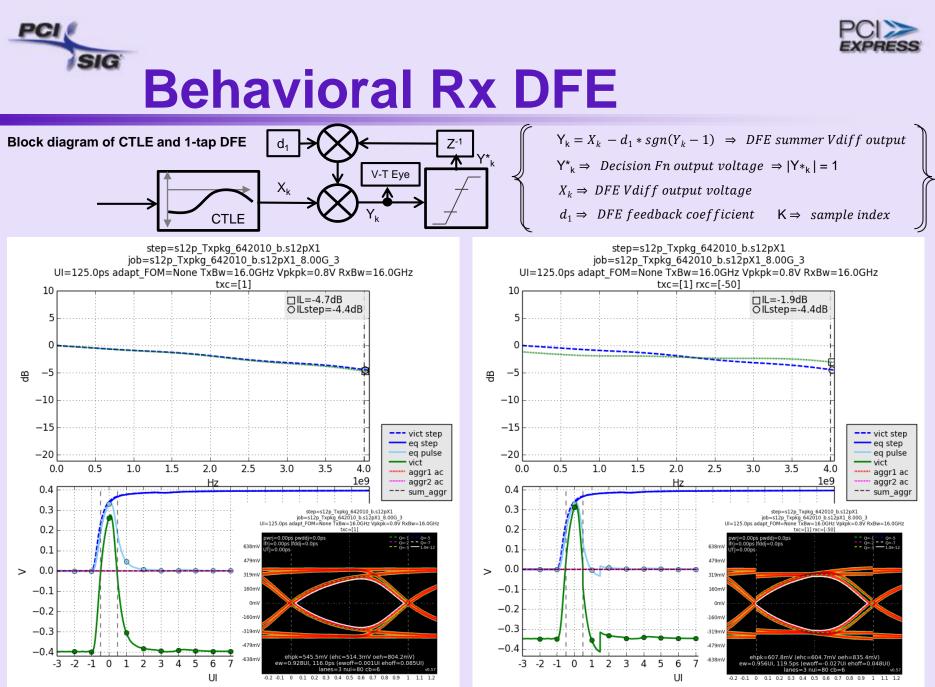


- Termination
  - ✓ 100ohm differential
  - ✓ 50ohm common-mode
    - 0v common-mode for detect
    - At 8GT/s Rx allowed to float common-mode
      - Requires LTSSM changes to avoid dead-locks
- Differential-mode return loss

✓ 10dB 2.5GT/s, 8dB 5GT/s, 5dB 8GT/s

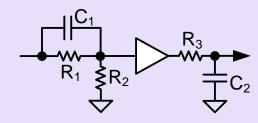
Common-mode return loss

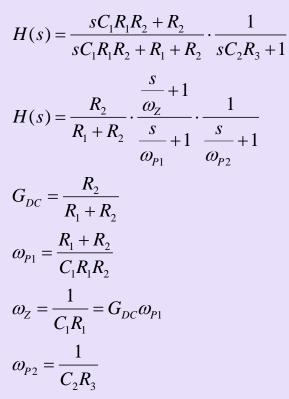
✓ 6dB 2.5/5GT/s, 5dB 8GT/s

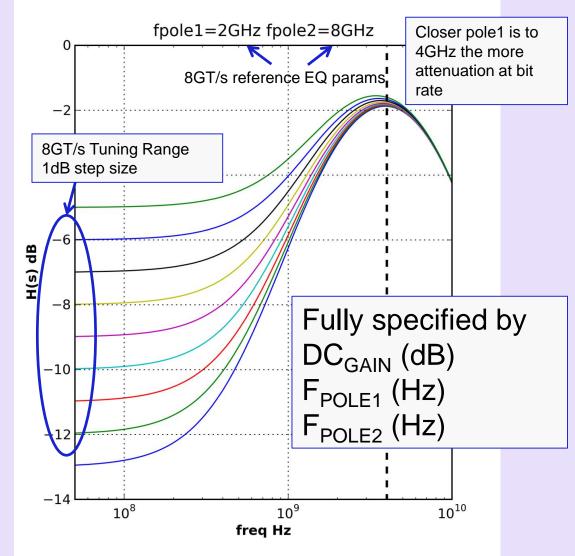




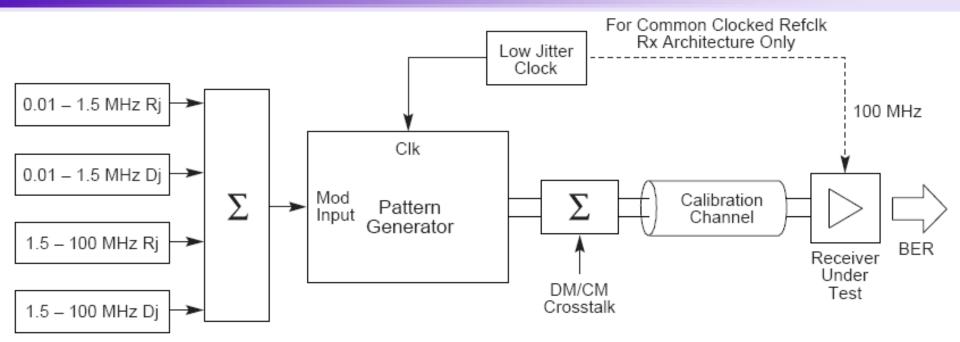






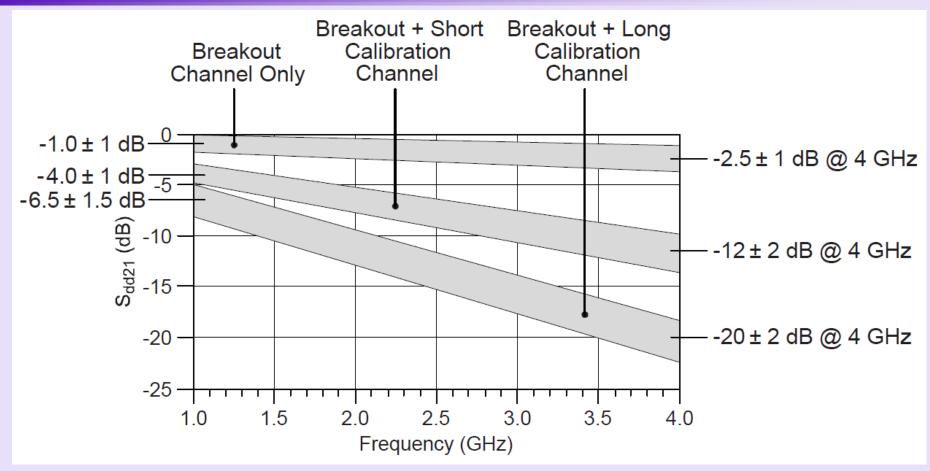






Stressed eye calibrated at pin reference plane Error rate measured using loopback Pass BER 10<sup>-12</sup>

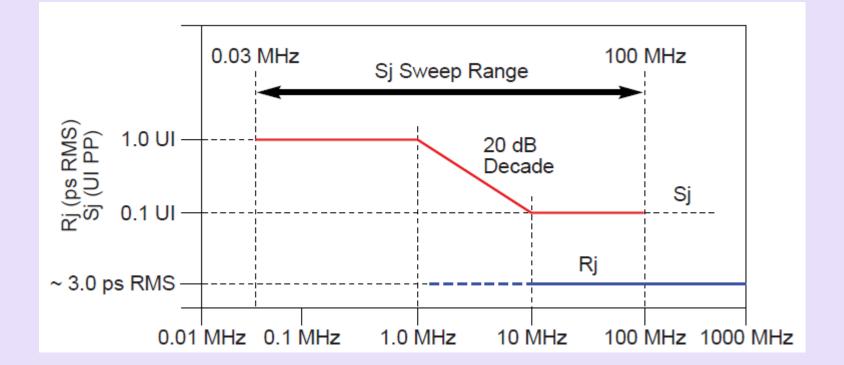
## **8GT/s Calibration Channels**



Frequency domain mask used for ISI stress to match tuning range of Rx EQ

### **8GT/s Receiver Jitter Tolerance Testing**





Validates that Rx can track LF jitter from refclk and Tx

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### **Seasim**

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## High Speed Channel Simulation Challenges



- Channel response at >4GHz is affected by large number of features in the channel
  - Pre-layout evaluation of topology choices is a complicated multi-dimensional problem
  - Need to be able to quickly build and test many different options
  - Large number of HVM permutations need to be evaluated to determine robustness of solution
- Seasim has been developed to allow EWG members to efficiently evaluate these options



Seasim Introduction

- A GUI form based interface
  - Underlying config file interface to seasim provides spec jitter parameters for channel simulations
  - ✓ A simple form based dialogue tool added
  - Tab based interface to group config controls by context
  - ✓ Ability to save and load configurations
  - ✓ Launch (and kill) seasim from GUI
- Touchstone channel modeling
  - A set of Touchstone files can be cascaded to form die-pad to die-pad channel
  - A vector of left hand and right hand ports define connections between Sparameters
  - ✓ Rx port and set of Tx ports define step responses to be generated
  - ✓ Tx amplitude and Gaussian bandwidth can be specified



**Seasim Channel Analysis** 

- Allows what-if analysis on the channel components by changing the Touchstone files that are concatenated together for the channel
- Different analyses can be selected as the channel is 'tuned'
- Either a pre-saved config can be loaded or the pcie-gen3.inc for normal sim conditions
- The other tabs allow simulation conditions to be changed from the default config

File	Inc	lud	e								
Mai	n	S-F	Parameters Jitt	ter/Noise Equalizers Step Responses Configu			ration Sweep				
19 1			C1	-			,		1004		
			one files	V		Plot S-parameter	S		1		
Statistical Eye 🗹 Measure EIEOS											
							V				
Job name				proc_pcie3_tx_enablement							
			se relative path	step_responses							
Base	e nar	ne t	for step								
			102 502 10221	/S-para	meters						
S-parameter relative path				1.5. *					Ports	Output Por	rts
1		-	AMD Processor								_
2		1	packages/tx_an		a s12n			range(	17)	range(7,13)	
3	H	-				ard		range(	-11	runge(7,15)	
4		Processor pin-escape and Motherboard     1 pinescape-via/12layer_pinescape_top2l10.s12p						range(	1.7)	range(7,13)	
5         ✓         1         sline/typloss/sli           6         ✓         0         sline/typloss/sli           7         ✓         1         ccap-via/12laye				ine3p_1.0oz_4_6_4_20_100ohm_typ_13in.s12p				range(		range(7,13)	
				ine3p_1.0oz_4_6_4_20_100ohm_typ_0.1in.s12p				range(	2012220	range(7,13)	
				er_accap_top2l3.s12p				range(	16	range(1,7)	
				_1.5oz_s5_100ohm_typ_0.40inch.s12p				range(1,7)	range(7,13)		
9	-	1						7,13)	range(1,7)		
1						ш					•
Jnit	inter	rval	in secs	125e-12	# Time	in secs					
Tota	l nu	mbe	er of channels	3							
					Ru	n				Sto	эp
			t_res=50								
	Setting: adapt_pole=[2e9]  # CTLE fixed pole location Setting: jit seconds=True										
	Setting: jit_pwddj=10e-12  # PWJ pk-pk dual-dirac jitter (2*jit_hfddj)										
			weep_yvars={'c	h_idle_ex	it':172,'ew':(	0.35,'eh':34}					
			t_eye=True _zero=0.0								
Set	ting:	isi_	xtalk_ratio=4	#	Ratio vpt to r	max ISI and Xtalk	magnituc	le (divis	ible by	2 or 1)	
			oeff=[0]								
			apt_DE=[]								

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Seasim Port Definitions

- Touchstone tuple port definitions
  - Reflects the S-parameter models intrapair net order
  - Provides pair-to-pair (victim/aggressor) relationship for crosstalk inclusion
- Transmitter ports
  - Allows renormalization of port impedance by providing a list of terminal impedance values
  - Define transmitter pad differential voltage amplitude
  - Transmitter bandwidth defined by Gaussian filter setting
- Receiver port
  - Provide custom port renormalization impedance

ile Ir	nclude								
1ain	S-Parameters	Jitter/Noise	Equalizers	Step Responses Configuration Sweep					
para	neter normalized	l Rx port for s	steps	(9,10)	# D	ifferential Rx p	ort		
para	meter normalized	I Tx ports for	steps	(3,4),(1,2),(5,6) # Differential Tx ports					
e-nori	malize port imped	dance ohms		50					
x peal	k-peak voltage int	to port imped	ance	0.8	# S-	parameter Tx p	ok-pk voltage	2	
x Gau	ssian bandwidth			8e9	8e9 # S-parameter Gaussian bandwidth				
	teps from touchs oncatenated touc	55356 L 1695/1935		e					
DR ste	ep bandwidth			10e9					
DR tin	ne window			1e-9					



## **Seasim Jitter Configuration**

#### Jitter

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- Consistent jitter definitions with the PCIe base spec
- Default jitter settings can be loaded with the default configuration file
- Jitter values can also be customized using the field in the GUI and saved

#### Noise

 Random low frequency noise can be defined in addition to the aggressorvictim coupling present in the Touchstone file

File Include					
Main S-Parameters Jitter/Noise	Equalizers	Step Responses	Configuration	Sweep	
Jse seconds for Jitter	$\checkmark$				
Pulse Width Random jitter	1e-12	# PWJ RJ (1.414	1*jit_hfrj)		
Pulse Width Dual-Dirac jitter	10e-12	# PWJ pk-pk du	al-dirac jitter (2	*jit_hfddj)	
Edge RJ Nui earlier than cursor	1.375e-12 # nui-cycle RJ				
.F Random jitter	1.55e-12 # Gaussian sigma post channel jitter				
.F Dual-Dirac jitter	7e-12 # dual-dirac post channel jitter				
F Uniformly distributed jitter	0.0				
F Random Voltage noise	0.0				
.F Uniformly distributed Voltage noise	0.0				



#### SIG **Seasim Equalization**

- Tx FIR Filter
  - Can either fix pre-shoot and deemphasis or set coefficient search space for adaptation
- **Rx** Linear Equalizer
  - Define pole/zero value or range of  $\checkmark$ values for adaptation
  - May cascade multiple continuous time LEQ filters
- **Decision Fed Equalizer** 
  - Can enable multiple DFE taps beyond defaults
  - Can vary dynamic range of taps independently

	o (root_dir: C:\Introduction_To_SeaSim\PCIE3)						
File Include							
Main S-Parameters Jitter/Noise Equali	Zers Step Responses Configuration Sweep						
Adaptation FOM	area 👻						
Include xtalk during adaptation							
Tx pre-shoot search space (priority) (dB)							
Tx de-emphasis search space (priority) (dB)	0						
Tx coefficient search space	24 # Coefficent space size						
LEQ1 DC gain search space (dB)	range(-12,-5) # DC gain of CTLE in dB						
LEQ1 pole search space (Hz)	[2e9] # CTLE fixed pole location						
LEQ2 DC gain search space (dB)	[0]						
LEQ2 pole search space (Hz)	[0]						
Max Tx EQ boost (dB)	8.0 # Maximum Tx EQ boost in dB for Cspace search						
DFE taps and max magnitude (V)	[0.030] # Number and dynamic range of DFE taps						
If no adaptation EQ can be explicitly set below	N						
Tx pre-shoot (priority) (dB)	0.0						
Tx de-emphasis (priority) (dB)	0.0						
Tx EQ FIR coefficients	[1]						
LEQ1 DC gain (dB)	0.0						
LEQ1 pole (Hz)	0.0						
LEQ1 zero (Hz) (provides gain if not 0)	0.0						
LEQ2 DC gain (dB)	0.0						
LEQ2 pole (Hz)	0.0						
LEQ2 zero (Hz) (provides gain if not 0)	0.0						
Rx bandwidth (Hz) (1st pole)	8e9 # HF roll-off of equalizer						
Rx bandwidth (Hz) (2nd pole)	0.0						
LEQ response cPickle file of pole/gain/Hz							
DFE tap values (V)	[0]						



## **Seasim Step Responses**

#### Channel Step Response

- Alternative simulation method to providing channel S-parameter models
- Measured or simulated voltage-time records of channel step responses can be used directly for statistical simulation

#### Crosstalk

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- Independent waveforms can be supplied for the inclusion of aggressor coupling to the victim receiver
- Can optionally offset the aggressorto-victim alignment

File Ir	nclude							
Main	S-Parameters	Jitter/Noise	Equalizers	Step Responses	Configuration	Sweep		
List of a	aggressor delays	in UI	[]					
Auto ag	ggressor alignme	nt	cente	er 🔹				
Aggr bi	t mask, 0=center	, 1=edge, -1	=OFF []					
Differer	ntial aggressor nu	umbers		0				
Victim r	rise step template	e	%s_\	%s_vict.rfstep1				
Aggres	sor rise step tem	plate	%s_ā	%s_aggr%d.rfstep1 🔹				
Victim f	fall step template		%s_\	%s_vict.rfstep0 👻				
Aggressor fall step template				%s_aggr%d.rfstep0 -				
Dictiona	ary of step names	5	0	0				
Write fo	domain insertion	loss	<b>_</b>					

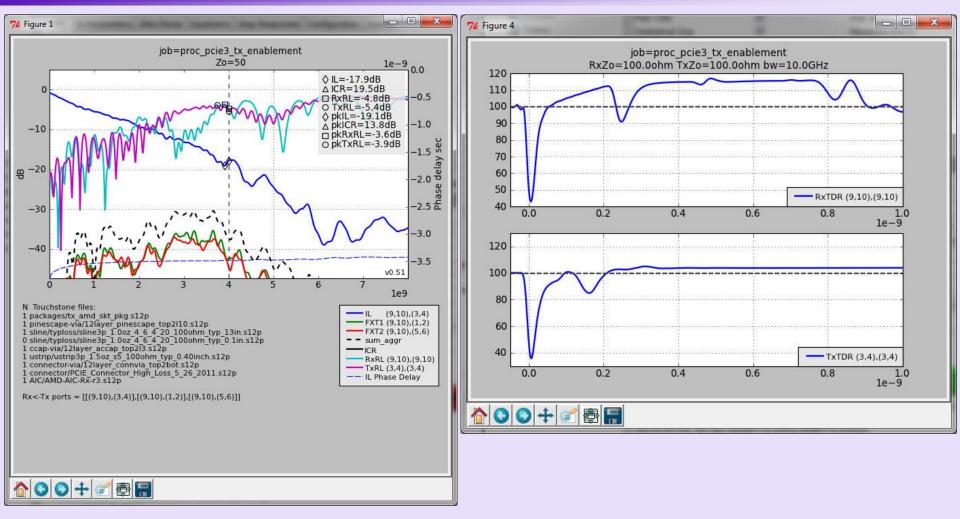




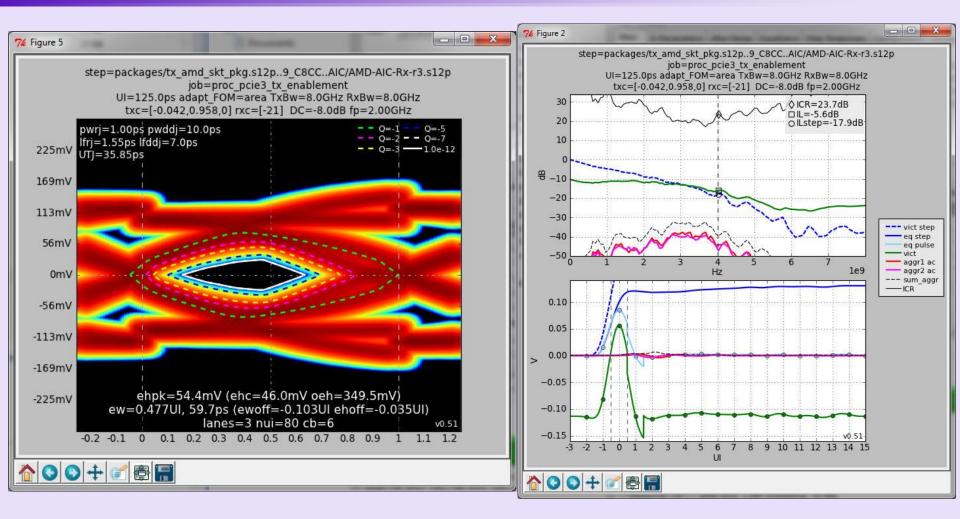
- Seasim can be used to define HVM sweeps
- The channel model can be swept to represent manufacturing variations of impedance or loss
- To consider the impact of different PCB layout the length of different channel segments can be swept
- Seasim will launch jobs in parallel then collect results and plot them

File	Inc	lude															
Mai	n	S-Parameters	Jitter/Nois	e Equ	alizers	Step Res	onses	Co	onfig	urati	on	Swee	p				
-	# SG tol			n	00	01	02	03	03 04	05	06	07	08	09	10	11	-
1		Motherboard														_	١.
2		1	tstone_po	ts.T.5	13in	14in	15in					-					1
3	-	2	tstone_po			1	2	3	4	5	6	7	8	9	_		
4		3	tstone_ports,T,5		Contract and the second	75ohm			1.22	181		2	10	-			ſ
5	-	3	tstone_ports,T,6						1								Ē
6																	
7																	
8																	
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1		1		1	1	1										+	
we	en h	ase name	1	oroc tx	sweep												
on	curre	ent sims, jobs p	ier sim	4,1													
Run sweep jobs run_seasim																	
Kil	l run	ning jobs															
_																	
Cr	eck	job status															
ist	of SI	weep Groups fo	r x axis	0													
Dicti	onar	y of "variable":	limit	{'ch_idle_exit':172,'ew':0.35,'eh':34}													
		•	Constants														
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	0.00.0000	ep text for plot	labels														
Plo	ot sw	eep results															
De	lete	logs															
Fire	+ 5	nfinished jobs:	8														1
		_sweep_new_0															ľ
		sweep_new_0															
Fini	shed	jobs 28/30															
Sub	mitte	ed 30 sims of 1	jobs 30 jol	os com	pleted												
Plot	ting.																
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F111	sneu	poung															ι,

### Seasim Channel Simulation Frequency Response & Bidir TDR

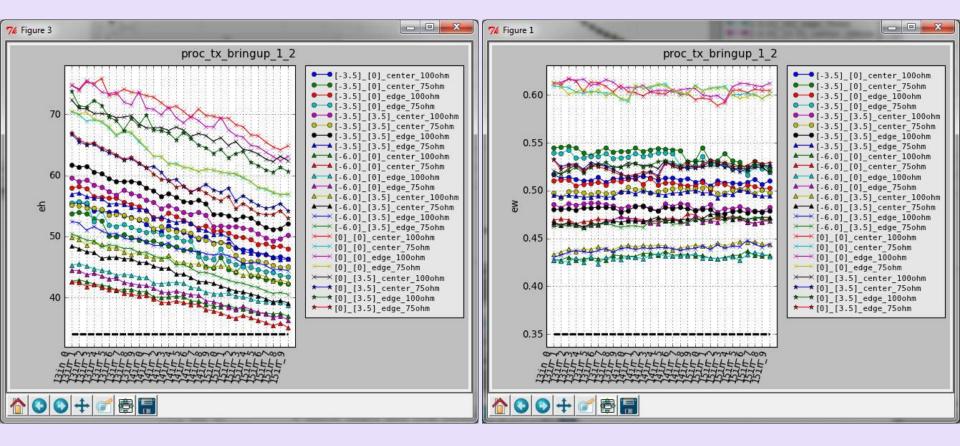


### Seasim Output Eye & Equalized Freq & Time Response



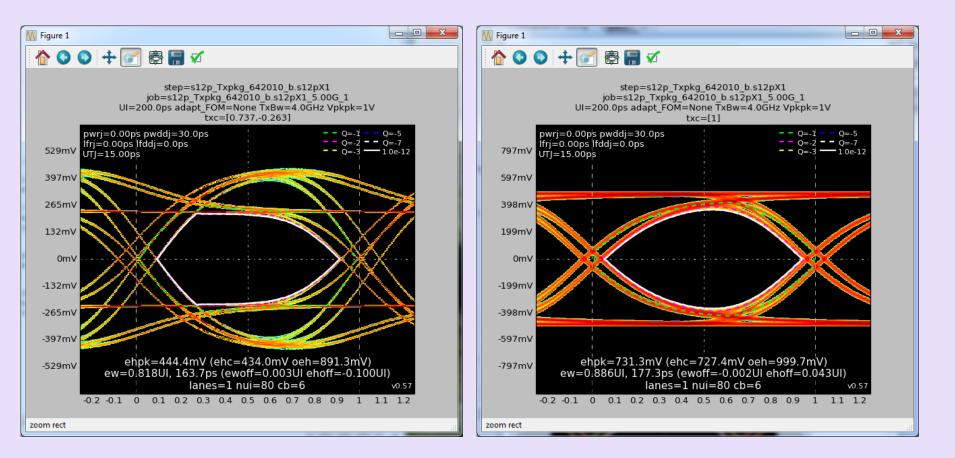


#### Seasim Sweep Results Analysis Plots

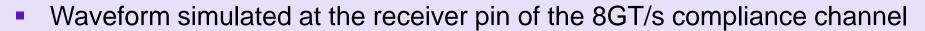


# Seasim Legacy Data Rate Simulation Setup

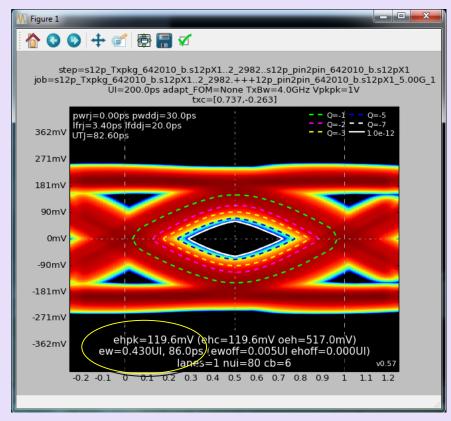
 PCIe 2.x simulation requires calibrating the transmitter De-emphasis and signal amplitude at the package pin (i.e. -6dB/0.8V/0.9UI)



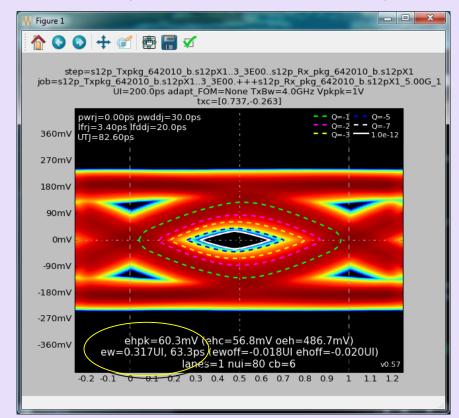
# Seasim Legacy Data Rate Simulation Setup



Simulated at the receiver pin of the 8GT/s compliance channel. PCIe 2.x min is 120mV/0.4UI.

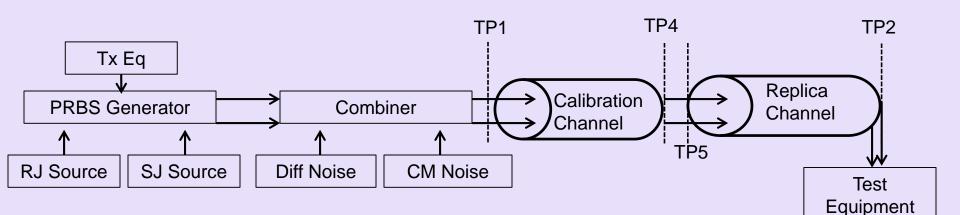


Simulated at the receiver pad using the 8GT/s spec Tx pkg + spec channel + spec Rx pkg.



#### Seasim Rx Tolerance Calibration





Eye distortions are calibrated independently to mitigate the noise floor of the test equipment.

Post process

Pkg mod

CTLE/DFE Behave CDR

TP2P

Three Phases to Calibration

- Channel ISI and behavioral Rx EQ
  - ✓ Calibrate loss from TP1 to TP2
    - Fine adjustment with generator equalization
  - ✓ Use base spec PDA search for CTLE and DFE settings
    - Constrained to be no better than what's used in channel compliance
- Phase jitter, differential voltage noise and common-mode noise
  - ✓ Use Seasim to calculate required RJ & VN
  - ✓ Set and measure RJ & SJ at TP1
    - Assumes jitter amplification in channel is negligible
  - ✓ Set and measure VN & CMN at TP2
    - VN de-embedded from ideal Rx-latch back to TP2
- Cumulative eye measurement
  - $\checkmark$  All distortions applied, extrapolate and interpolate to  $10^{-12}$  &  $10^{-6}$

VNA Measurement TP1 to TP2

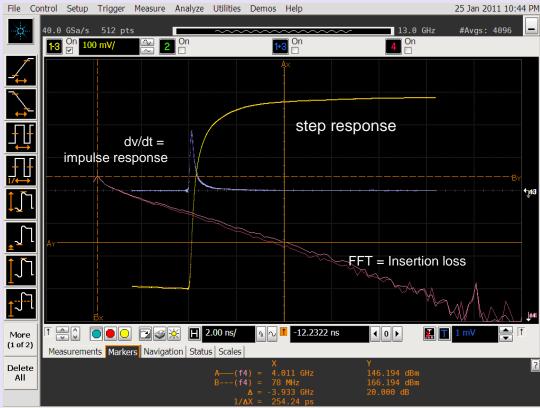


Needs to include all cables used for measurement.



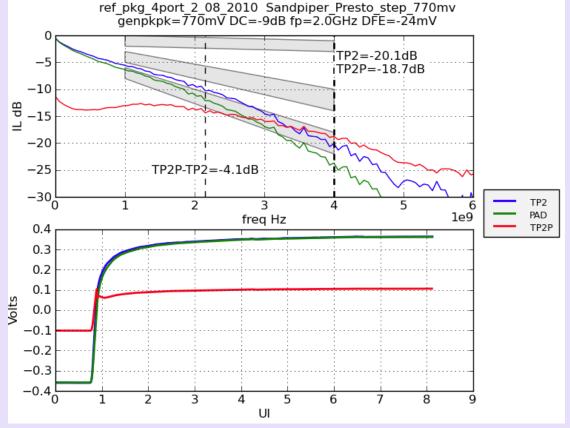
## Step Response

- Scope averaged and interpolated step response at TP2
- 128 UI 1/0 clock waveform
- 1ps time steps

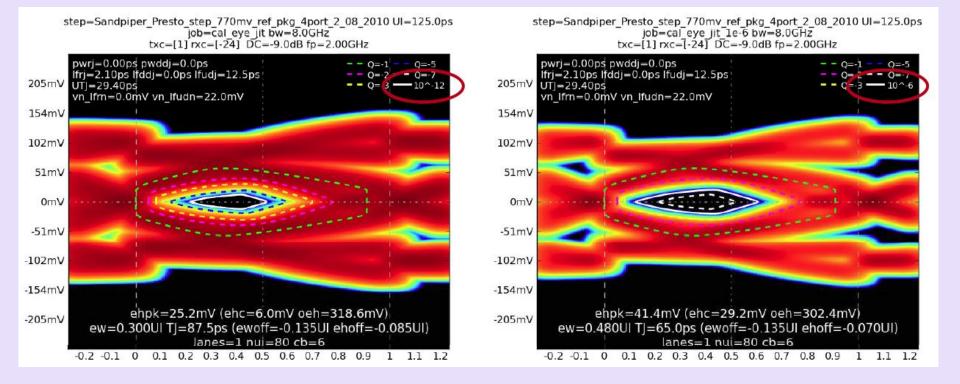




- Pad waveform is TP1 channel extended by behavioral package to Rx die pad
- Difference between TP2P and TP2 (-4.1dB) at 2.1GHz used to de-embed VN to TP1







\*May need to iteratively tune generator amplitude and VN to get EW > 0.3UI and EH = 25mV

PCIe Technology Seminar





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### **Derivation of Coefficients**

$$t_{0} + t_{1} + t_{2} = 1; \quad t_{1} = 1 - t_{0} - t_{2}$$

$$DE = \frac{V_{PK}(-t_{0} + t_{1} - t_{2})}{V_{PK}(-t_{0} + t_{1} + t_{2})} = \frac{1 - 2t_{0} - 2t_{2}}{1 - 2t_{0}}$$

$$PS = \frac{V_{PK}(+t_{0} + t_{1} - t_{2})}{V_{PK}(-t_{0} + t_{1} - t_{2})} = \frac{1 - 2t_{2}}{1 - 2t_{0} - 2t_{2}}$$

$$DE \cdot PS = \frac{1 - 2t_{2}}{1 - 2t_{0}}$$

$$2t_{2} = 1 - DE \cdot PS(1 - 2t_{0})$$

$$DE = \frac{1 - 2t_{0} - 1 + DE \cdot PS(1 - 2t_{0})}{1 - 2t_{0}} = \frac{-2t_{0}}{1 - 2t_{0}} + DE \cdot PS$$

$$2t_{0} = (DE \cdot PS - DE)(1 - 2t_{0})$$

$$2t_{0} = DE \cdot PS - DE + 2t_{0}DE - 2t_{0}DE \cdot PS$$

$$2t_{0}(1 - DE + DE \cdot PS) = DE \cdot PS - DE$$

$$2t_{0} = \frac{DE \cdot PS - DE}{1 + DE \cdot PS - DE}$$

$$t_{0} = \frac{DE(PS - 1)}{2 + 2DE(PS - 1)}$$

 $DE = \frac{Vb}{Va}; PS = \frac{Vc}{Vb}$ 

$$2t_{2} = 1 - DE \cdot PS (1 - 2t_{0})$$

$$2t_{2} = 1 - DE \cdot PS + 2DE \cdot PSt_{0}$$

$$2t_{2} = 1 - DE \cdot PS + DE \cdot PS \frac{DE(PS - 1)}{1 + DE(PS - 1)}$$

$$2t_{2} = \frac{(1 + DE(PS - 1))(1 - DE \cdot PS) + DE^{2} \cdot PS(PS - 1)}{1 + DE(PS - 1)}$$

$$2t_{2} = \frac{1 - DE \cdot PS + DE(PS - 1) - DE^{2} \cdot PS(PS - 1) + DE^{2} \cdot PS(PS - 1)}{1 + DE(PS - 1)}$$

$$2t_{2} = \frac{1 - DE \cdot PS + DE \cdot PS - DE}{1 + DE(PS - 1)}$$

$$t_{2} = \frac{1 - DE}{2 + 2DE(PS - 1)}$$

**Tx FIR Coefficients** 

PS		0			1			2			3		4			
DE	c0	c1	c2	c0	c1	c2	c0	c1	c2	c0	c1	c2	c0	c1	c2	
0	0.000	1.000	0.000	-0.054	0.946	0.000	-0.103	0.897	0.000	-0.146	0.854	0.000	-0.185	0.815	0.000	
-1	0.000	0.946	-0.054	-0.049	0.902	-0.049	-0.094	0.862	-0.044	-0.134	0.826	-0.040	-0.171	0.793	-0.036	
-2	0.000	0.897	-0.103	-0.044	0.862	-0.094	-0.085	0.829	-0.085	-0.123	0.799	-0.077	-0.159	0.771	-0.070	
-3	0.000	0.854	-0.146	-0.040	0.826	-0.134	-0.077	0.799	-0.123	-0.113	0.774	-0.113	-0.146	0.750	-0.103	
-4	0.000	0.815	-0.185	-0.036	0.793	-0.171	-0.070	0.771	-0.159	-0.103	0.750	-0.146	-0.135	0.730	-0.135	
-5	0.000	0.781	-0.219	-0.032	0.763	-0.205	-0.064	0.745	-0.191	-0.094	0.728	-0.178	-0.124	0.712	-0.165	
-6	0.000	0.751	-0.249	-0.029	0.736	-0.235	-0.057	0.722	-0.221	-0.086	0.708	-0.207	-0.113	0.694	-0.193	
-7	0.000	0.723	-0.277	-0.026	0.712	-0.262	-0.052	0.700	-0.248	-0.078	0.689	-0.234	-0.104	0.677	-0.219	
-8	0.000	0.699	-0.301	-0.023	0.690	-0.287	-0.047	0.680	-0.273	-0.071	0.671	-0.258	-0.094	0.661	-0.244	
-9	0.000	0.677	-0.323	-0.021	0.670	-0.309	-0.042	0.662	-0.295	-0.064	0.655	-0.281	-0.086	0.647	-0.267	
-10	0.000	0.658	-0.342	-0.019	0.652	-0.329	-0.038	0.646	-0.316	-0.058	0.640	-0.302	-0.078	0.633	-0.289	