PCI Express® Electrical Basics

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Topics

- PCI Express® Overview
- Enhancements for 8GT/s
- Target channels for the specification
- Electrical signaling
- Transmitter
- Receiver
- SEASIM

Electrical Features

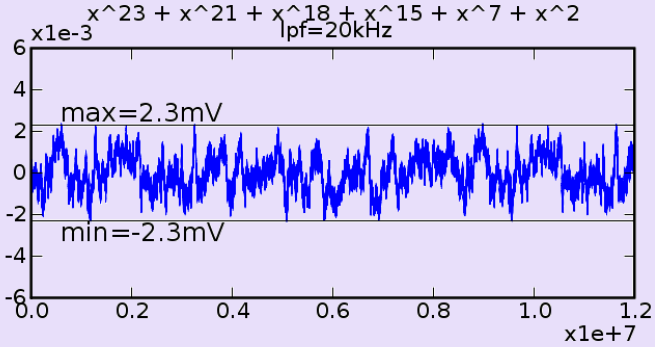
- Data rates 2.5GT/s, 5GT/s and 8GT/s
- 10^{-12} bit error ratio
- AC coupled
- Link widths 1, 2, 4, 8, 16, 32 lanes
- Hot swap capable
- 2.5 and 5GT/s scrambled + 8b10b
- 8GT/s scrambled + 128/130
- Power management

Doubling from 5GT/s

- Major goal was to make PCIe® 3.0 evolutionary
  - ✓ Support existing usage models
  - ✓ Preserve Common Reference Clock and Data Clocked modes
  - ✓ Re-use of 5GT/s reference clock generators
  - ✓ Re-use of silicon PHY architectures
- Evaluated channels at 10GT/s and 8GT/s
  - ✓ 10GT/s would have allowed 8b10b coding to be preserved
- Shown that a non-linear increase in difficulty to reach 10GT/s
  - ✓ Increased channel improvement cost
  - ✓ Increased power in silicon
  - ✓ Increased difficulty for eco-system
- Concluded the cost of changing encoding acceptable
  - ✓ A new scrambled encoding scheme was developed
  - ✓ Efficiency 20% better than 8b10b

8GT/s Enablers

- Receiver equalization required
- Introduce statistical channel analysis
  - ✓ Channel compliance & simulation with behavioral Tx/Rx
- Mitigate baseline wander & crosstalk
  - ✓ Polynomial choice of 128/130 code on individual lanes
  - ✓ Baseline wander:



  - ✓ LFSR offsets between adjacent lanes reduces simultaneous switching

Red: vict+2aggr; pink: vict+1aggr; black: vict only

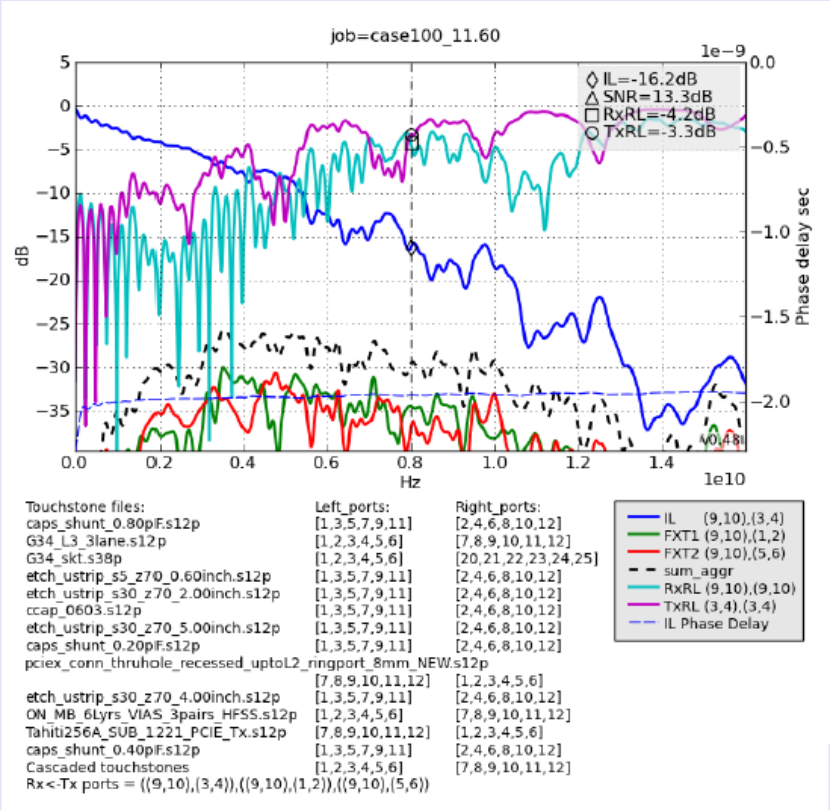
Target Channels

PCI Express Channels

- Channel specification
  - ✓ No formal spec for 2.5 and 5GT/s
    - Channel budget implied
  - ✓ 8GT/s introduces time domain spec
  - ✓ Card Electromechanical (CEM) spec sets limits and measurement points
- Two worst case models assumed
  - ✓ Client CEM
    - Short to medium length (3-12”), reflection and crosstalk dominated
  - ✓ Server CEM
    - Medium to long (20”) loss dominated

Client Channel

Typical Client Topology

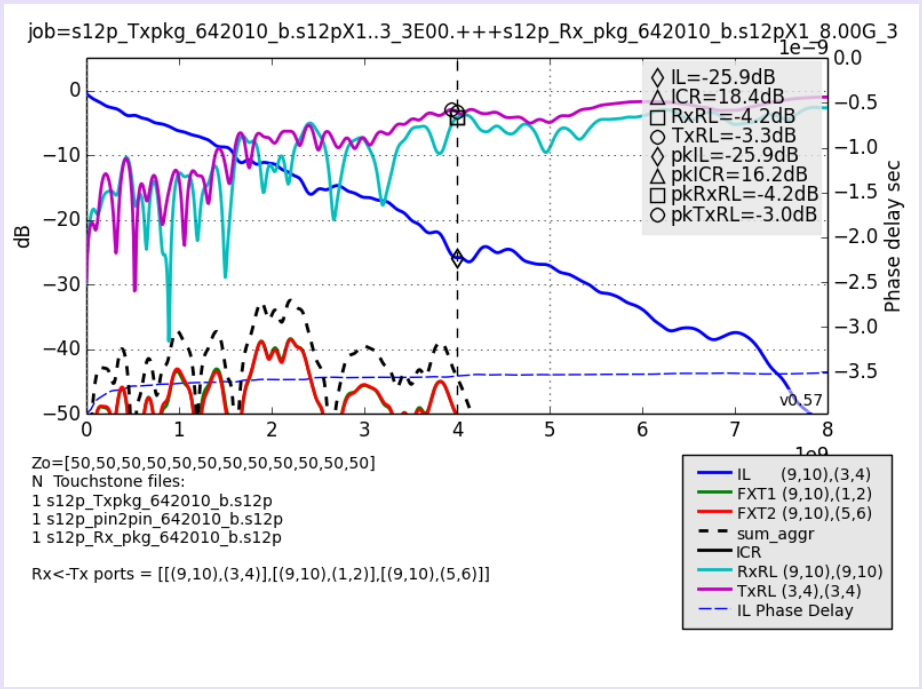


Add in card 3-4”

4-layer microstrip 3-7” with PTH via stubs

Server Channel

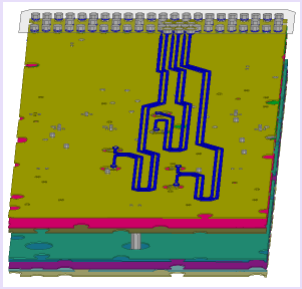
Typical Server Topology



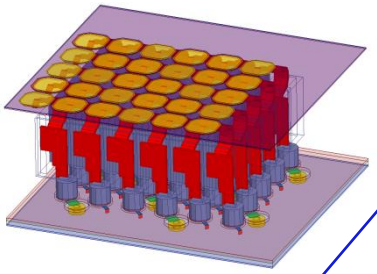
6- 8 layers, 20”, 1 or 2 connectors
Stripline with via stubs

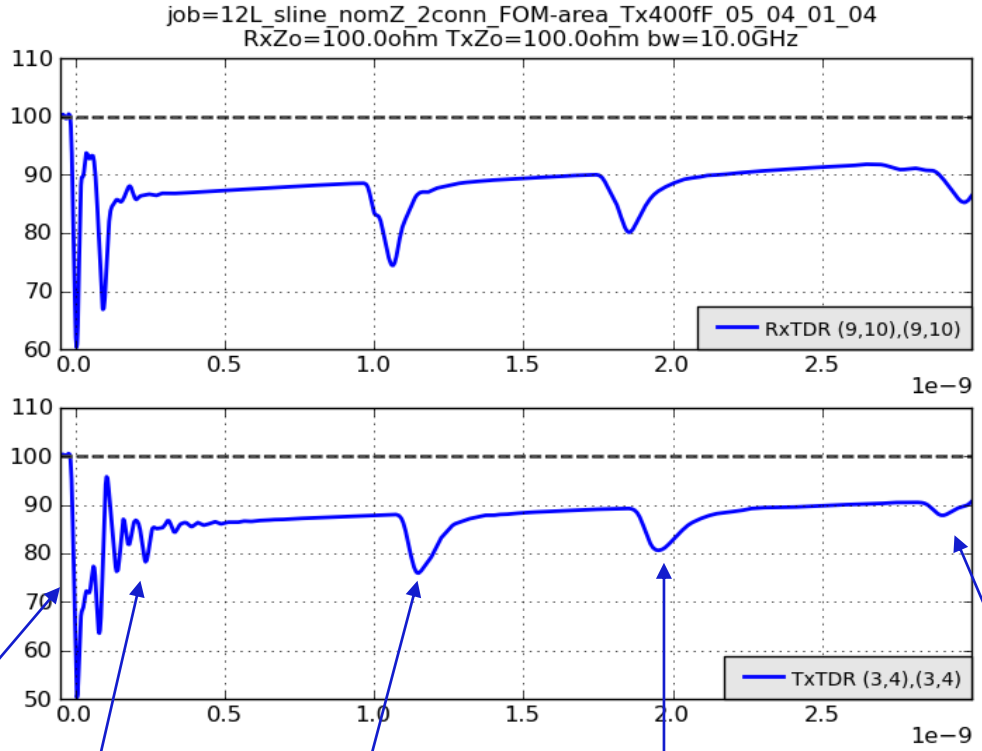
Bidir TDR of 2-Connector Server Channel

FCLGA Package

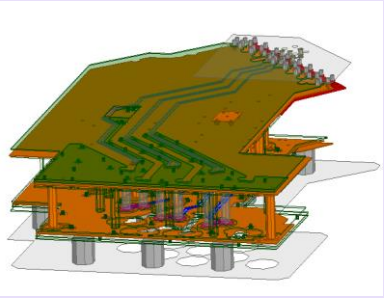


LGA Socket



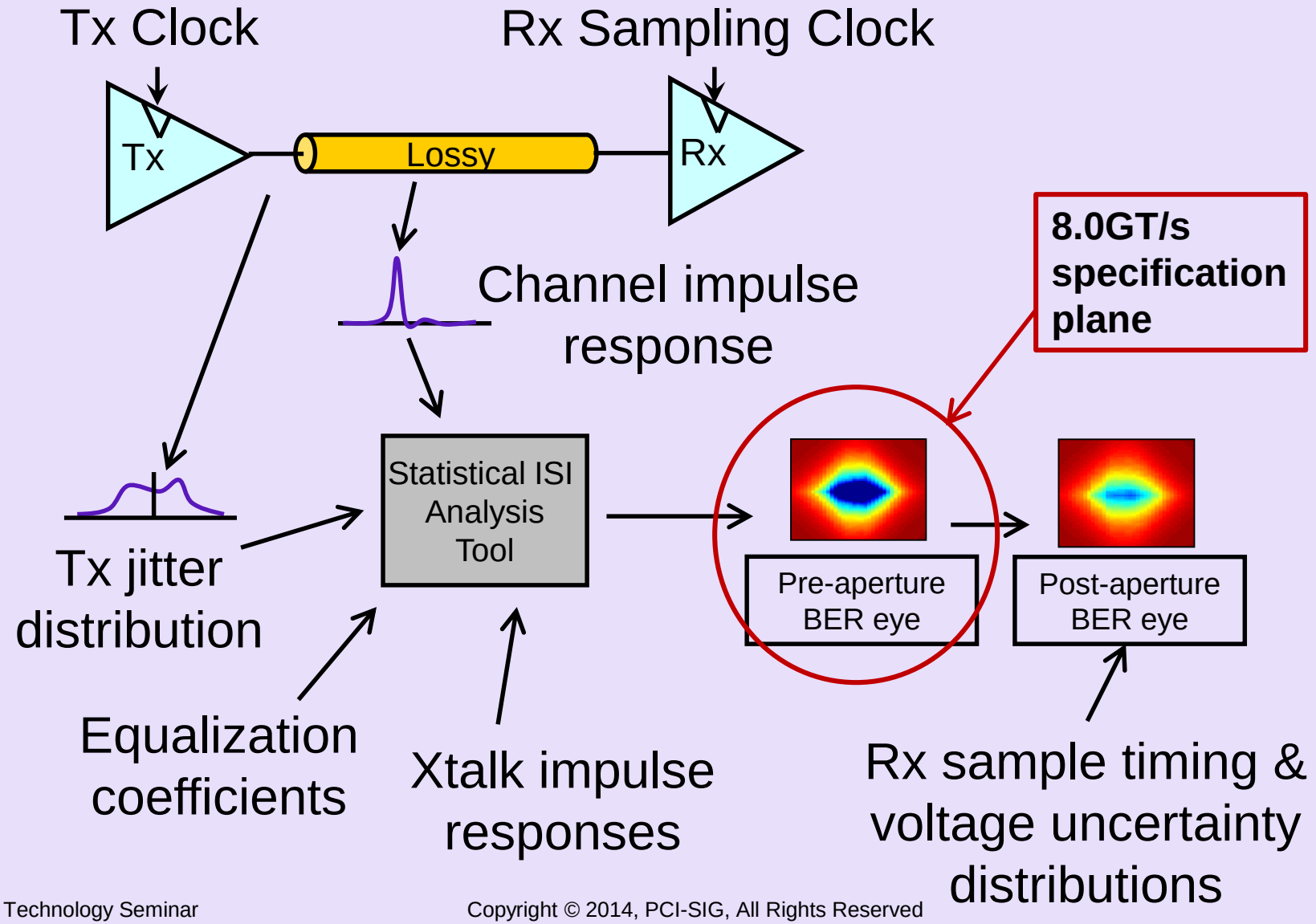


BGA Package



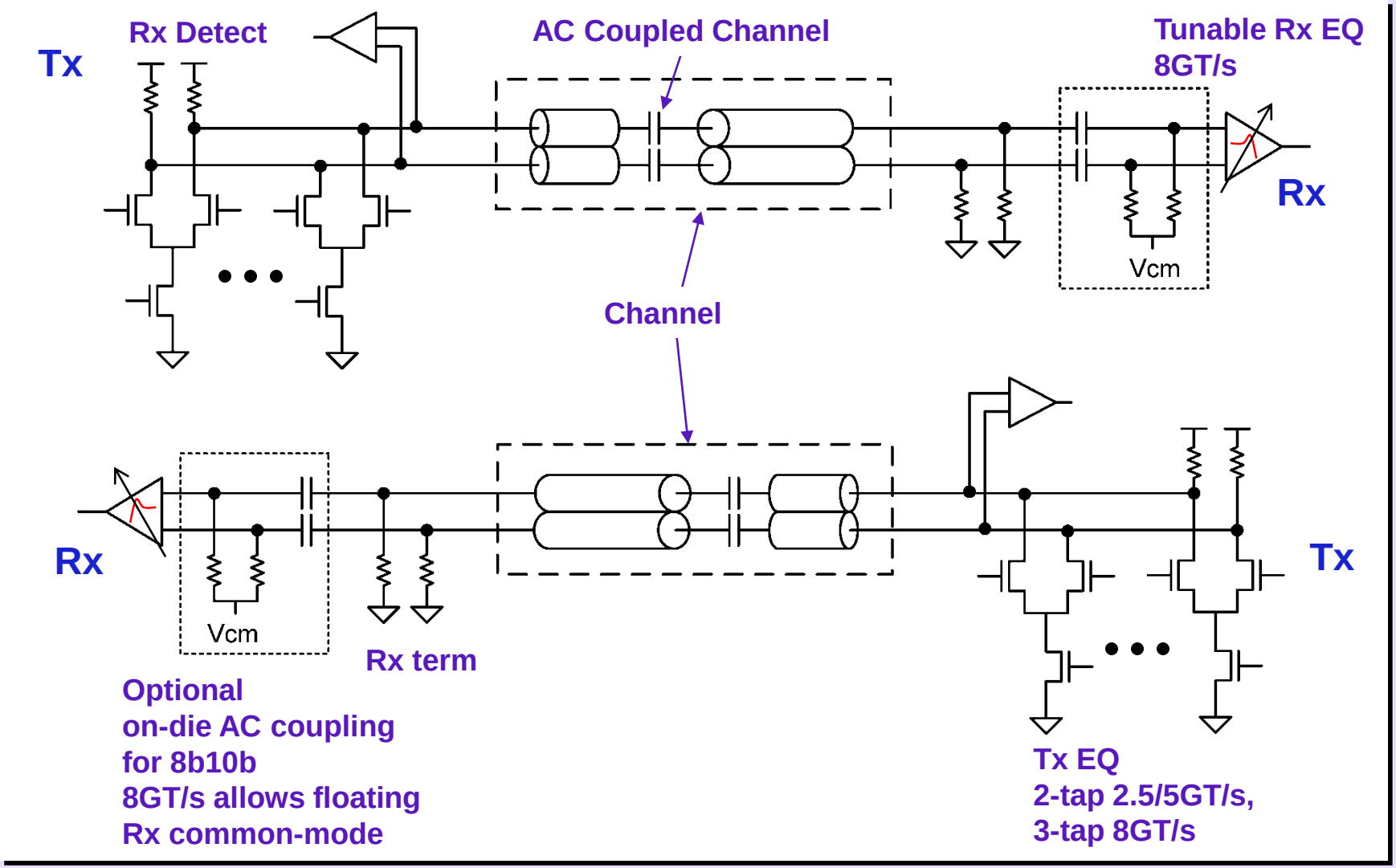
Connector transitions clearly visible in TDR data

8.0GT/s Statistical Channel Analysis

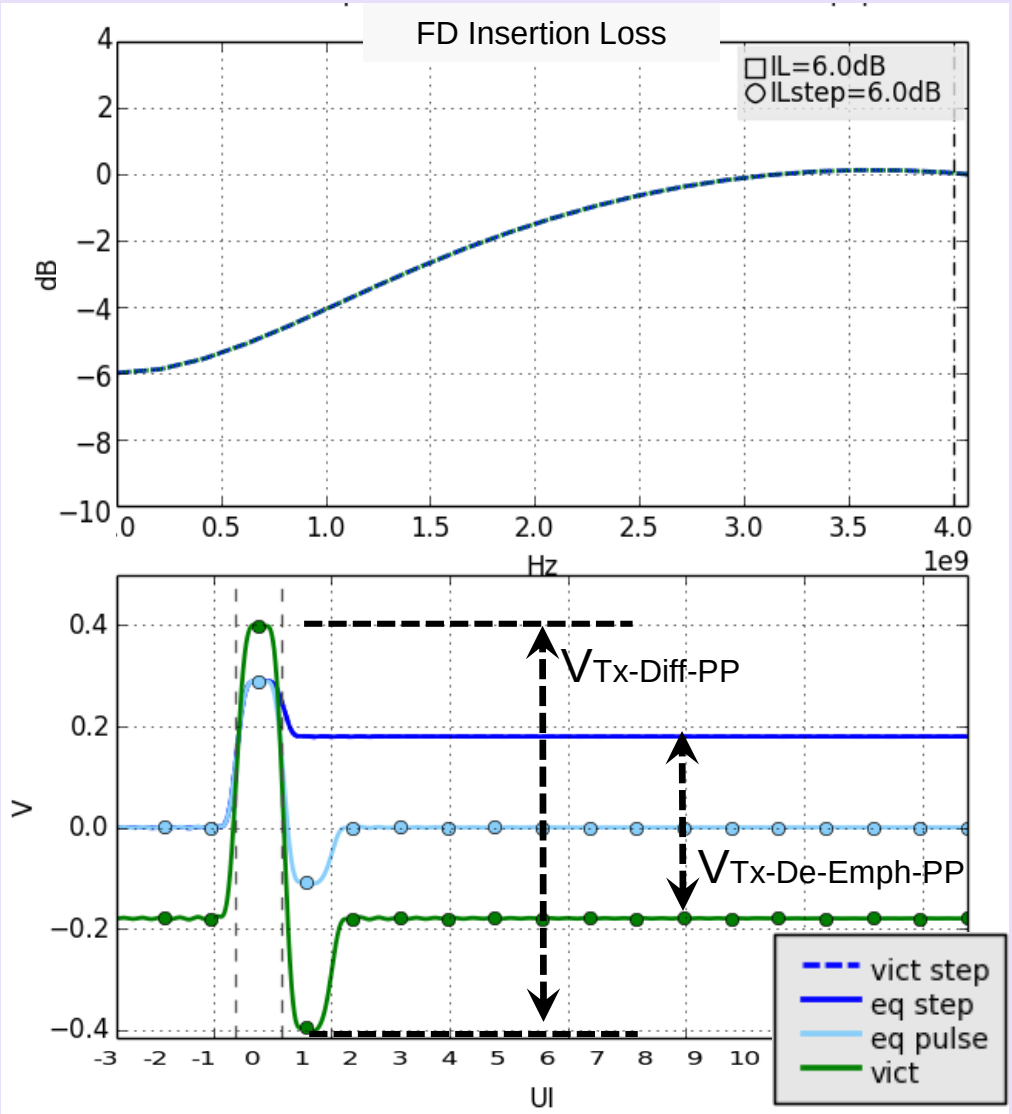


Electrical Signaling

Transceiver and Channel



Transmit De-Emphasis

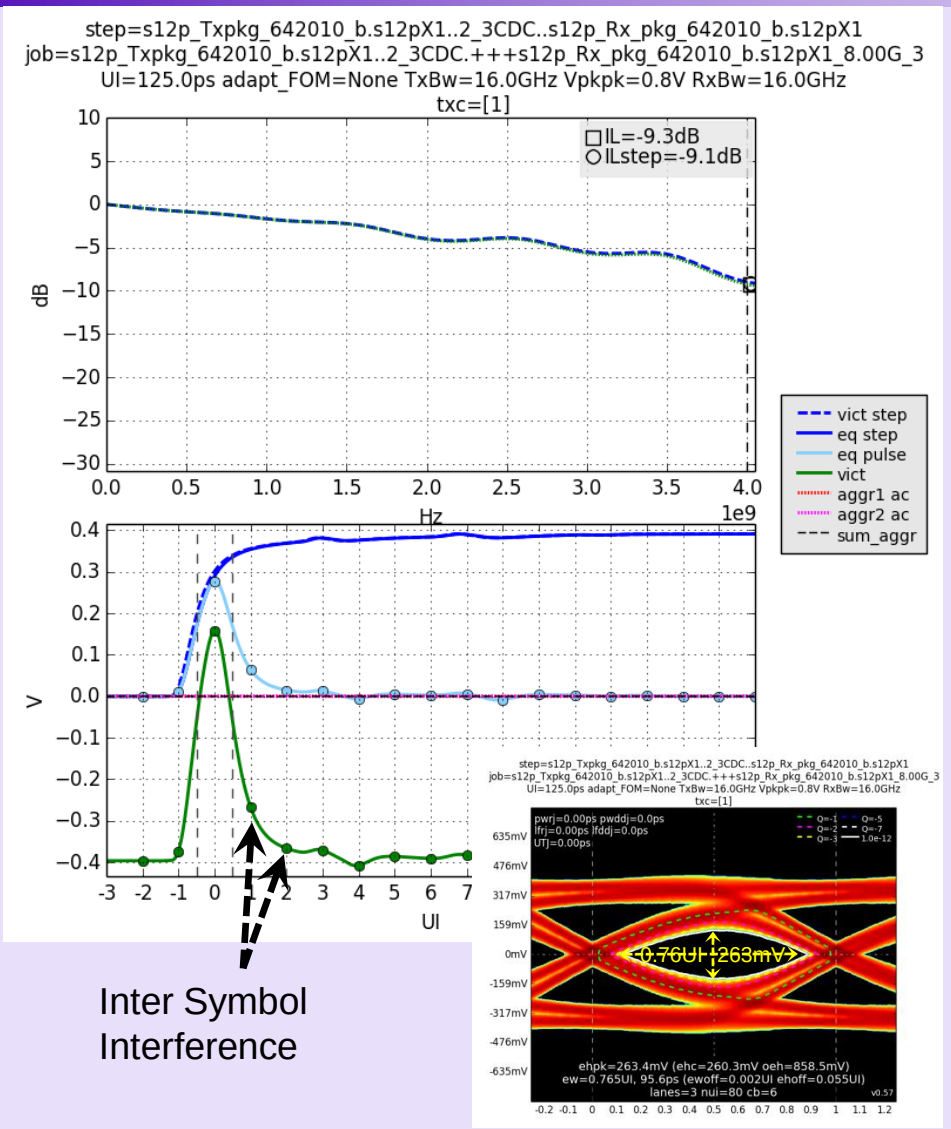


Transmitter circuits use De-Emphasis to equalize the frequency response of the channel in order to minimize inter-symbol interference

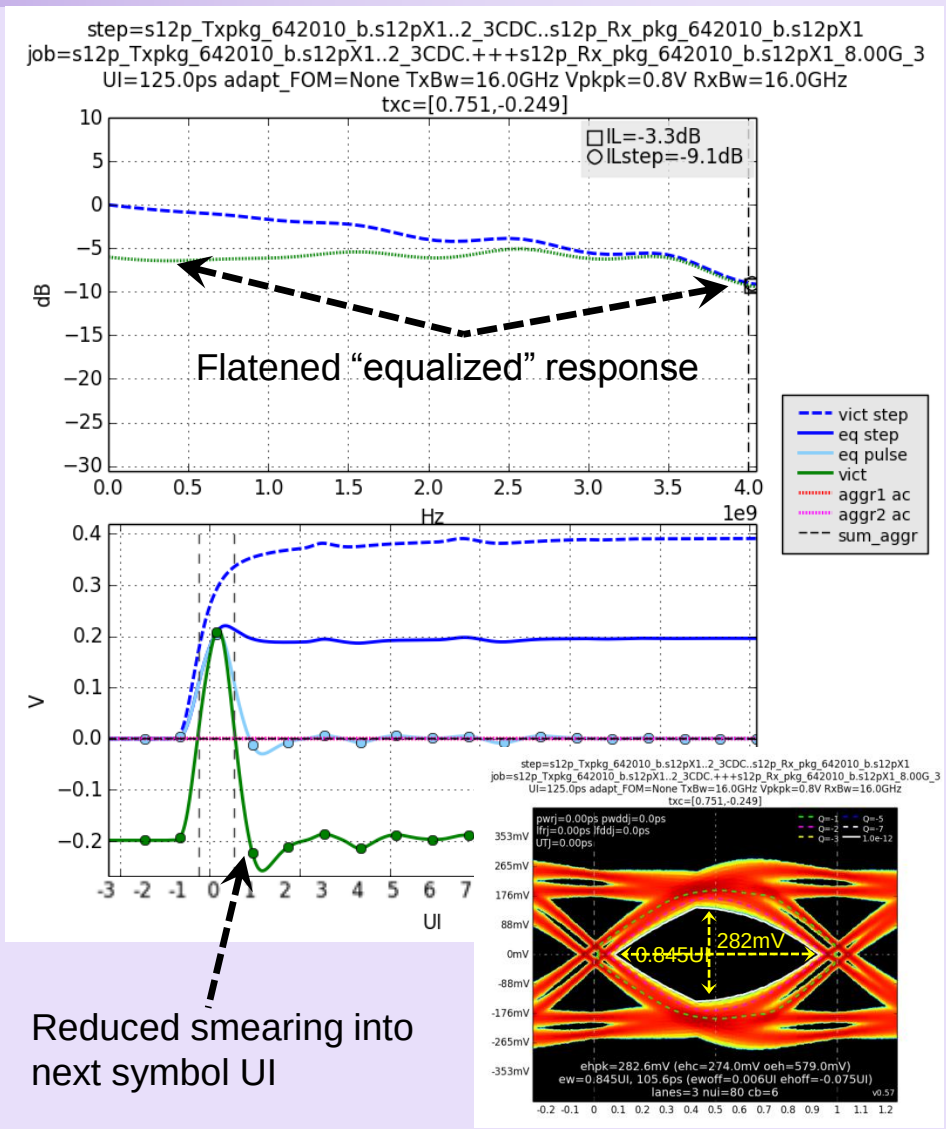
Available Equalization Settings:

2.5GT/s: [-3.5dB]
5.0GT/s: [-3.5dB, -6dB]
8.0GT/s: [-3.5dB, -6dB, pre-cursor]
* 10-presets
* coefficient tuning space

De-Emphasis Pulse & Frequency Domain Response



Inter Symbol Interference



Reduced smearing into next symbol UI

Tx FIR EQ Definitions

$$V_{TX} = V_{PK} \sum_{n=0}^{k} c_n d_{m-n} \text{ and } \sum_{n=0}^{k} |c_n| = 1$$

V_{TX} is output voltage and V_{PK} the peak voltage

k is number of Tx coefficients

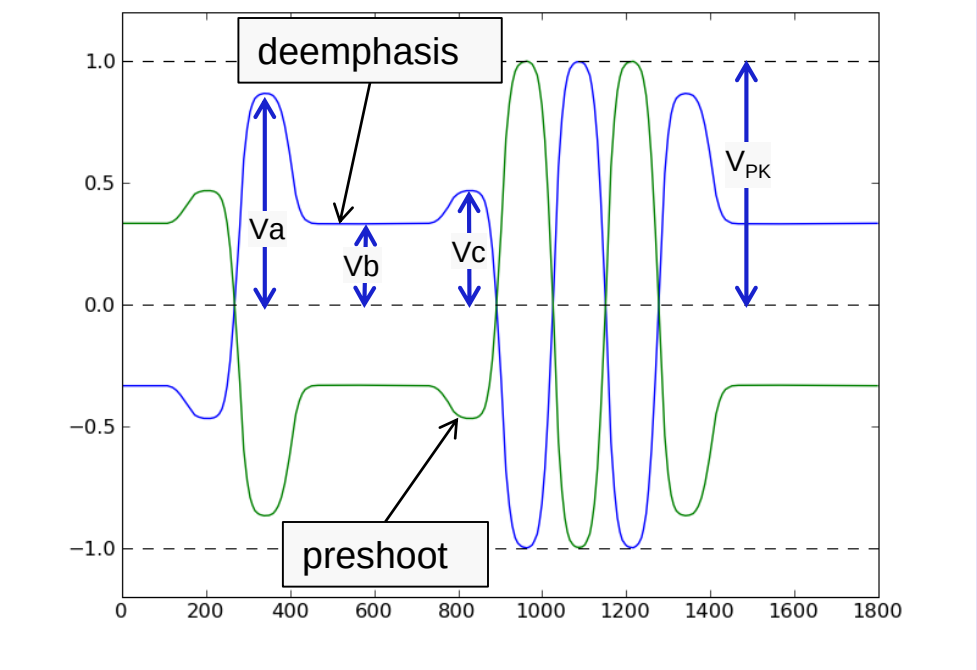
d is vector of +1 and -1 for logic 1 and 0

m is the index into the bit stream

For a 3 tap Gen3 FIR c_1 is positive and

c_0 and c_2 are negative

data is delayed by 1UI



For data stream 00010111

$V_{PK} = 1$ and $t_0 = -c_0; \quad t_1 = c_1; \quad t_2 = -c_2$

$000 \rightarrow +t_0 - t_1 + t_2$

$001 \rightarrow -t_0 - t_1 + t_2$

$011 \rightarrow -t_0 + t_1 + t_2 \rightarrow Va$

$111 \rightarrow -t_0 + t_1 - t_2 \rightarrow Vb$

$110 \rightarrow +t_0 + t_1 - t_2 \rightarrow Vc$

$$deemphasis = 20\log_{10}\frac{Vb}{Va}$$

$$preshoot = 20\log_{10}\frac{Vc}{Vb}$$

Fully specified by
$V_{TX\text{-}DE\text{-}RATIO}$ (0 to -8dB)
$V_{TX\text{-}PS\text{-}RATIO}$ (0 to +3dB)

Transmitter

Transmitter Reference Plane

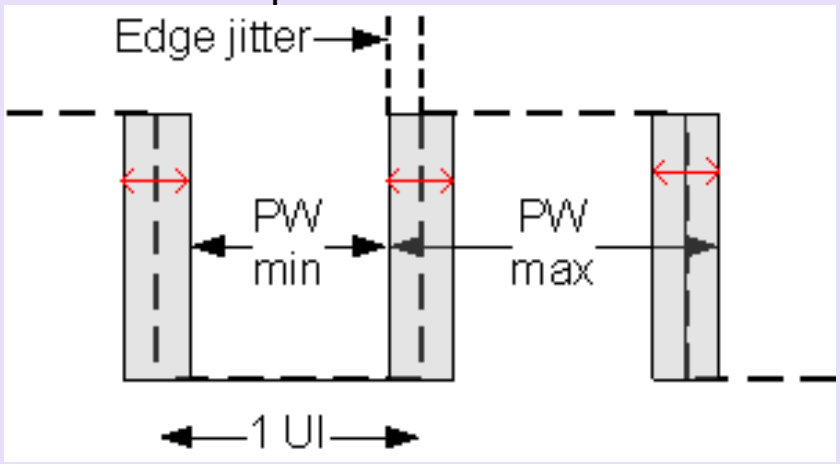
- Reference plane is DUT pin
  - ✓ Most convenient manufacturing boundary
- For 2.5 and 5GT/s
  - ✓ Package losses are part of Tx performance
- For 8GT/s die pad, package route and package pin interactions are more significant
  - ✓ Makes fixture de-embedding inaccurate
  - ✓ Tx EQ and jitter measurements inaccurate
- Use data-dependent jitter separation
  - ✓ Effectively measure Tx jitter at die pad
  - ✓ Use LF measurement technique for presets at pin

Transmitter

- Differential ~100ohm transmitter
  - ✓ FS: 800-1200mV, HS: 400-800mV
  - ✓ 0.75UI eye opening
- 2.5/5GT/s 2-tap EQ
  - ✓ FS: -3.5dB and -6dB, HS: 0dB
- 8GT/s 3-tap EQ
  - ✓ 10 presets, min boost 8dB, coefficient tuning space
- AC coupled channel series capacitor
  - ✓ 2.5/5GT/s 75-265nF
  - ✓ 2.5/5/8GT/s (Rev 3.0) 176-265nF
- Return Loss
  - ✓ SDD11 -10dB 2.5GT/s, -8dB 5GT/s, -4dB 8GT/s (differential)
  - ✓ SCC11 -6dB, -3dB 8GT/s (common-mode)

PCIe 3.0 Tx Jitter

- PCIe 3.0 Tx jitter is separated into two categories
  - ✓ Data Dependent: package loss, reflections, ISI
  - ✓ Uncorrelated Jitter: PLL jitter, power supply, duty cycle error
- Pulse Width Jitter (PWJ)
  - ✓ PWJ is a subset of uncorrelated jitter
  - ✓ PWJ is amplified by channel loss
  - ✓ Edges are assumed to be independent
- Relationship between pulse width jitter and edge jitter
  - ✓ Important for measurement and channel simulation tools



$PWJ = PW_{max} - PW_{min}$
Edge Jitter DJ= PWJ_DJ/2
Edge Jitter RJ = PWJ_RJ/√2

Receiver

Receiver

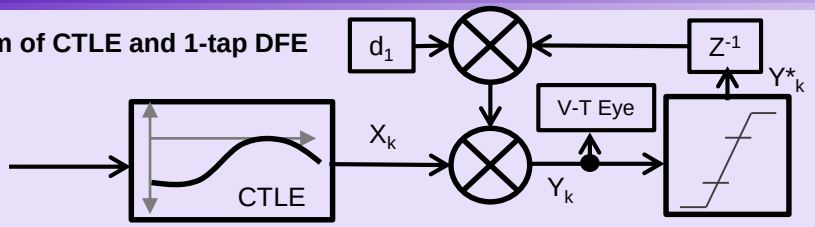
- 2.5/5GT/s open eye specification, validated at device pin, package included in device budget
  - ✓ Eye height 175/120mV 2.5/5GT/s
  - ✓ Eye width 0.4/0.32UI 2.5/5GT/s
  - ✓ AC common-mode 300mV pk-pk
- 8GT/s closed eye at pin, specified after applying behavioral receiver
  - ✓ Defines minimum Rx EQ performance
  - ✓ Used for both Rx stressed eye calibration and channel compliance
  - ✓ Eye height 25mV 8GT/s
  - ✓ Eye width 0.3UI 8GT/s
  - ✓ AC common-mode 150mV pk-pk (EH<100mV) 250mV (EH>=100mV)

Receiver Cont.

- Termination
  - ✓ 100ohm differential
  - ✓ 50ohm common-mode
    - 0v common-mode for detect
    - At 8GT/s Rx allowed to float common-mode
      - Requires LTSSM changes to avoid dead-locks
- Differential-mode return loss
  - ✓ 10dB 2.5GT/s, 8dB 5GT/s, 5dB 8GT/s
- Common-mode return loss
  - ✓ 6dB 2.5/5GT/s, 5dB 8GT/s

Behavioral Rx DFE

Block diagram of CTLE and 1-tap DFE

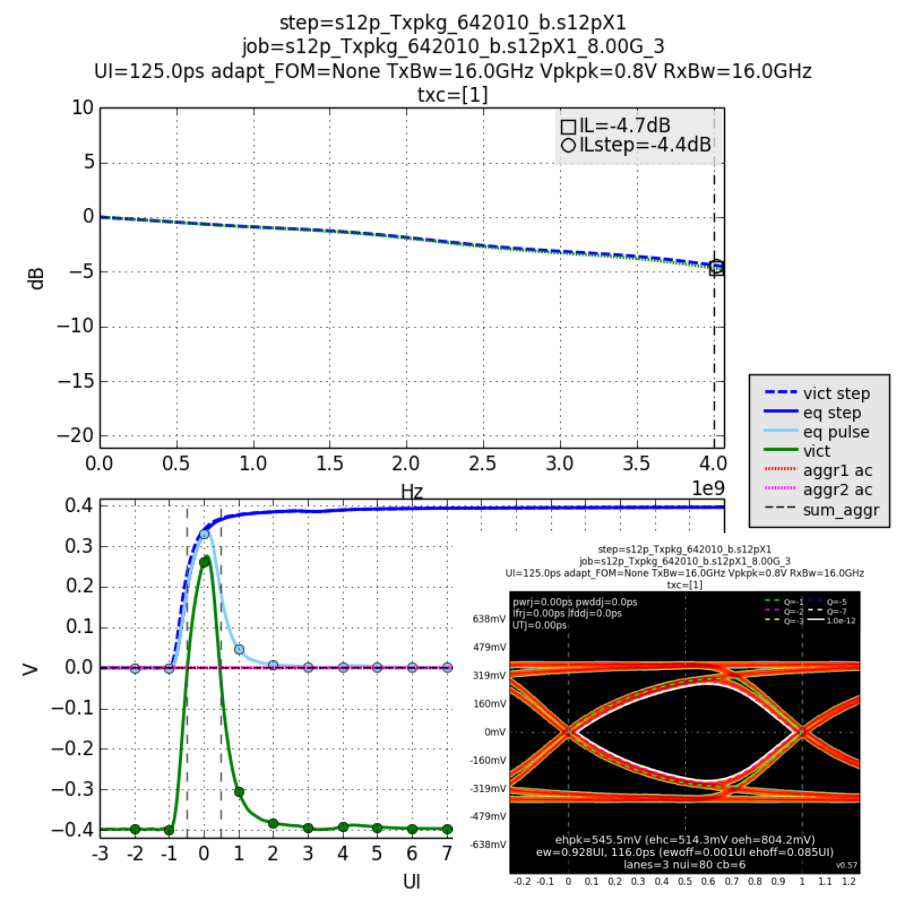


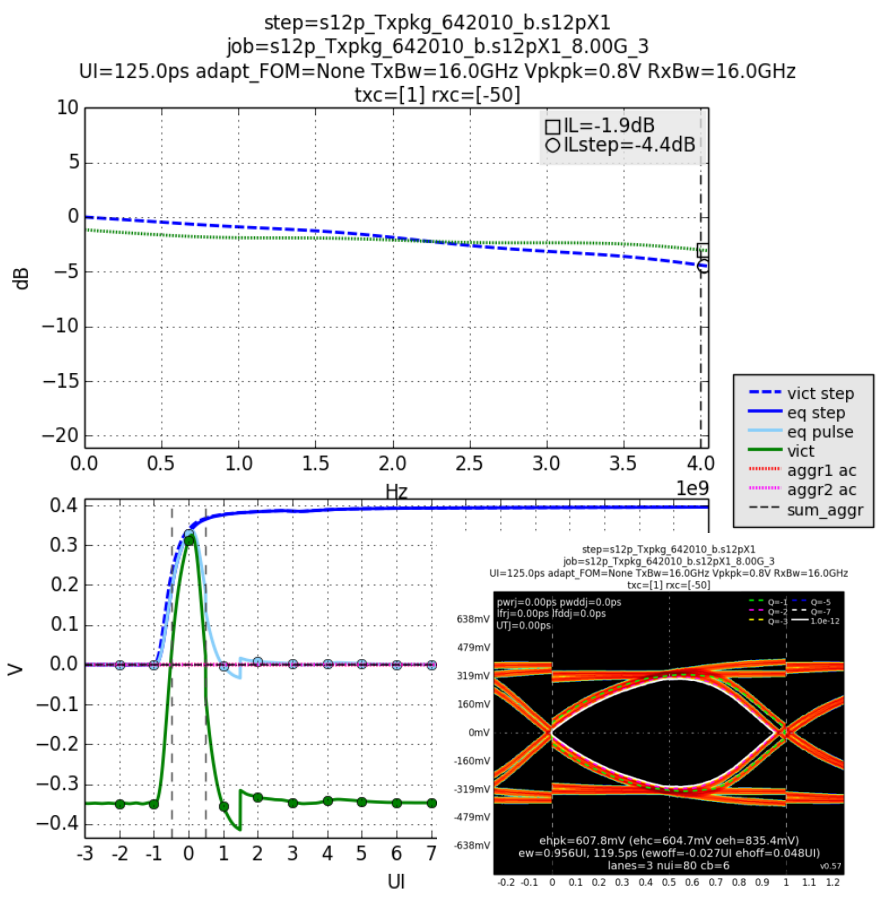
$$Y_k = X_k - d_1 * sgn(Y_k - 1) \Rightarrow DFE\ summer\ Vdiff\ output$$

$Y^*_k \Rightarrow$ *Decision Fn output voltage* $\Rightarrow |Y^*_k| = 1$

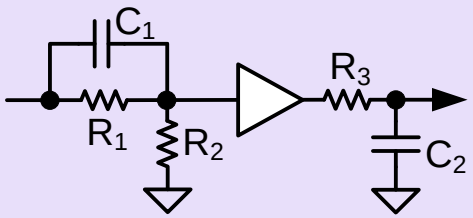
$X_k \Rightarrow$ *DFE Vdiff output voltage*

$d_1 \Rightarrow$ *DFE feedback coefficient* K $\Rightarrow$ *sample index*





Rx Linear EQ



$$H(s) = \frac{sC_1R_1R_2 + R_2}{sC_1R_1R_2 + R_1 + R_2} \cdot \frac{1}{sC_2R_3 + 1}$$

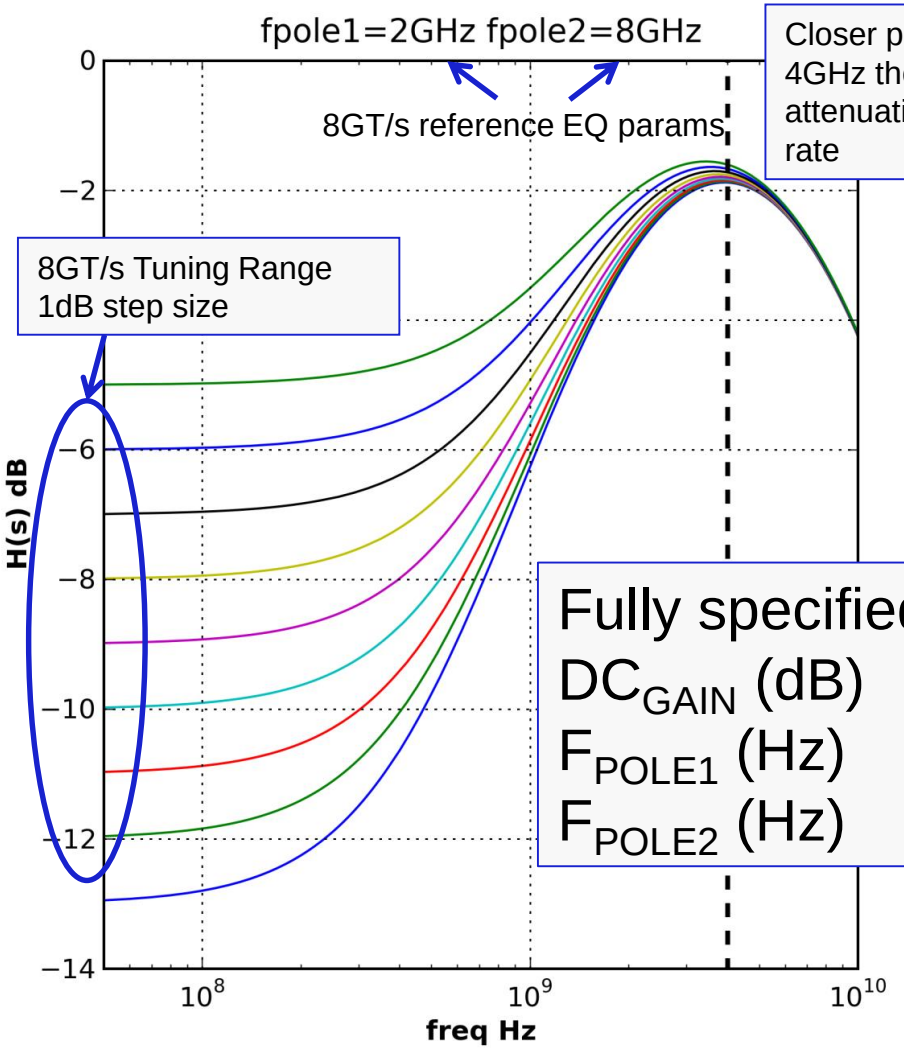
$$H(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{\frac{s}{\omega_Z} + 1}{\frac{s}{\omega_{P1}} + 1} \cdot \frac{1}{\frac{s}{\omega_{P2}} + 1}$$

$$G_{DC} = \frac{R_2}{R_1 + R_2}$$

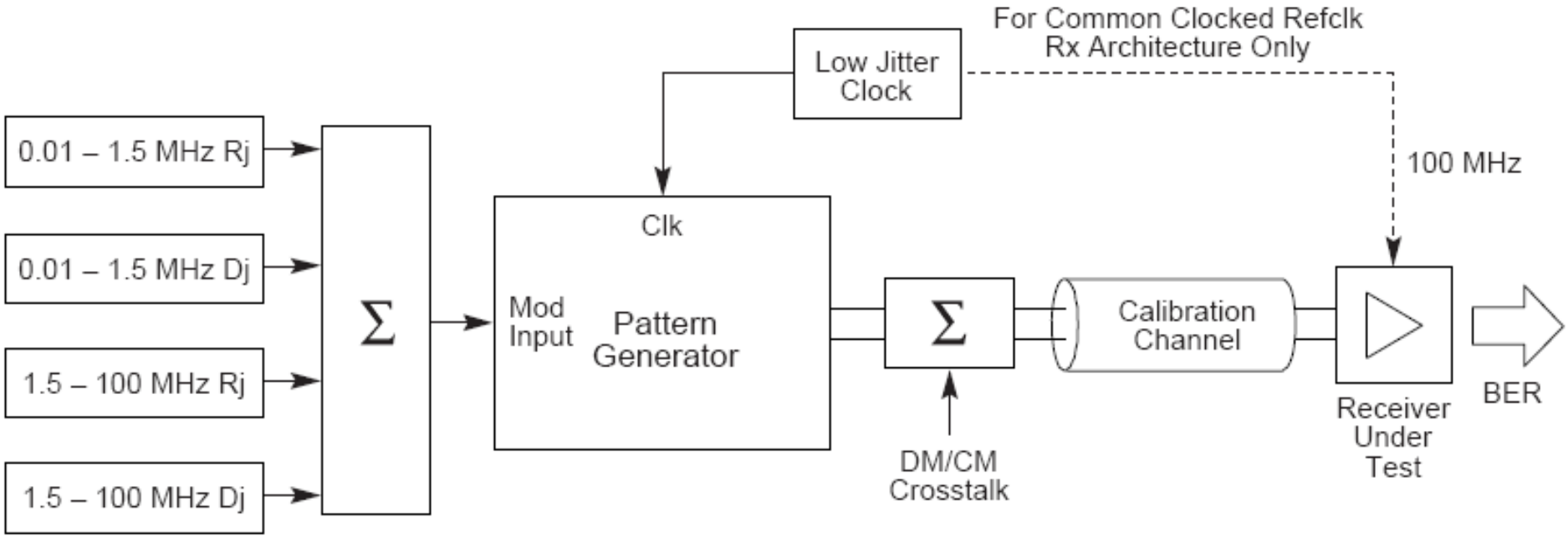
$$\omega_{P1} = \frac{R_1 + R_2}{C_1R_1R_2}$$

$$\omega_Z = \frac{1}{C_1R_1} = G_{DC}\omega_{P1}$$

$$\omega_{P2} = \frac{1}{C_2R_3}$$



Receiver Compliance Testing

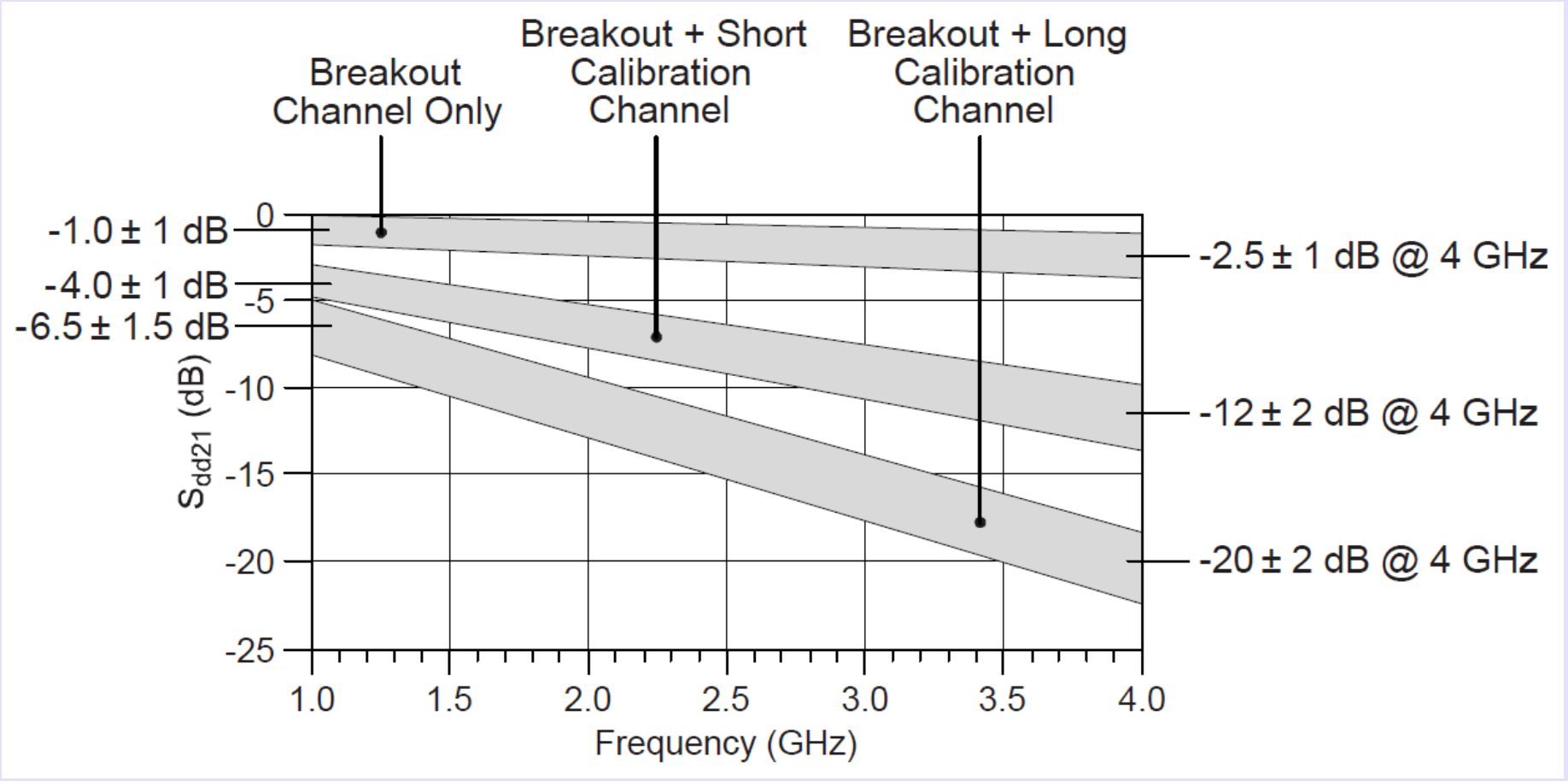


Stressed eye calibrated at pin reference plane

Error rate measured using loopback

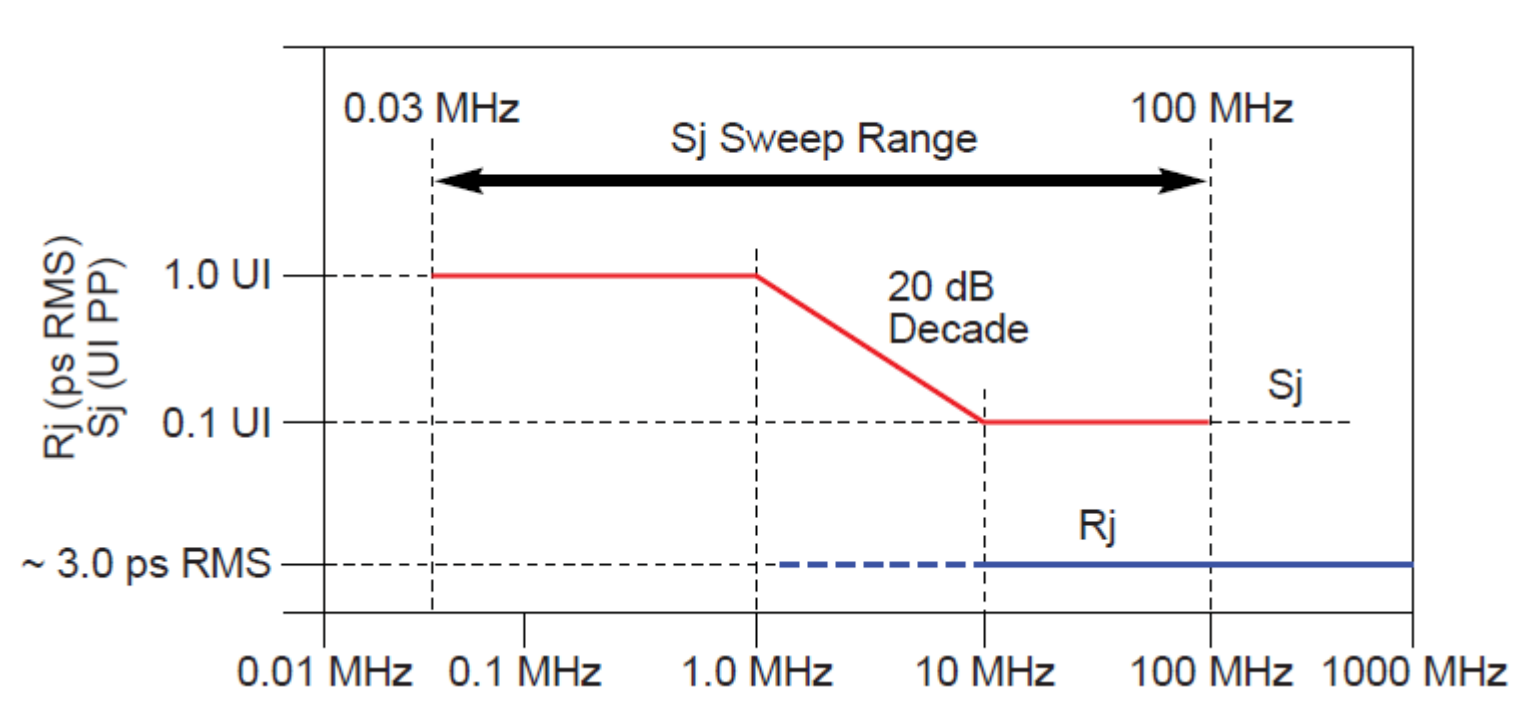
Pass BER 10^{-12}

8GT/s Calibration Channels



Frequency domain mask used for ISI stress to match tuning range of Rx EQ

8GT/s Receiver Jitter Tolerance Testing



Validates that Rx can track LF jitter from refclk and Tx

Seasim

High Speed Channel Simulation Challenges

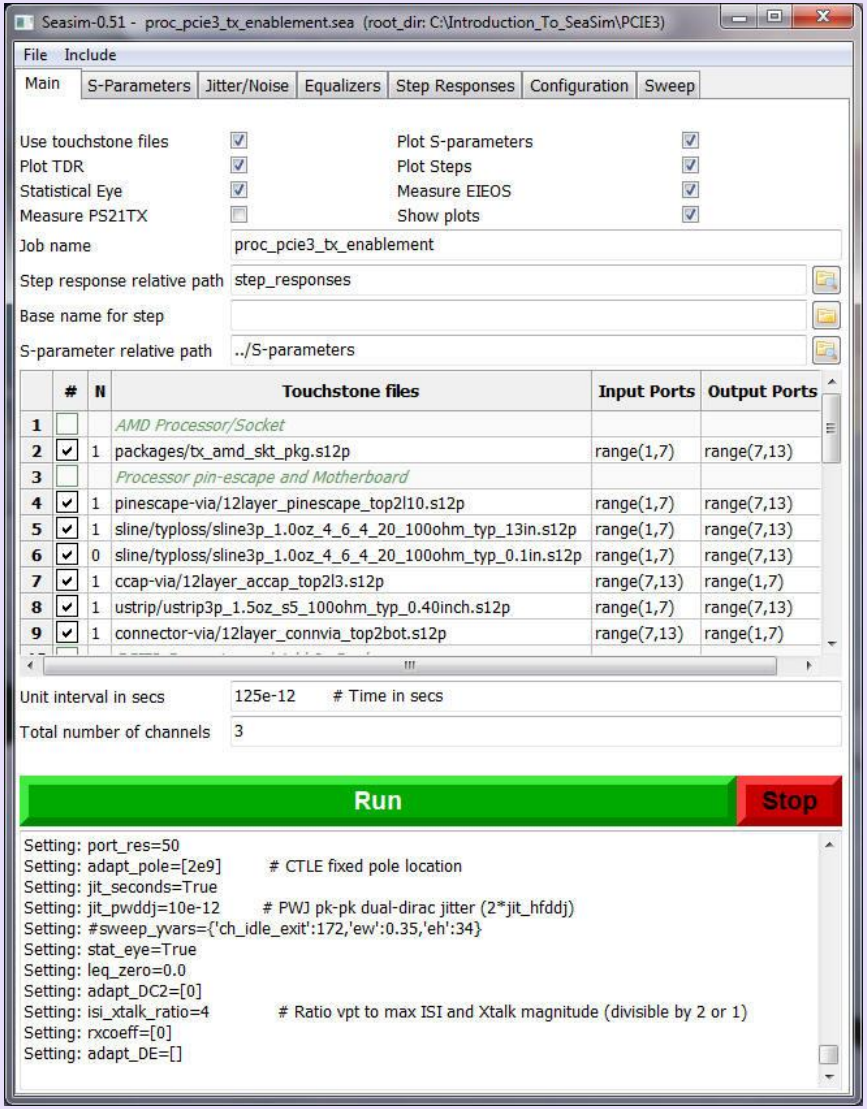
- Channel response at >4GHz is affected by large number of features in the channel
  - ✓Pre-layout evaluation of topology choices is a complicated multi-dimensional problem
  - ✓Need to be able to quickly build and test many different options
  - ✓Large number of HVM permutations need to be evaluated to determine robustness of solution
- Seasim has been developed to allow EWG members to efficiently evaluate these options

Seasim Introduction

- A GUI form based interface
  - ✓ Underlying config file interface to seasim provides spec jitter parameters for channel simulations
  - ✓ A simple form based dialogue tool added
  - ✓ Tab based interface to group config controls by context
  - ✓ Ability to save and load configurations
  - ✓ Launch (and kill) seasim from GUI
- Touchstone channel modeling
  - ✓ A set of Touchstone files can be cascaded to form die-pad to die-pad channel
  - ✓ A vector of left hand and right hand ports define connections between S-parameters
  - ✓ Rx port and set of Tx ports define step responses to be generated
  - ✓ Tx amplitude and Gaussian bandwidth can be specified

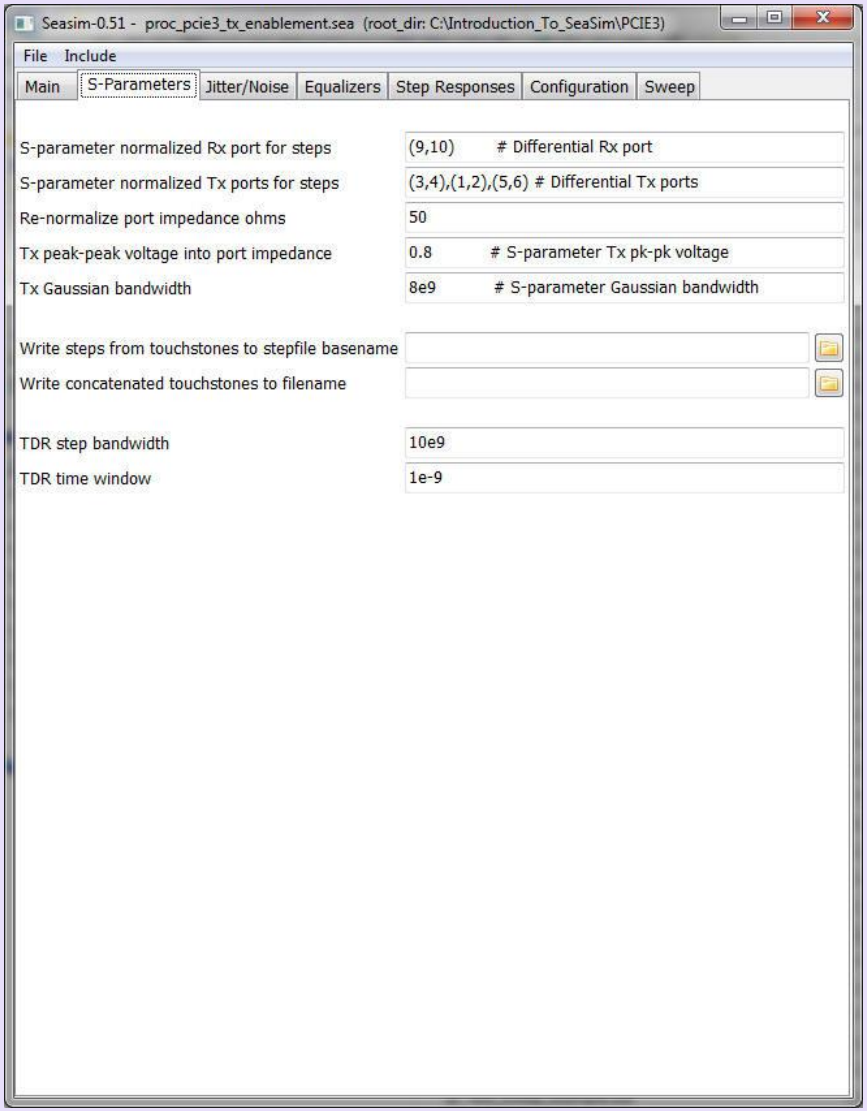
Seasim Channel Analysis

- Allows what-if analysis on the channel components by changing the Touchstone files that are concatenated together for the channel
- Different analyses can be selected as the channel is ‘tuned’
- Either a pre-saved config can be loaded or the pcie-gen3.inc for normal sim conditions
- The other tabs allow simulation conditions to be changed from the default config



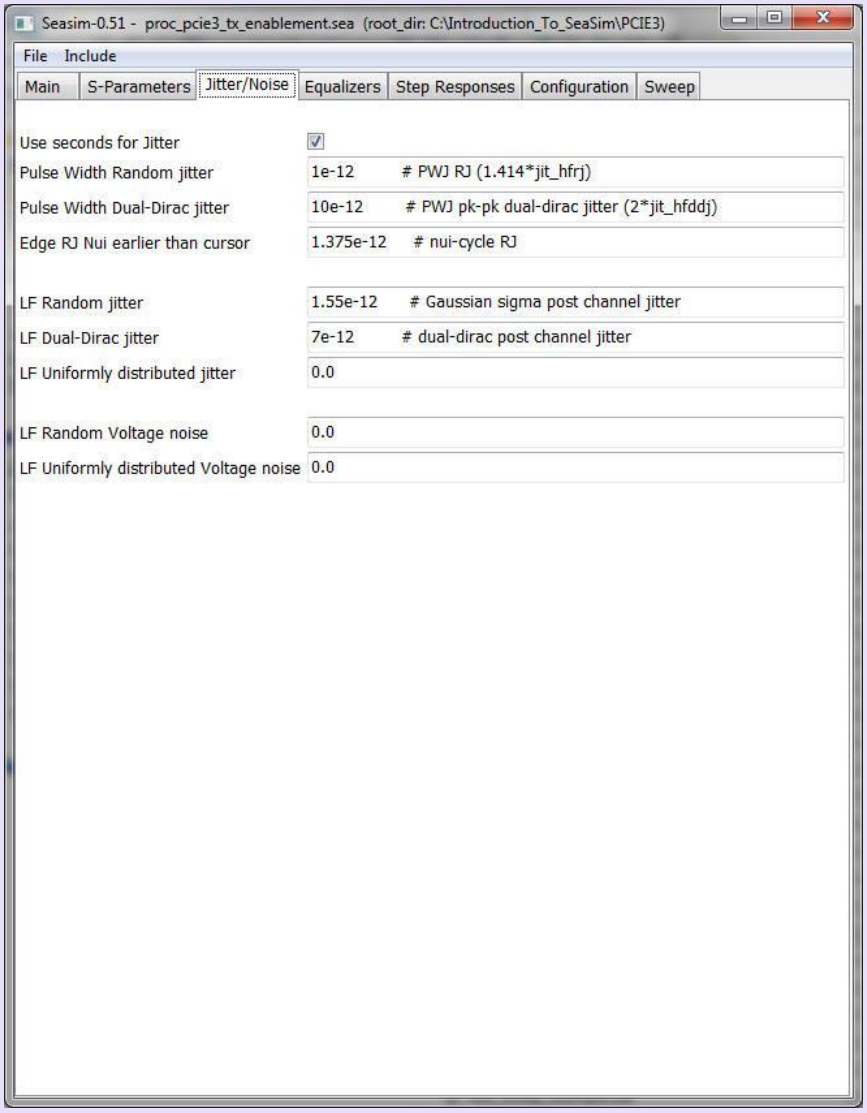
Seasim Port Definitions

- Touchstone tuple port definitions
  - ✓ Reflects the S-parameter models intrapair net order
  - ✓ Provides pair-to-pair (victim/aggressor) relationship for crosstalk inclusion
- Transmitter ports
  - ✓ Allows renormalization of port impedance by providing a list of terminal impedance values
  - ✓ Define transmitter pad differential voltage amplitude
  - ✓ Transmitter bandwidth defined by Gaussian filter setting
- Receiver port
  - ✓ Provide custom port renormalization impedance



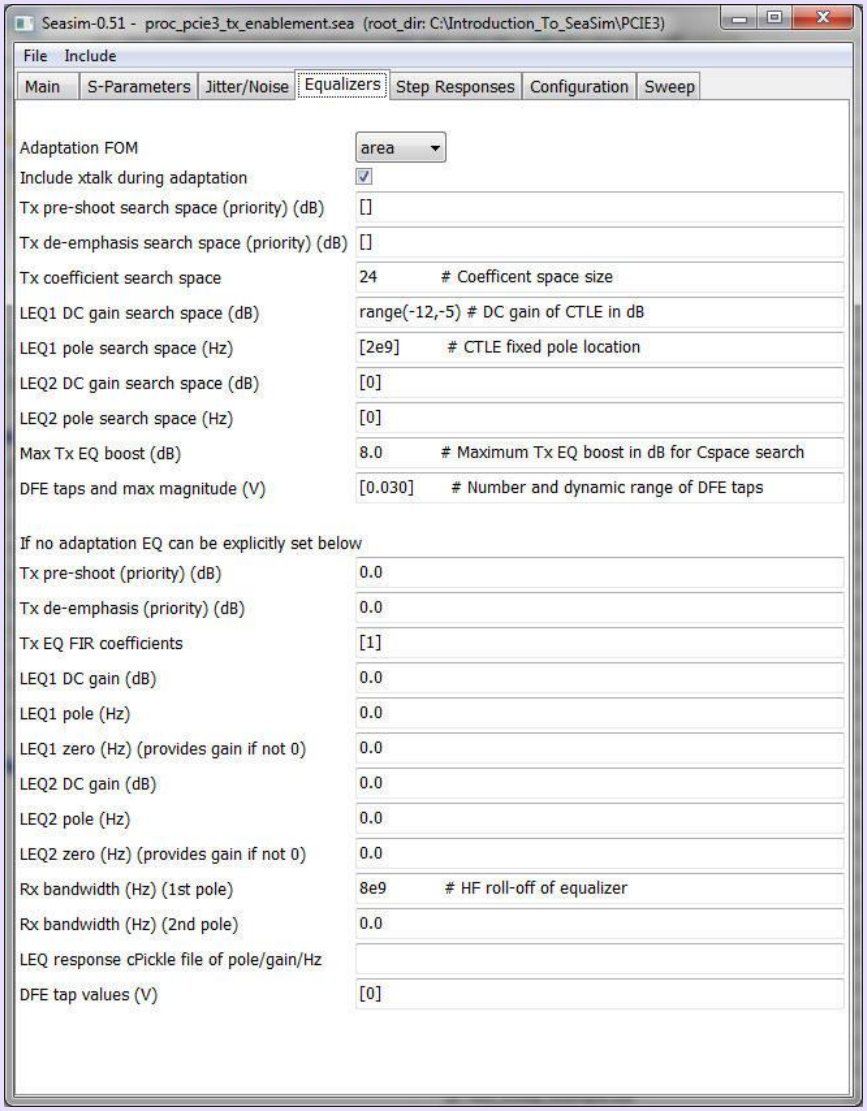
Seasim Jitter Configuration

- Jitter
  - ✓ Consistent jitter definitions with the PCIe base spec
  - ✓ Default jitter settings can be loaded with the default configuration file
  - ✓ Jitter values can also be customized using the field in the GUI and saved
- Noise
  - ✓ Random low frequency noise can be defined in addition to the aggressor-victim coupling present in the Touchstone file



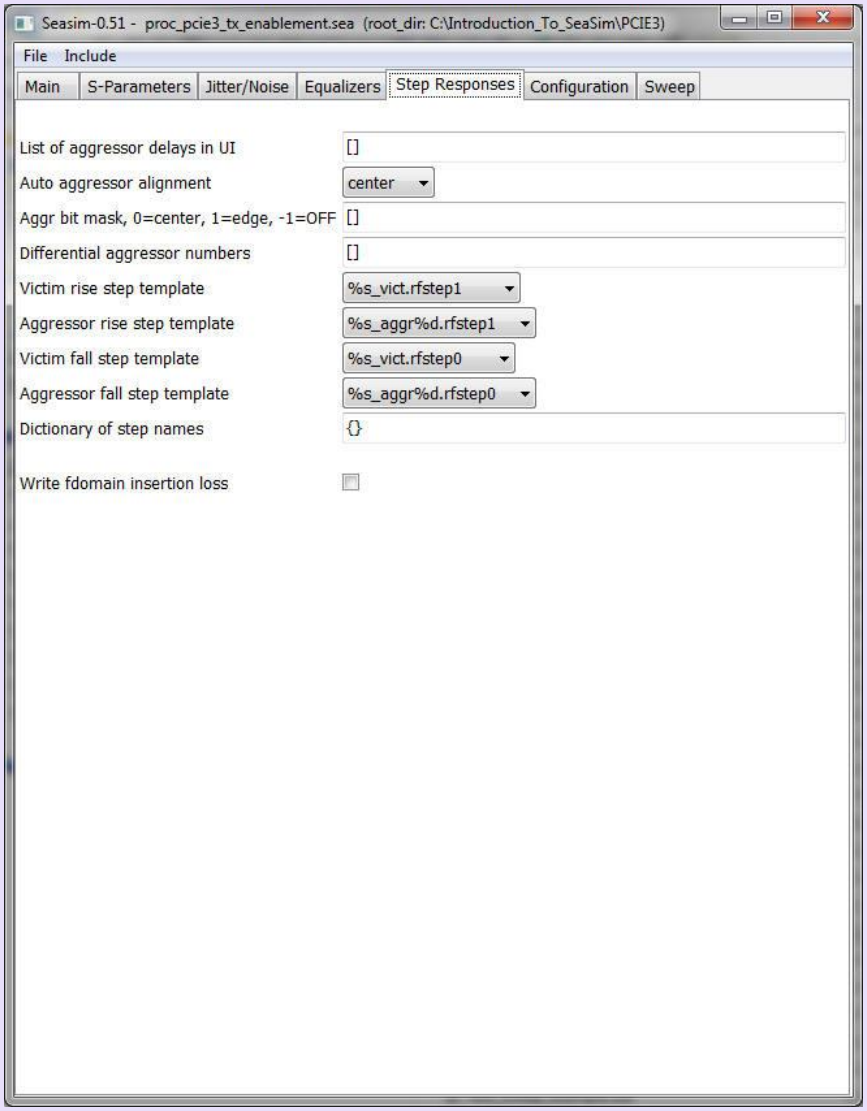
Seasim Equalization

- Tx FIR Filter
  - ✓ Can either fix pre-shoot and de-emphasis or set coefficient search space for adaptation
- Rx Linear Equalizer
  - ✓ Define pole/zero value or range of values for adaptation
  - ✓ May cascade multiple continuous time LEQ filters
- Decision Fed Equalizer
  - ✓ Can enable multiple DFE taps beyond defaults
  - ✓ Can vary dynamic range of taps independently



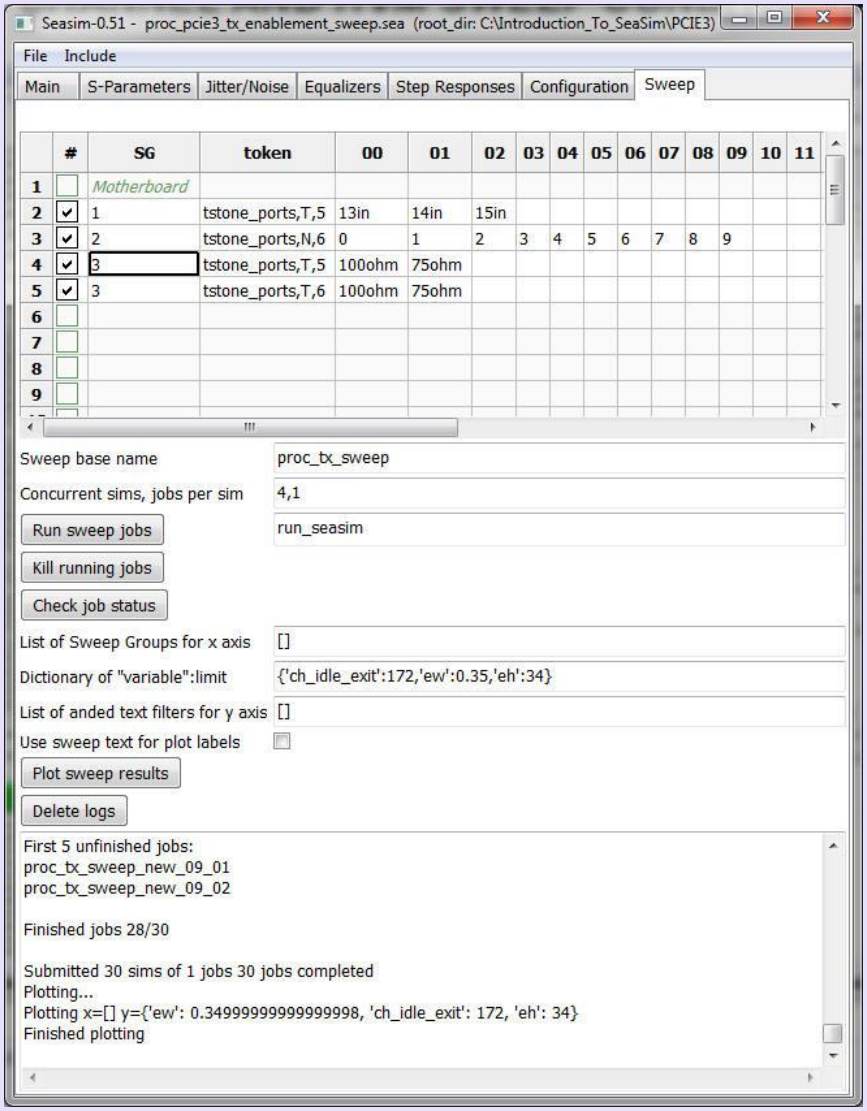
Seasim Step Responses

- Channel Step Response
  - ✓ Alternative simulation method to providing channel S-parameter models
  - ✓ Measured or simulated voltage-time records of channel step responses can be used directly for statistical simulation
- Crosstalk
  - ✓ Independent waveforms can be supplied for the inclusion of aggressor coupling to the victim receiver
  - ✓ Can optionally offset the aggressor-to-victim alignment

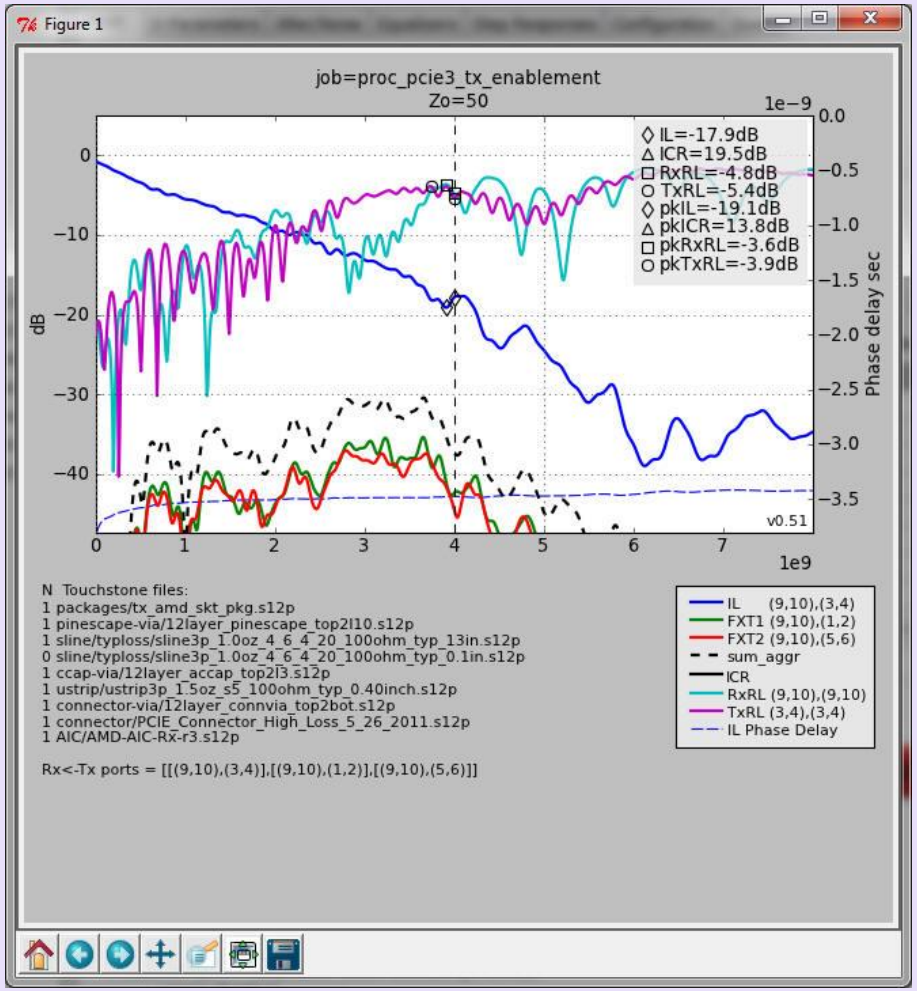


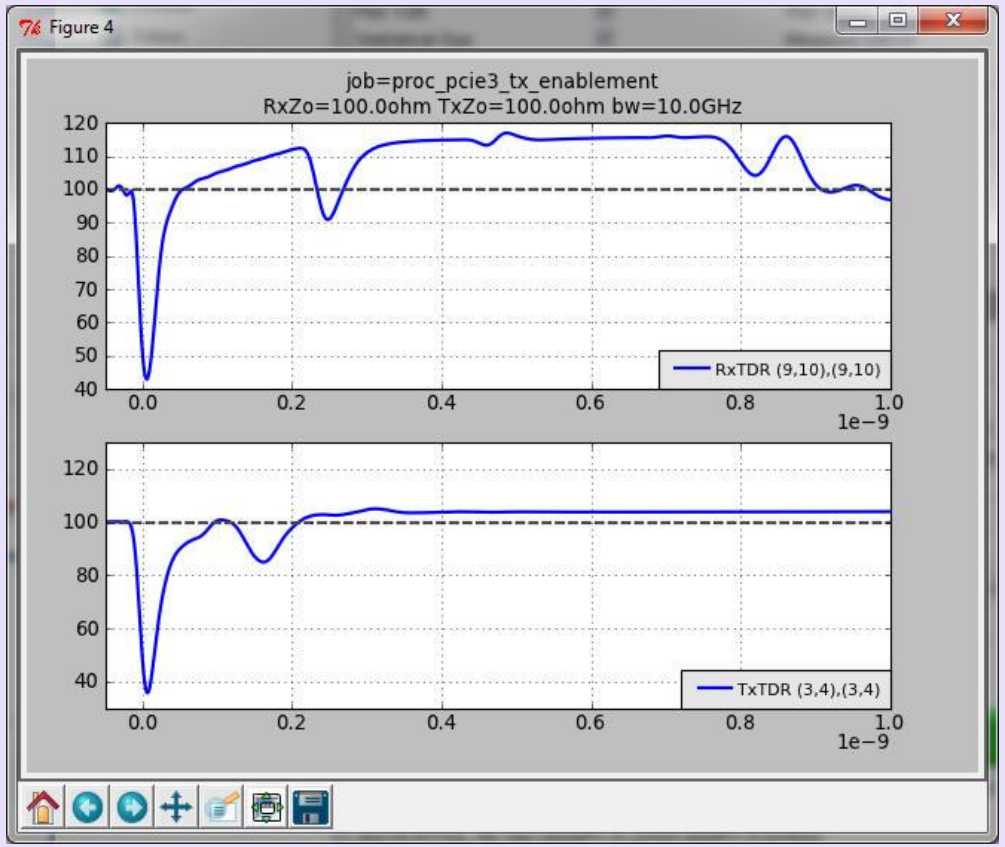
Seasim Sweep

- Seasim can be used to define HVM sweeps
- The channel model can be swept to represent manufacturing variations of impedance or loss
- To consider the impact of different PCB layout the length of different channel segments can be swept
- Seasim will launch jobs in parallel then collect results and plot them

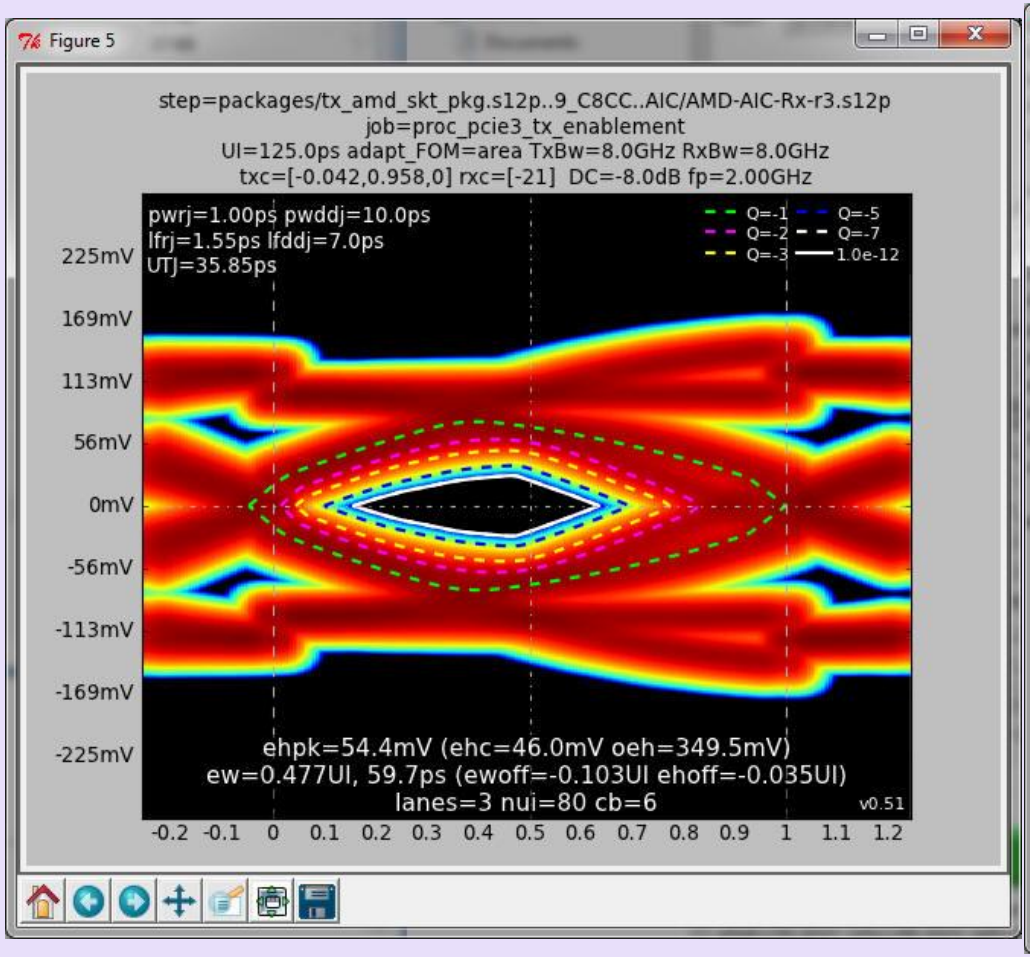


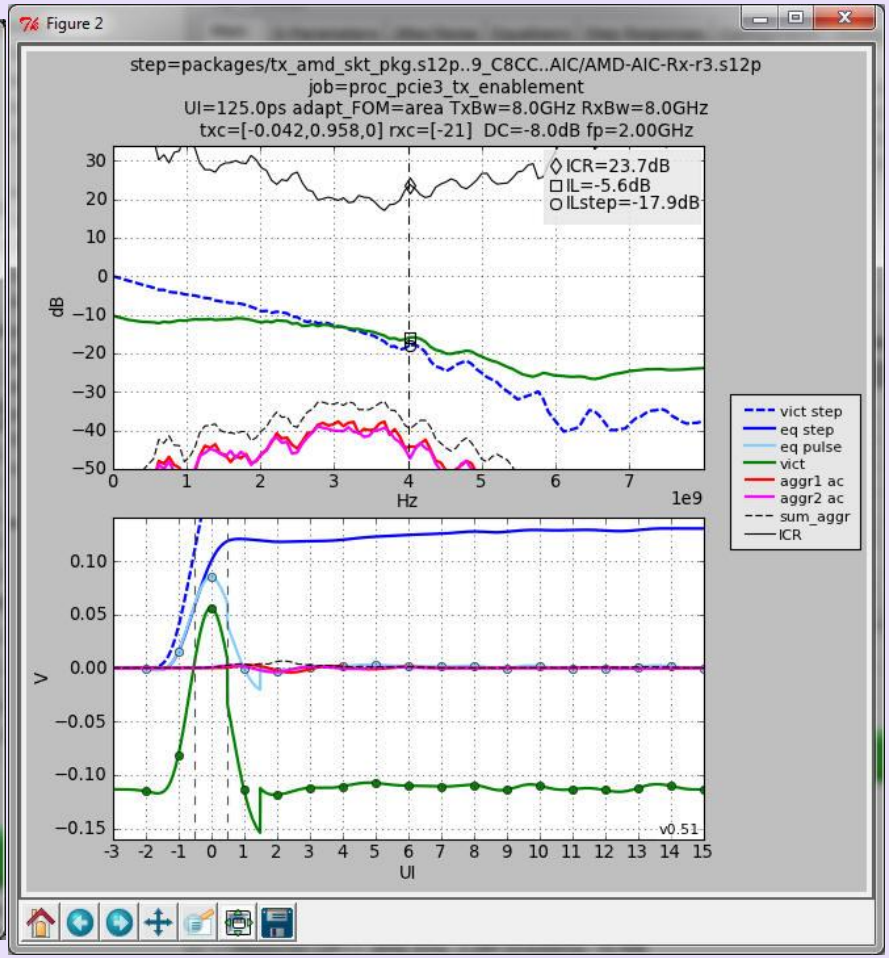
Seasim Channel Simulation Frequency Response & Bidir TDR



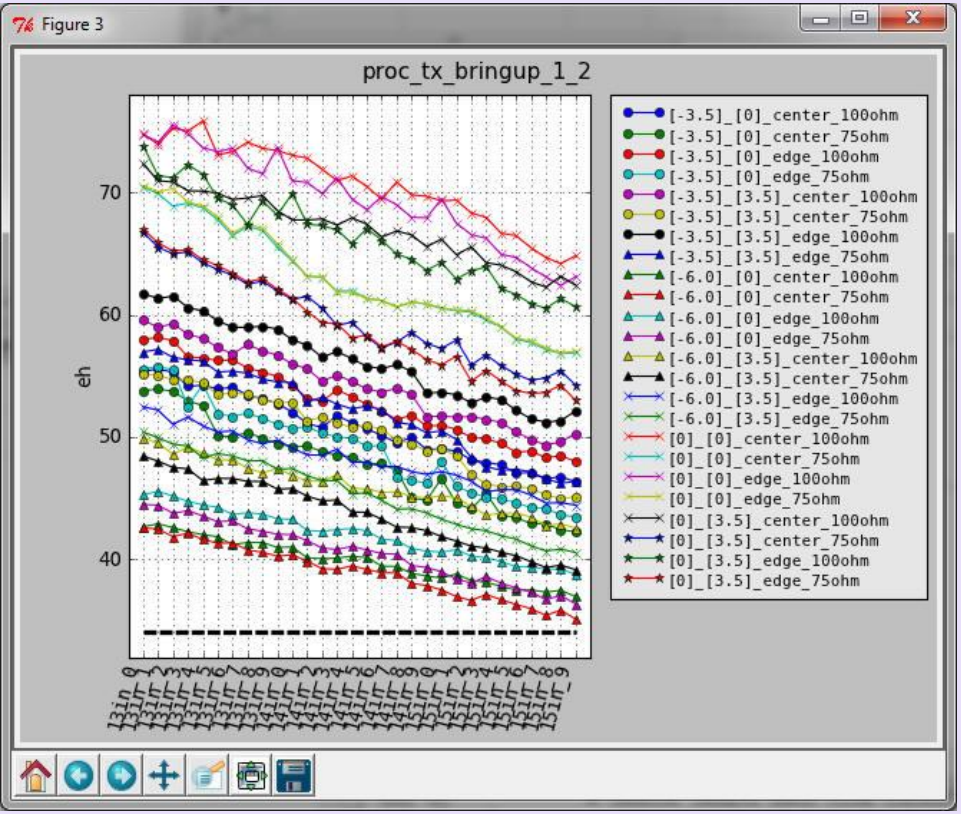


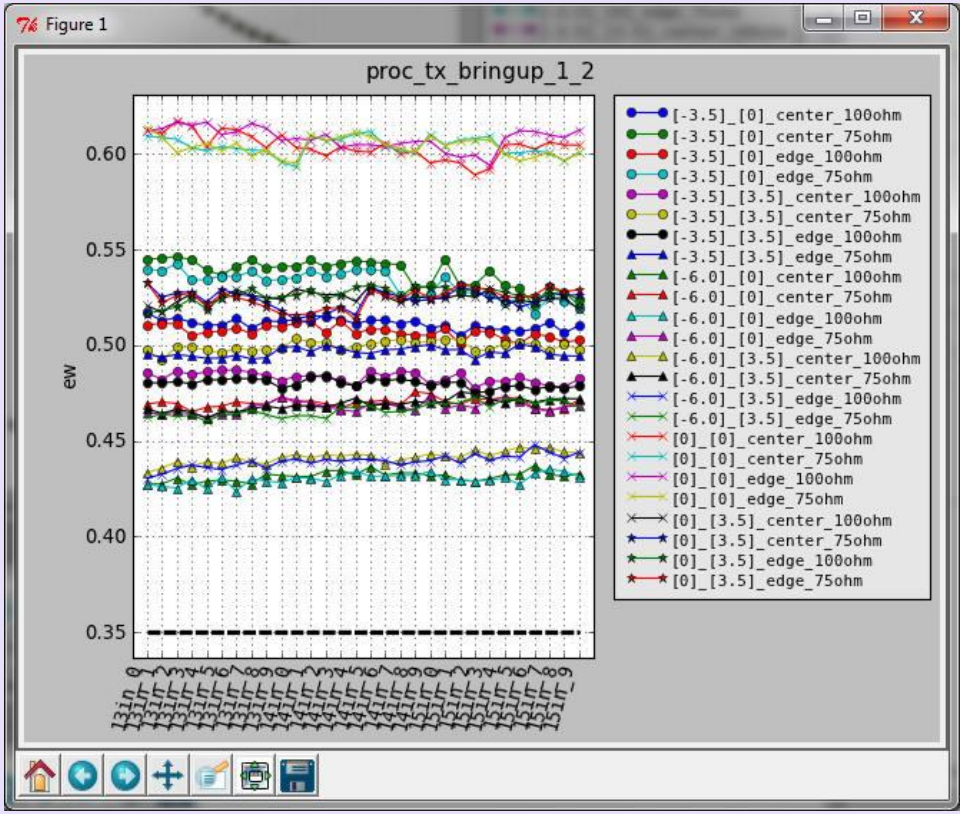
Seasim Output Eye & Equalized Freq & Time Response





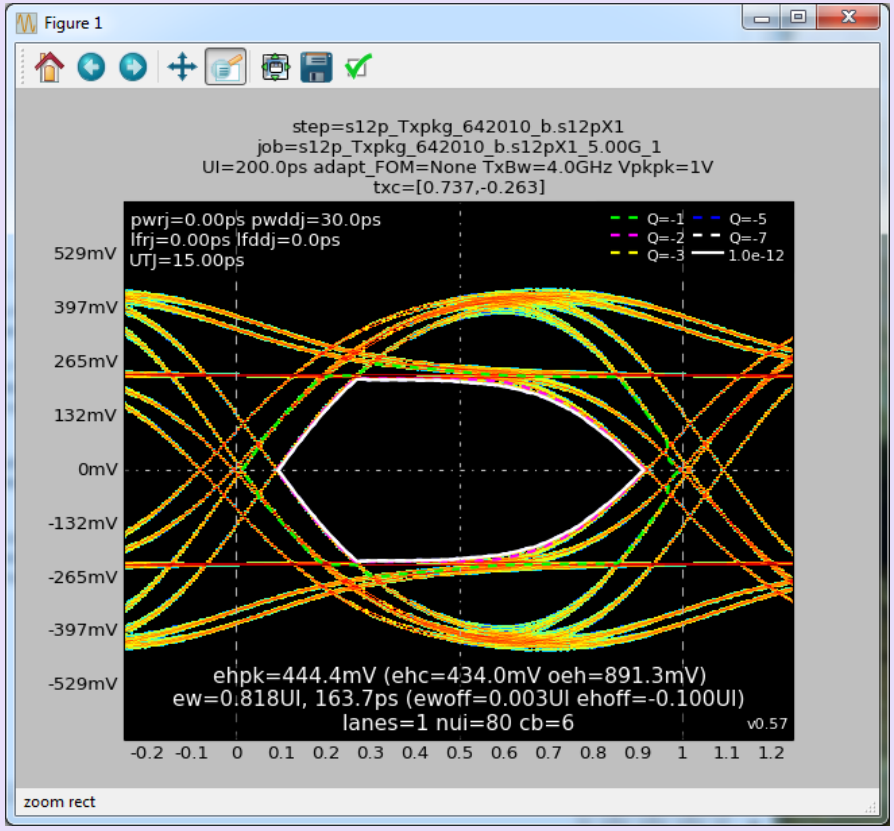
Seasim Sweep Results Analysis Plots

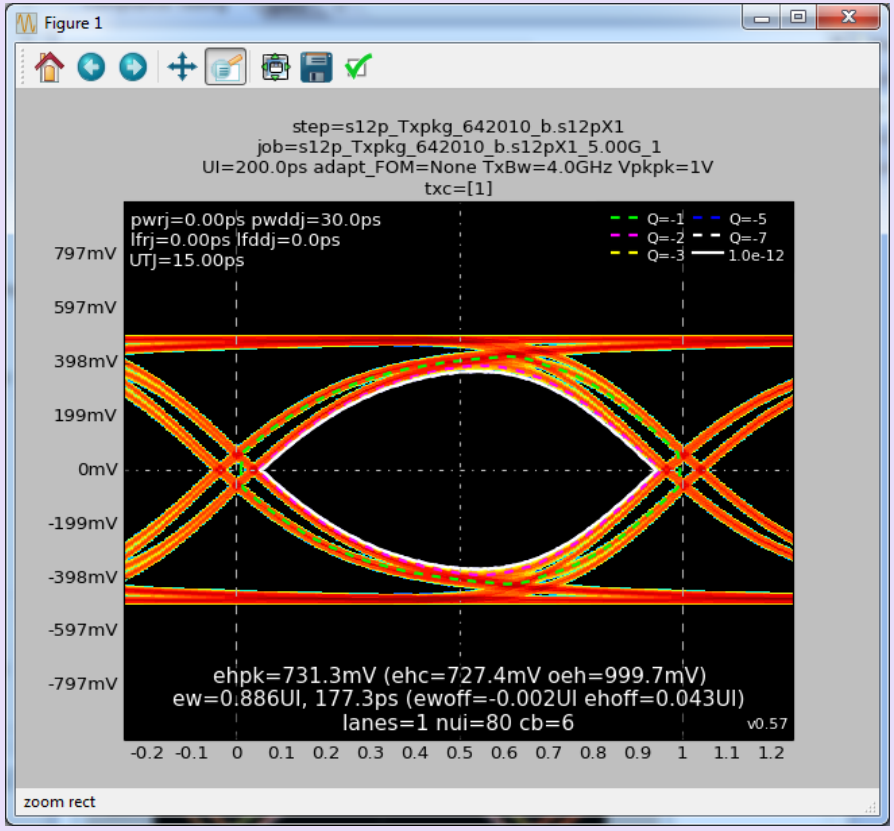




Seasim Legacy Data Rate Simulation Setup

- PCIe 2.x simulation requires calibrating the transmitter De-emphasis and signal amplitude at the package pin (i.e. -6dB/0.8V/0.9UI)

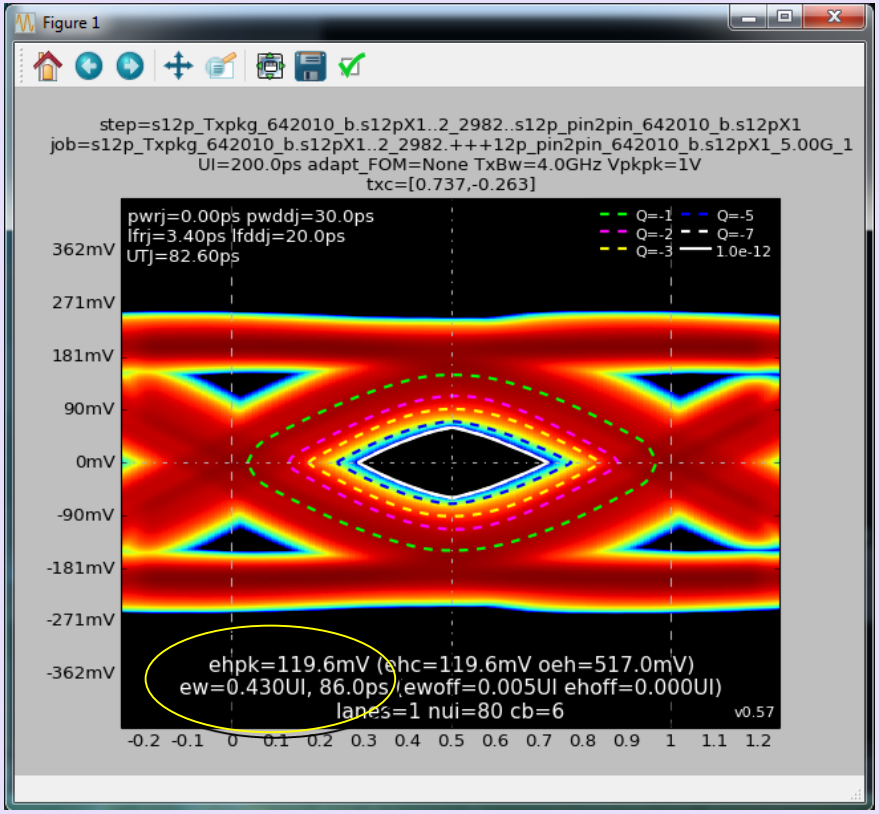




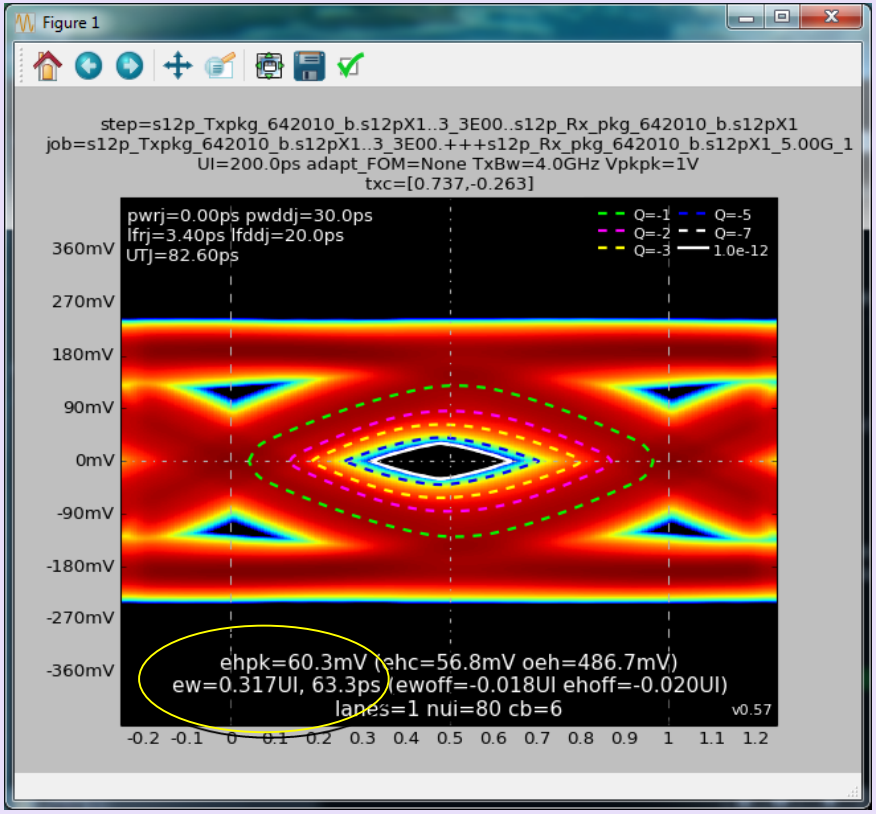
Seasim Legacy Data Rate Simulation Setup

- Waveform simulated at the receiver pin of the 8GT/s compliance channel

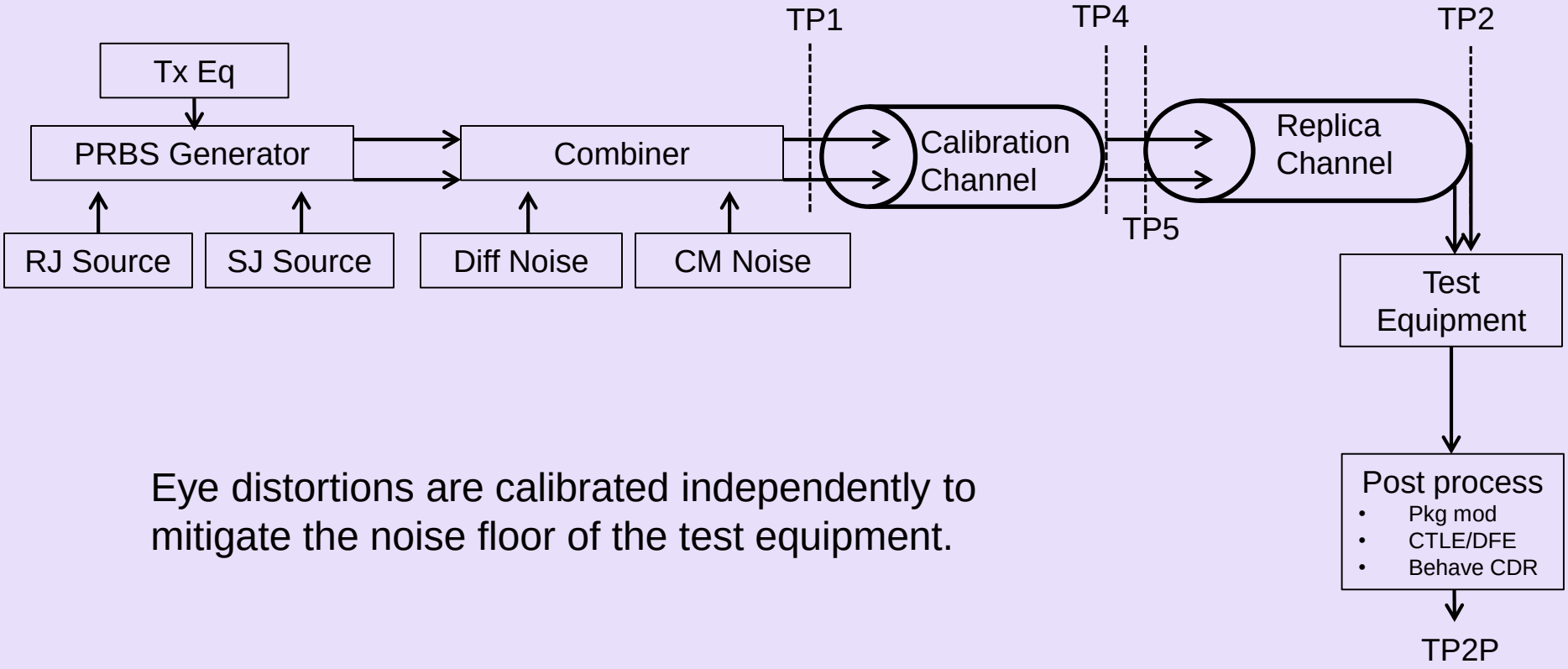
Simulated at the receiver pin of the 8GT/s compliance channel. PCIe 2.x min is 120mV/0.4UI.



Simulated at the receiver pad using the 8GT/s spec Tx pkg + spec channel + spec Rx pkg.



Seasim Rx Tolerance Calibration

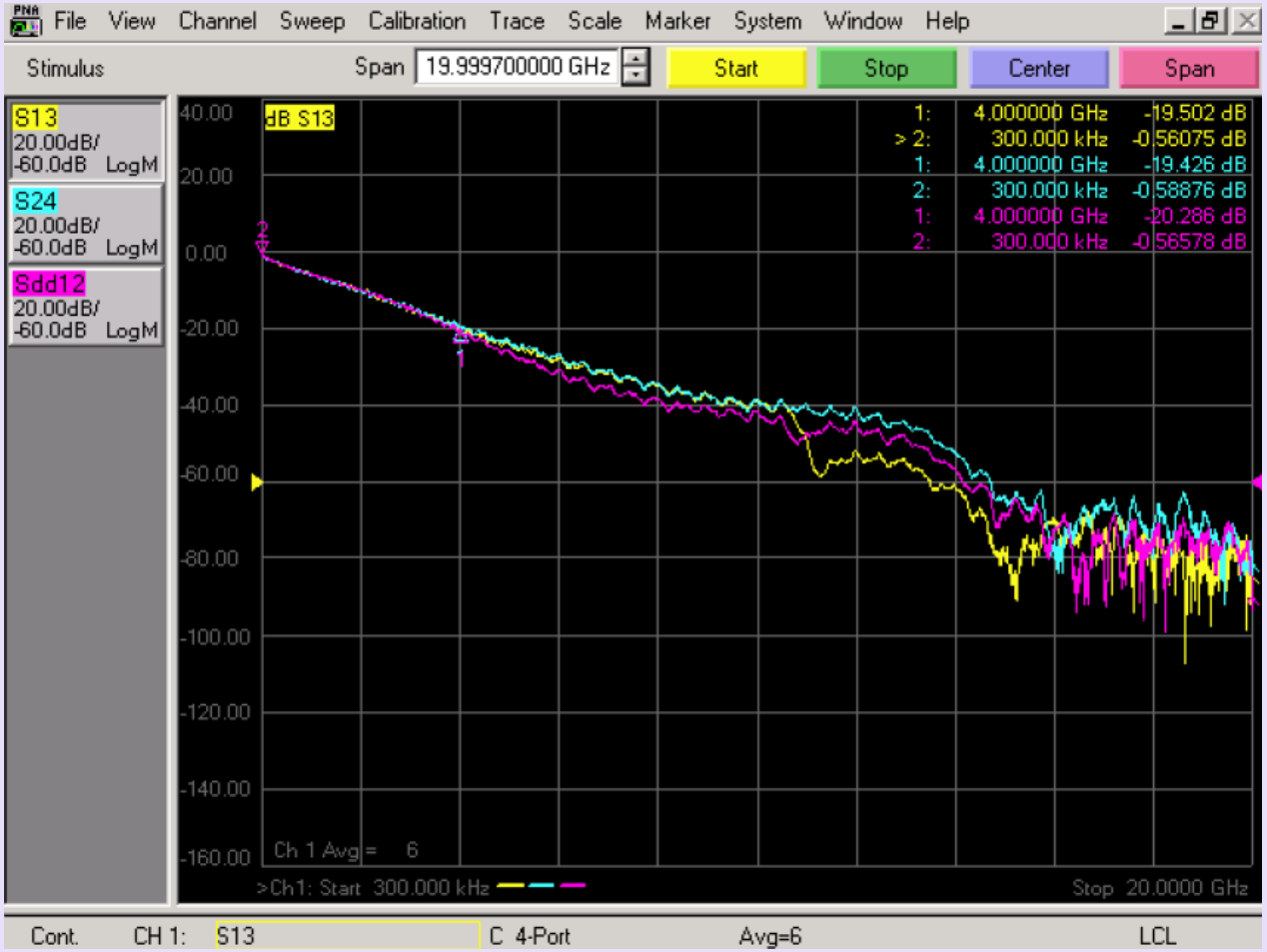


Eye distortions are calibrated independently to mitigate the noise floor of the test equipment.

Three Phases to Calibration

- Channel ISI and behavioral Rx EQ
  - ✓ Calibrate loss from TP1 to TP2
    - Fine adjustment with generator equalization
  - ✓ Use base spec PDA search for CTLE and DFE settings
    - Constrained to be no better than what's used in channel compliance
- Phase jitter, differential voltage noise and common-mode noise
  - ✓ Use Seasim to calculate required RJ & VN
  - ✓ Set and measure RJ & SJ at TP1
    - Assumes jitter amplification in channel is negligible
  - ✓ Set and measure VN & CMN at TP2
    - VN de-embedded from ideal Rx-latch back to TP2
- Cumulative eye measurement
  - ✓ All distortions applied, extrapolate and interpolate to 10^{-12} & 10^{-6}

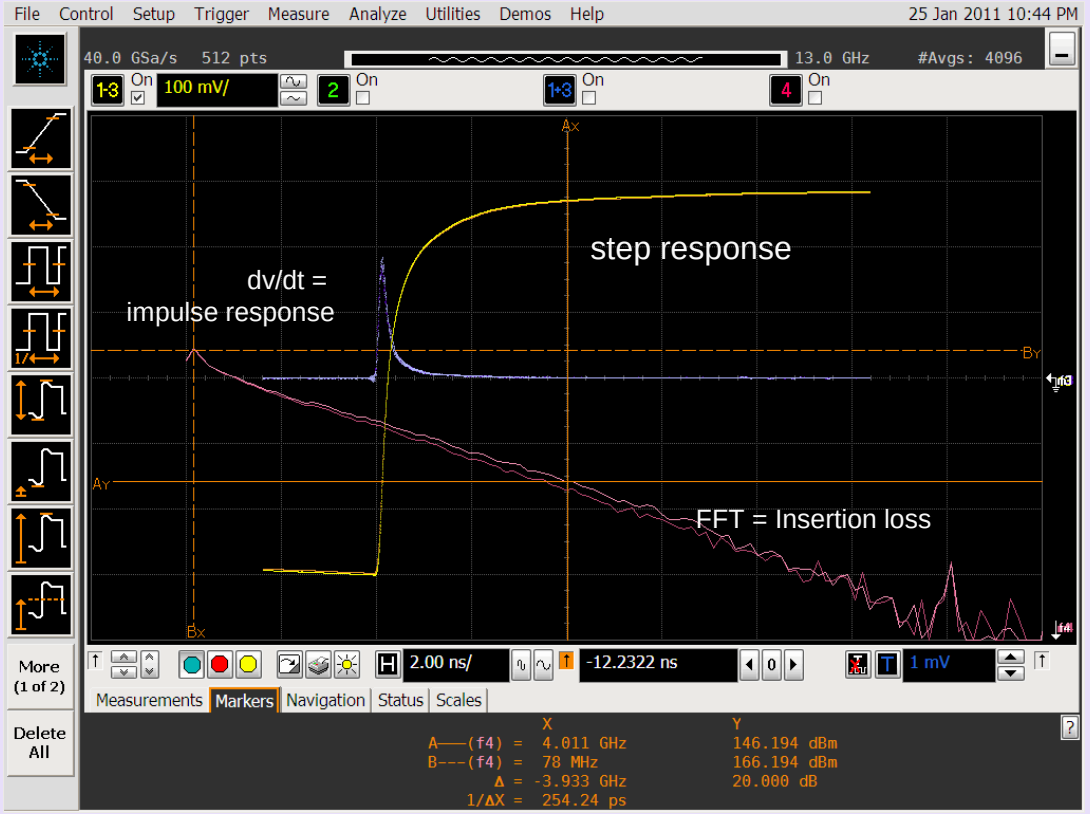
VNA Measurement TP1 to TP2



Needs to include all cables used for measurement.

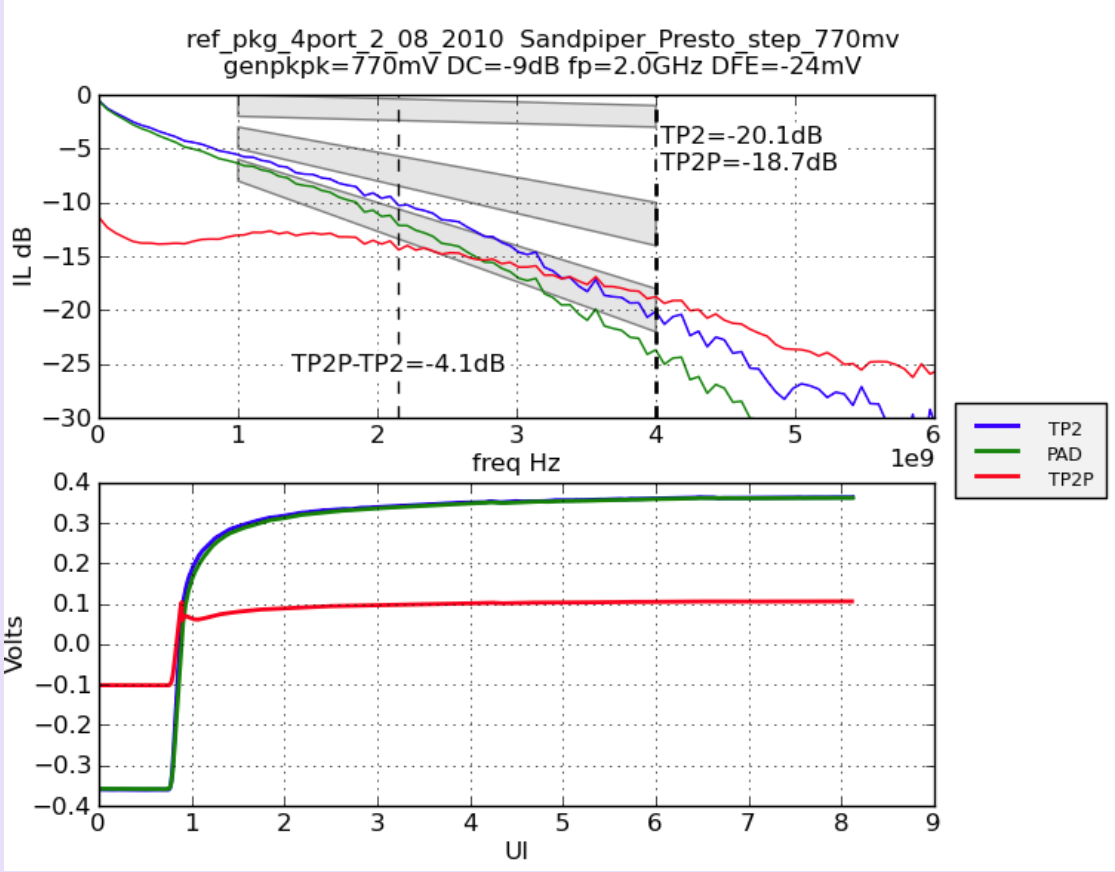
Step Response

- Scope averaged and interpolated step response at TP2
- 128 UI 1/0 clock waveform
- 1ps time steps

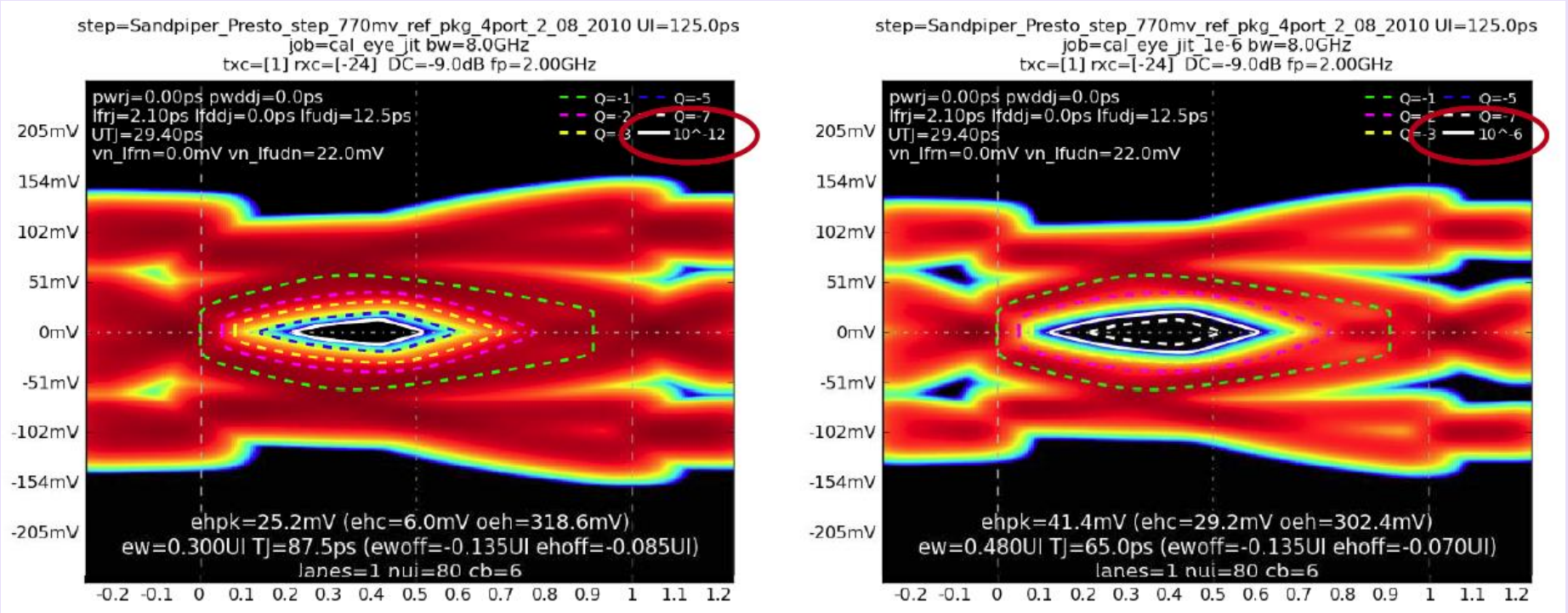


Post Process Step Response

- Pad waveform is TP1 channel extended by behavioral package to Rx die pad
- Difference between TP2P and TP2 (-4.1dB) at 2.1GHz used to de-embed VN to TP1



Seasim RJ & VN Calculation



*May need to iteratively tune generator amplitude and VN to get EW > 0.3UI and EH = 25mV

Thank you for attending the PCIe Technology Seminar

For more information please go to www.pcisig.com

Backup

Derivation of Coefficients

$$DE = \frac{Vb}{Va}; \quad PS = \frac{Vc}{Vb}$$

$$t_0 + t_1 + t_2 = 1; \quad \underline{t_1 = 1 - t_0 - t_2}$$

$$DE = \frac{V_{PK}(-t_0 + t_1 - t_2)}{V_{PK}(-t_0 + t_1 + t_2)} = \frac{1 - 2t_0 - 2t_2}{1 - 2t_0}$$

$$PS = \frac{V_{PK}(+t_0 + t_1 - t_2)}{V_{PK}(-t_0 + t_1 - t_2)} = \frac{1 - 2t_2}{1 - 2t_0 - 2t_2}$$

$$DE \cdot PS = \frac{1 - 2t_2}{1 - 2t_0}$$

$$2t_2 = 1 - DE \cdot PS(1 - 2t_0)$$

$$DE = \frac{1 - 2t_0 - 1 + DE \cdot PS(1 - 2t_0)}{1 - 2t_0} = \frac{-2t_0}{1 - 2t_0} + DE \cdot PS$$

$$2t_0 = (DE \cdot PS - DE)(1 - 2t_0)$$

$$2t_0 = DE \cdot PS - DE + 2t_0 DE - 2t_0 DE \cdot PS$$

$$2t_0(1 - DE + DE \cdot PS) = DE \cdot PS - DE$$

$$2t_0 = \frac{DE \cdot PS - DE}{1 + DE \cdot PS - DE}$$

$$\underline{t_0 = \frac{DE(PS - 1)}{2 + 2DE(PS - 1)}}$$

$$2t_2 = 1 - DE \cdot PS(1 - 2t_0)$$

$$2t_2 = 1 - DE \cdot PS + 2DE \cdot PSt_0$$

$$2t_2 = 1 - DE \cdot PS + DE \cdot PS \frac{DE(PS - 1)}{1 + DE(PS - 1)}$$

$$2t_2 = \frac{(1 + DE(PS - 1))(1 - DE \cdot PS) + DE^2 \cdot PS(PS - 1)}{1 + DE(PS - 1)}$$

$$2t_2 = \frac{1 - DE \cdot PS + DE(PS - 1) - DE^2 \cdot PS(PS - 1) + DE^2 \cdot PS(PS - 1)}{1 + DE(PS - 1)}$$

$$2t_2 = \frac{1 - DE \cdot PS + DE \cdot PS - DE}{1 + DE(PS - 1)}$$

$$\underline{t_2 = \frac{1 - DE}{2 + 2DE(PS - 1)}}$$

Tx FIR Coefficients

PS	0			1			2			3			4		
DE	c0	c1	c2	c0	c1	c2	c0	c1	c2	c0	c1	c2	c0	c1	c2
0	0.000	1.000	0.000	-0.054	0.946	0.000	-0.103	0.897	0.000	-0.146	0.854	0.000	-0.185	0.815	0.000
-1	0.000	0.946	-0.054	-0.049	0.902	-0.049	-0.094	0.862	-0.044	-0.134	0.826	-0.040	-0.171	0.793	-0.036
-2	0.000	0.897	-0.103	-0.044	0.862	-0.094	-0.085	0.829	-0.085	-0.123	0.799	-0.077	-0.159	0.771	-0.070
-3	0.000	0.854	-0.146	-0.040	0.826	-0.134	-0.077	0.799	-0.123	-0.113	0.774	-0.113	-0.146	0.750	-0.103
-4	0.000	0.815	-0.185	-0.036	0.793	-0.171	-0.070	0.771	-0.159	-0.103	0.750	-0.146	-0.135	0.730	-0.135
-5	0.000	0.781	-0.219	-0.032	0.763	-0.205	-0.064	0.745	-0.191	-0.094	0.728	-0.178	-0.124	0.712	-0.165
-6	0.000	0.751	-0.249	-0.029	0.736	-0.235	-0.057	0.722	-0.221	-0.086	0.708	-0.207	-0.113	0.694	-0.193
-7	0.000	0.723	-0.277	-0.026	0.712	-0.262	-0.052	0.700	-0.248	-0.078	0.689	-0.234	-0.104	0.677	-0.219
-8	0.000	0.699	-0.301	-0.023	0.690	-0.287	-0.047	0.680	-0.273	-0.071	0.671	-0.258	-0.094	0.661	-0.244
-9	0.000	0.677	-0.323	-0.021	0.670	-0.309	-0.042	0.662	-0.295	-0.064	0.655	-0.281	-0.086	0.647	-0.267
-10	0.000	0.658	-0.342	-0.019	0.652	-0.329	-0.038	0.646	-0.316	-0.058	0.640	-0.302	-0.078	0.633	-0.289