PCI-SIG® Compliance Workshop #133
February 18-21, 2025
Taipei Marriott Hotel
Taipei, Taiwan

Please read carefully for registration information and the details.
Please come prepared.

When

The PCI-SIG Compliance Workshop #133 will be held February 18-21, 2025. The registration deadline is **12 pm (PT) on Thursday, January 16th, 2025**. **The Hotel Reservation deadline is Monday January 20, 2025. Hotel rooms under the discounted rate are on a first come, first serve basis.**

Objective

PCI: Compliance Workshops are held to promote PCI Express® specification compliance in the industry with the goals of eliminating interoperability issues and ensuring proper implementation of PCIe specifications.

Member: Participation provides an opportunity to find and fix problems before products release. This saves your company time and resources while offering valuable networking and training opportunities with your fellow engineers.

Products may be added to the PCI-SIG Integrators List by passing the testing requirements at a single compliance workshop **and** submitting a PCI-SIG Integrators List Product Listing Request Form.

How

PCI-SIG schedules compliance test sessions, plus private test sessions between Add-in Card and System vendors for testing. PCI-SIG also provides technical consultants to assist in testing and fault analysis. **Engineers must accompany all products tested.**

What Technologies Will Be Tested

PCI Express 5.0 – Official Testing
PCI Express 5.0 Retimer – Official Testing
PCI Express 4.0 – Official Testing
PCI Express 4.0 Retimer – Official Testing
PCI Express U.2®/SFF-8639/ (8 GT/s) – Official Testing

Please find detailed information about the testing conducted at a Compliance Workshop in the PCIe Workshop Testing Summary.

PCI Express 5.0 Official Testing: The PCI-SIG will be offering official testing for PCIe 5.0 at 32 GT/s for both add-in cards and systems. You must provide a separate device and attendee to conduct the PCIe 5.0 testing for each product you register.

- **Configuration Space Testing for PCIe 5.0 Systems:** Please be aware that the CV test for systems is mandatory to attend but the result is FYI only.
- **Lane Margining:** Lane Margining testing is mandatory for both PCIe 5.0 Add-In Cards and Systems. For Systems please ensure that your system is setup to run one of the Lane Margining tools at the Compliance Workshop.
- **Please note the following component policy for 5.0 official Integrators List testing:**
  PCI-SIG Integrators List testing for CEM devices is performed at the PCI Express connector, and AICs or System boards that pass can be added to the Integrators List. Vendors that wish to place the corresponding component onto the Integrators List based on that passing result, must certify to PCI-SIG that the electrical interface exposed at the CEM connector is the electrical interface of that component. Note that devices such as Redrivers or Retimers when present between the component and the CEM connector prevent the full electrical and functional testing of the component itself, and therefore while such an AIC or System board may achieve a passing result (and be placed on the Integrators List as an AIC or System), the component itself has not achieved a passing result and therefore cannot be placed on the Integrators List as a Component unless specifically tested.

PCI Express 5.0 Testing for Retimers: PCI-SIG will offer official testing of PCIe 5.0 Retimers. The PCIe 5.0 Retimer testing includes electrical and protocol testing per the applicable PCI Express 5.0 Test Specifications. The Retimer vendor can provide a CEM based adapter board for use in Add-In Card and System testing or must provide a short channel silicon evaluation board and necessary adapters to SMA test equipment connections.

Since Retimers are tested as both upstream port and downstream port two registrations are required for Retimers one as an Add-In Card and one as a System. It is required that the Retimer vendor bring their own system and Add-In Card. Note: PCI-SIG will NOT provide a system or Add-In Card for testing.

PCI Express 4.0 Official Testing: The PCI-SIG will be offering official testing for PCIe 4.0 at 16 GT/s for both add-in cards and systems. You must provide a separate device and attendee to conduct the PCIe 4.0 testing for each product you register.

- **Lane Margining:** Please be aware that the Lane Margining test that was conducted at previous FYI workshops will remain an FYI test for 4.0 Integrators List testing.
- **Please note the following component policy for 4.0 official Integrators List testing:** PCI-SIG Integrators List testing for CEM devices is performed at the PCI Express connector, and AICs or System boards that pass can be added to the Integrators List. Vendors that wish to place the corresponding component onto the Integrators List based on that passing result, must certify to PCI-SIG that the electrical interface exposed at the CEM connector is the electrical interface of that component. Note that devices such as Redrivers or Retimers when present between the component and the CEM connector prevent the full electrical and functional testing of the component itself, and therefore while such an AIC or System board may achieve a passing result (and be placed on the Integrators List as an AIC or System), the component itself has not achieved a passing result and therefore cannot be placed on the Integrators List as a Component unless specifically tested.

PCI Express 4.0 Testing for Retimers: PCI-SIG will also offer official testing of PCIe 4.0 Retimers. The PCIe 4.0 Retimer testing includes electrical and protocol testing per the applicable PCI Express 4.0 Test Specifications. The Retimer vendor can provide a CEM based adapter board for use in Add-In Card and System testing or must provide a short channel silicon evaluation board and necessary adapters to SMA test equipment connections.

Since Retimers are tested as both upstream port and downstream port two registrations are required for Retimers one as an Add-In Card and one as a System.

PCI Express U.2/SFF-8639 (8 GT/s) Testing: If you would like your device listed as **both** CEM and U.2, on the Integrators List, please ensure that you register *TWO* instances of your device – one for the SFF-8639/ PCI Express U.2 testing, and one for the CEM form factor (bringing your own adapter for CEM).

SFF-8639/PCI Express U.2 Cards must be registered separately from CEM based Cards. Please note that one person cannot escort both SFF-8639/PCI Express U.2 Cards and CEM based cards, you will need to register an additional attendee to manage the additional testing schedule. Please see the registration restrictions in the “How to Register” section.

Cost

Attendance at this **Members Only** event is free. If you do not bring your product to the event or your product registration is not canceled by 12 **pm (PT) on Thursday, January 16th, 2025** you may be charged a $250 no show fee.

This event is non-hosted. Participants pay for their own travel, food, and hotel expenses. Lunch is provided for attendees Tuesday through Friday.

Where

Taipei Marriott Hotel
No. 199號, Lequn 2nd Rd,
Zhongshan District, Taipei City, Taiwan 10491

Shipping Instructions

Please ensure your shipment does not arrive at the hotel prior to **Friday, February 14th 2025**. If you would like to ship items to the hotel, **please ensure you complete the group package delivery form and send to the contact information provided on the form. Please note that shipping to the hotel is only available to those staying at the hotel.**

Ship to: Marriott Taipei- No. 199號, Lequn 2nd Rd, Zhongshan District, Taipei City, Taiwan 10462
Tel: +886 2-8502 9999, Fax: +886 2-8502 6866
Attn: Hold for (Your name / Your company name / Tel.) / February 18-21, 2025 PCI-SIG / Charlie Liao

Hotel Reservations – Reserve your room early!

*Reservations cut-off date is **Monday, January 20, 2025**.To ensure the group rate is applied and the hotel has rooms available please make your reservations as soon as possible. Hotel rooms under the discounted rate are on a first come, first serve basis.

When making a hotel reservation, please use our group specific page: https://www.marriott.com/event-reservations/reservation-link.mi?id=1732766605117&key=GRP&guestreslink2=true&app=resvlink

HOW TO REGISTER

I. EVENT REGISTRATION

- All Attendees MUST accompany a co-worker who is registered to test equipment.
- Online Registration – https://pcisig.com/events/pci-sig-compliance-workshop-133
- Online registration ends at **12:00pm PT on Thursday, January 16 2025.**

II. SLEEPING ROOM RESERVATIONS

- Instructions are found above.
- ***NOTE: A testing room must be reserved by the System vendor company to participate. The room reservation must check in on Monday, February 17th with a checkout of Friday, February 21st , 2025.***

III. ON-SITE CHECK-IN

- Name badges and test schedules will be distributed on the first day of the event from 8:00-8:45am (subject to change) outside the PCI-SIG Hospitality Suite. An email will be sent to all attendees if schedule and name badge pick up time has changed.

PCI-SIG Compliance Workshop Test Syllabus

One-on-One Test Sessions

PCI-SIG Compliance Workshops include one-on-one private 15 minute to one-hour test sessions between an Add-in Card vendor and a System vendor. System vendors and Add-in Card vendors will test their products in as many combinations as time and capabilities permit. The results of these test sessions are recorded and will be used as one of the elements in determining PCI-SIG compliance.

The one-on-one test sessions are held in hotel suites as reserved by the System vendors (Add-in Card vendors travel to the system vendor suites). The privacy of these sessions promotes willingness to test products that may not be fully "market ready." Additionally, vendors are able to establish contacts which enable a strong PCI Engineering community and encourage future cooperation for debugging and development.

Add-In Card Test Session

PCI-SIG hosts staffed compliance test suites to test PCI Add-in Cards using test software and hardware to provide extensive testing for compliance against specific aspects of the appropriate PCI-SIG specification. Add-in Card vendors will be scheduled to visit each applicable compliance test suite during the compliance one-on-one test sessions. Results will be recorded and used as one of the elements in determining PCI-SIG compliance.

System Test Sessions

PCI-SIG hosts staffed compliance test suites for testing System products. Commercially available PCI-SIG test cards and test software serve as the test platform for extensive testing for specific aspects of the system environment. System vendors will need to roam to the PCI-SIG approved test suite for compliance test sessions.

Integrators List Policy

Products that pass 80% of one-on-one interoperability test sessions, pass all appropriate PCI-SIG compliance tests, **and** submit the Product Listing Request Form, may be listed on a PCI-SIG Integrators List. The Integrators List is used by a number of PCI-SIG companies to make product purchase decisions. When submitting the Product Listing Request Form, only one product will be listed per product tested at a PCI-SIG Compliance Workshop. A product may be submitted at any point following the workshop where the product was tested, there is no deadline.

Questions?

If you have any questions, please contact PCI-SIG at Tel. (503) 619-0569 or Fax (503) 644-6708 or e-mail PCI-SIG Administration at compliance@pcisig.com.

Thank you,

Reen Presnell
Executive Director
PCI-SIG