PCI-SIG® 2019 Update

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Vice President and Developers
Conference Chair
PCI-SIG® DevCon Key Updates

- PCI-SIG Overview
- PCI Express® Roadmap
- PCI Express in Taipei
PCI-SIG® Snapshot

Organization that defines the PCI Express® (PCIe®) I/O bus specifications and related form factors.

800+ member companies located worldwide.

Creating specifications and mechanisms to support compliance and interoperability.

PCI-SIG member companies support the following industries:

- Virtual reality
- Automotive
- Artificial intelligence
- Enterprise Servers
- Cloud
- Storage
- PC / Mobile / IoT
One Interconnect – Infinite Applications

**Artificial Intelligence**
- High-performance
- High-bandwidth

**Automotive**
- High-performance
- Reliability
- Availability
- Serviceability

**Cloud**
- Scalable architecture
- Increased performance
- Reduced TCO

**Enterprise Servers**
- Redundancy/failover
- Ubiquity
- Power savings

**PC/Mobile/IoT**
- Faster performance
- Power efficiency
- Low latency

**Storage**
- Faster data transfer
- Better user experience
- Ubiquity
PCI-SIG® Roadmap

I/O BANDWIDTH DOUBLES EVERY 3 YEARS

- 0.13 GB/s (PCI 2.0) in 1992
- 0.26 GB/s (PCI-X 2.0) in 1995
- 0.5 GB/s (PCI 2.0) in 1998
- 1.06 GB/s (PCI-X 2.0) in 2001
- 4.2 GB/s (PCI 2.0) in 2004
- 8 GB/s (PCI 2.0) in 2007
- 16 GB/s (PCI 2.0) in 2010
- 32 GB/s (PCI 2.0) in 2013
- 64 GB/s (PCI 3.0) in 2016
- 128 GB/s (PCI 4.0) in 2019
- 256 GB/s (PCI 5.0) in 2022
- 256 GB/s (PCI 6.0) in 2025

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Adoption is Well Under Way

• **Key Features:**
  • Delivers 16 GT/s
  • Maintains backward compatibility with PCIe 3.x, 2.x, and 1.x
  • Implements:
    • Extended tags and credits
    • Reduced system latency
    • Lane margining
  • Superior RAS capabilities
  • Scalability for added lanes and bandwidth
  • Improved I/O virtualization and platform integration
  • dB loss is 28dB

• **Compliance Status:**
  • PCI-SIG Launched Official Testing for PCIe 4.0 in 2019
  • Formal Compliance testing targeted for Q3 2019

• **Adoption:**
  • Numerous vendors with 16GT/s PHYs and controllers in silicon
  • Test equipment from multiple vendors available
  • Several member companies have publicly announced & exhibited PCIe 4.0 products
PCI Express® 5.0 Specification & Status

Published in May 2019

- **Key Features:**
  - Delivers 32 GT/s
  - Maintains backward compatibility with PCIe 4.0, 3.x, 2.x, and 1.x
  - dB loss is 36dB
  - Electrical changes to improve signal integrity and mechanical performance of connectors

- **Compliance Status:**
  - PCIe 5.0 compliance testing is under development

- **Adoption**
  - Several member companies have publicly announced and are showcasing PCIe 5.0 solutions
  - Adoption expected to grow in the next 18-24 months due to demand from high performance applications
Targeting completion in 2021; PCIe® 6.0, Version 0.3 released to members in October

- **Key Features:**
  - Doubles bandwidth to 64 GT/s (PCIe 6.0) from 32 GT/s (PCIe 5.0)
  - Implements PAM4 signaling (PCIe 6.0) rather than NRZ (PCIe 5.0)
    - Pulse Amplitude Modulation (PAM) allows PCIe 6.0 technology to pack more bits into the same amount of time on a serial channel
  - Includes low-latency Forward Error Correction (FEC) with additional mechanisms to improve bandwidth efficiency
  - Maintains backward compatibility with all previous generations of PCIe technology
  - Delivers similar channel reach as PCIe 5.0
  - More than two dozen member companies of the PCI-SIG Electrical Work Group attended a Face-to-Face Meeting in May

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### PCI Express® 6.0 Specification Details

<table>
<thead>
<tr>
<th>RAW BIT RATE</th>
<th>LINK BW</th>
<th>BW/LANE/WAY</th>
<th>TOTAL BW X16</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe 6.0</td>
<td>64GT/s</td>
<td>~6BG/s</td>
<td>256GB/s</td>
</tr>
<tr>
<td>PCIe 5.0</td>
<td>32GT/s</td>
<td>~4GB/s</td>
<td>~128GB/s</td>
</tr>
<tr>
<td>PCIe 4.0</td>
<td>16GT/s</td>
<td>~2GB/s</td>
<td>~64GB/s</td>
</tr>
<tr>
<td>PCIe 3.x</td>
<td>8.0GT/s</td>
<td>~1GB/s</td>
<td>~32GB/s</td>
</tr>
<tr>
<td>PCIe 2.x</td>
<td>5GT/s</td>
<td>500MB/s</td>
<td>16GB/s</td>
</tr>
<tr>
<td>PCIe 1.x</td>
<td>2.5GT/s</td>
<td>250MB/s</td>
<td>8GB/s</td>
</tr>
</tbody>
</table>
Taiwan is a leader in manufacturing PCIe-enabled technology

40% of PCI-SIG® member companies are based in Asia, highlighting the strength of PCI-SIG in APAC

Throughout APAC, PCIe is the nearly ubiquitous interconnect technology ecosystem, enabling storage, mobile, cloud, AI/ML and automotive, and more
Summary

- PCIe® technology delivers one interconnect for infinite applications
  - PCIe 4.0 formal compliance testing targeted for August 2019 and adoption is accelerating and the ecosystem is complete and robust
  - PCIe 5.0 specification published in May 2019 and compliance testing is under development
  - PCIe 6.0 doubles bandwidth again to 64 GT/s; targeted for publication in 2021

- Meets performance and user requirements for current and future applications in performance demanding markets like IoT, AI/ML and automotive. Taipei-based companies are leading the PCIe technology development in these markets

- PCI-SIG continues to maintain its leadership position in delivering high-performance, low power I/O
Back-Up Slides
NVM Express™ Driving PCIe® SSDs in the Data Center

- Data explosion is driving SSD adoption
  - SSD market CAGR of 14.8% during 2016-2021  
    \( \text{Source: } \text{IDC} \)
  - PCIe SSD market to surpass a CAGR of 33% during 2016-2020  
    \( \text{Source: } \text{Technavio} \)
- PCIe adoption is accelerating

Source: SSD Insights Q1/18, Forward Insights

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## Design for a Range of Objectives

<table>
<thead>
<tr>
<th>Low Power</th>
<th>Server Performance</th>
<th>High Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>M.2</td>
<td>U.2</td>
<td>CEM Add-in-card</td>
</tr>
</tbody>
</table>

**PCle® Form Factors**

- **M.2**: 42, 80, and 110mm lengths, smallest footprint of PCIe connector form factors, use for boot, for max storage density, for PXI/AXIe ecosystem.
- **U.2**: 2.5in makes up the majority of SSDs sold today because of ease of deployment, hotplug, serviceability, and small form factor Single-Port x4 or Dual-Port x2.
- **CEM Add-in-card**: Add-in-card (AIC) has maximum system compatibility with existing servers and most reliable compliance program. Higher power envelope, and options for height and length.
PCle® in Automotive

- Distributed ECUs with point-to-point links transitioning to centralized compute architectures

- Exploding bandwidth requirement
  - Video resolution: From 720p to 4K+
  - Displays: From 3 to 8+
  - Sensor nodes: From 4 to 12+
  - RADAR (RAdio Detection and Ranging) / LIDAR (LIght Detection And Ranging)

- PCle as Multi-Gigabit connectivity bus
  - SoC-to-SoC : ADAS (Advanced Driver Assistance Systems), IVI (In-vehicle Infotainment)
  - SoC-to-sensor, SoC-to-I/O connectivity

Source: TI Whitepaper Vision Enabled Automotive Technologies

Source: Delphi, Astera Labs
PCle® in IoT

- Data deluge from IoT driving intelligence and processing to the *Edge*
  - 45% of IoT data processed at edge* by 2020

- Industrial PCs or COM (Computer-on-Module) Express module form-factor
  - COM express Type 7 : 32 lanes, PCIe Gen 3.0
  - Proposed COM-HD : 64 lanes, PCIe Gen 5.0

- PCIe as Multi-Gigabit connectivity bus
  - IO expansion for CPUs
  - Interconnect between data processors (CPU/FPGA/Accelerators/SoC)
  - Storage (NVMe) connectivity

*IDC
PCle® in Machine Learning and AI

- **Computation-intensive workloads demand data-centric system design**
  - Big data analytics growing at 11.9% CAGR
  - AI and ML key drivers

- **Heterogeneous computing and workload-optimized platforms redefining connectivity backbone in servers**
  - PCIe 5.0 delivers 32 GT/sec bandwidth
  - Alternate protocol support included in PCIe 5.0

- **PCle as Multi-Gigabit connectivity bus**
  - Processor-to-Processor interconnect
  - Processor I/O expansion
  - Storage (NVMe) connectivity

*IDC