PCI-SIG® 2019 Update

Richard Solomon

Vice President and Developers Conference Chair

PCI-SIG® DevCon Key Updates

- PCI-SIG Overview
- PCI Express® Roadmap
- PCI Express in Taipei

PCI-SIG® Snapshot

Organization that **defines the PCI Express® (PCIe®) I/O bus specifications and related form factors.**

800+ member companies located worldwide.

Creating specifications and mechanisms to **support compliance** and **interoperability.**

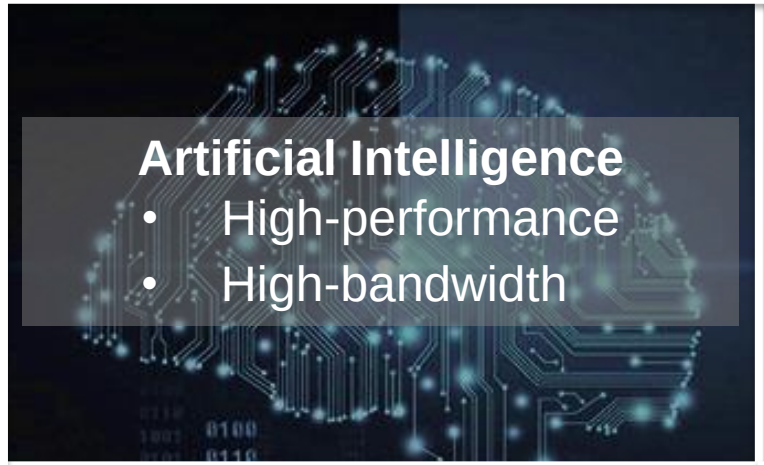
PCI-SIG member companies support the following industries:

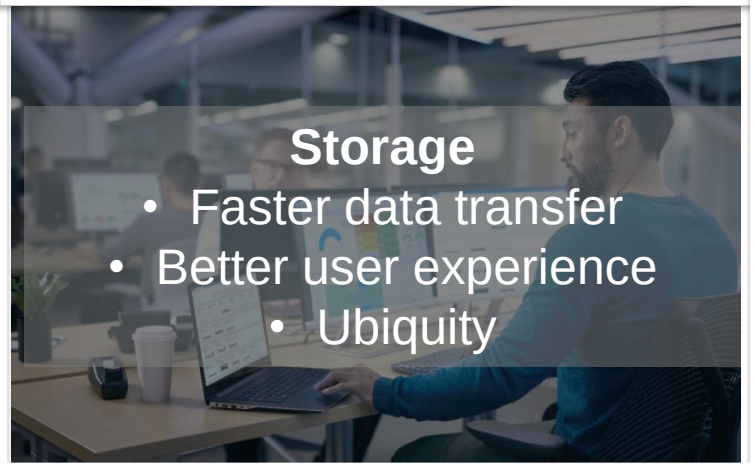
- Virtual reality
- Automotive
- Artificial intelligence
- Enterprise Servers
- Cloud
- Storage
- PC / Mobile / IoT

Board of Directors
2019 – 2020

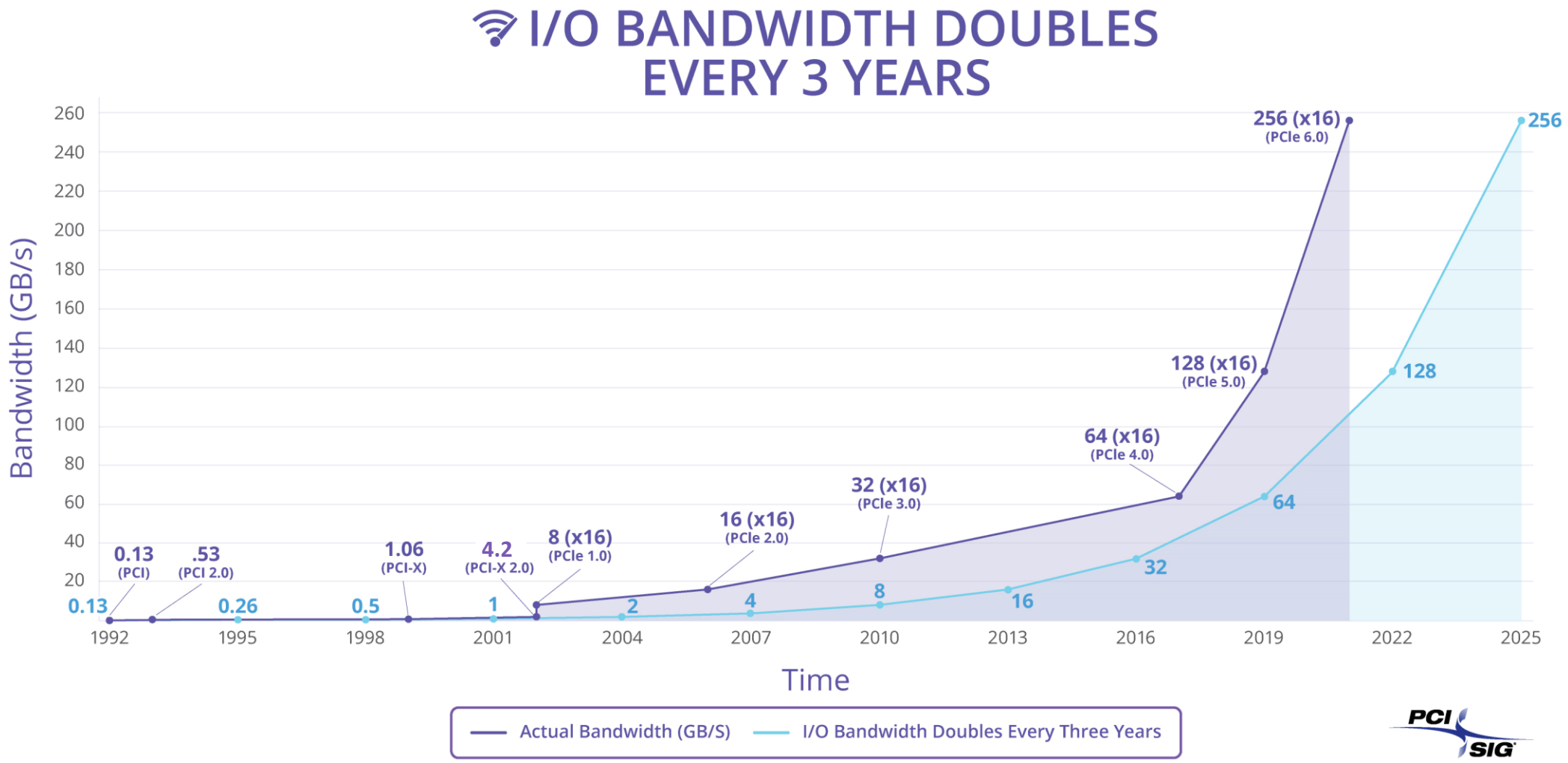
AMD
arm
DELL EMC
IBM
intel
KEYSIGHT TECHNOLOGIES
NVIDIA
Qualcomm
SYNOPSYS
Silicon to Software

One Interconnect – Infinite Applications





PCI-SIG® Roadmap



PCI Express® 4.0 Specification & Status

Adoption is Well Under Way

- **Key Features:**
  - Delivers 16 GT/s
  - Maintains backward compatibility with PCIe 3.x, 2.x, and 1.x
  - Implements:
    - Extended tags and credits
    - Reduced system latency
    - Lane margining
  - Superior RAS capabilities
  - Scalability for added lanes and bandwidth
  - Improved I/O virtualization and platform integration
  - dB loss is 28dB
- **Compliance Status:**
  - PCI-SIG Launched Official Testing for PCIe 4.0 in 2019
  - Formal Compliance testing targeted for Q3 2019
- **Adoption:**
  - Numerous vendors with 16GT/s PHYs and controllers in silicon
  - Test equipment from multiple vendors available
  - Several member companies have publicly announced & exhibited PCIe 4.0 products

PCI Express® 5.0 Specification & Status

Published in May 2019

- **Key Features:**
  - Delivers 32 GT/s
  - Maintains backward compatibility with PCIe 4.0, 3.x, 2.x, and 1.x
  - dB loss is 36dB
  - Electrical changes to improve signal integrity and mechanical performance of connectors
- **Compliance Status:**
  - PCIe 5.0 compliance testing is under development
- **Adoption**
  - Several member companies have publicly announced and are showcasing PCIe 5.0 solutions
  - Adoption expected to grow in the next 18-24 months due to demand from high performance applications

PCI Express® 6.0 Specification Details

Targeting completion in 2021; PCIe® 6.0, Version 0.3 released to members in October

- **Key Features:**
  - Doubles bandwidth to 64 GT/s (PCIe 6.0) from 32 GT/s (PCIe 5.0)
  - Implements PAM4 signaling (PCIe 6.0) rather than NRZ (PCIe 5.0)
    - Pulse Amplitude Modulation (PAM) allows PCIe 6.0 technology to pack more bits into the same amount of time on a serial channel
  - Includes low-latency Forward Error Correction (FEC) with additional mechanisms to improve bandwidth efficiency
  - Maintains backward compatibility with all previous generations of PCIe technology
  - Delivers similar channel reach as PCIe 5.0
  - More than two dozen member companies of the PCI-SIG Electrical Work Group attended a Face-to-Face Meeting in May

	RAW BIT RATE	LINK BW	BW/ LANE/WAY	TOTAL BW X16
PCIe 6.0	64GT/s	64GB/s	~6BG/s	256GB/s
PCIe 5.0	32GT/s	32Gb/s	~4GB/s	~128GB/s
PCIe 4.0	16GT/s	16Gb/s	~2GB/s	~64GB/s
PCIe 3.x	8.0GT/s	8Gb/s	~1GB/s	~32GB/s
PCIe 2.x	5GT/s	4Gb/s	500MB/s	16GB/s
PCIe 1.x	2.5GT/s	2Gb/s	250MB/s	8GB/s

PCIe® Technology in Taipei

- Taiwan is a leader in manufacturing PCIe-enabled technology
- 40% of PCI-SIG® member companies are based in Asia, highlighting the strength of PCI-SIG in APAC
- Throughout APAC, PCIe is the nearly ubiquitous interconnect technology ecosystem, enabling storage, mobile, cloud, AI/ML and automotive, and more

2020 PCI-SIG® APAC DevCon Sponsors

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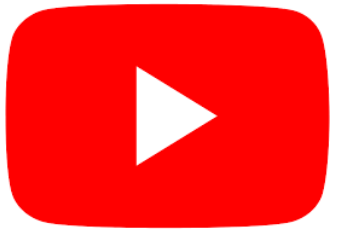
Summary

- PCIe® technology delivers one interconnect for infinite applications
  - PCIe 4.0 formal compliance testing targeted for August 2019 and adoption is accelerating and the ecosystem is complete and robust
  - PCIe 5.0 specification published in May 2019 and compliance testing is under development
  - PCIe 6.0 doubles bandwidth again to 64 GT/s; targeted for publication in 2021
- Meets performance and user requirements for current and future applications in performance demanding markets like IoT, AI/ML and automotive. Taipei-based companies are leading the PCIe technology development in these markets
- PCI-SIG continues to maintain its leadership position in delivering high-performance, low power I/O

Engage with PCI-SIG® on Social Media

@PCI_SIG

https://www.linkedin.com/company/pcisig/

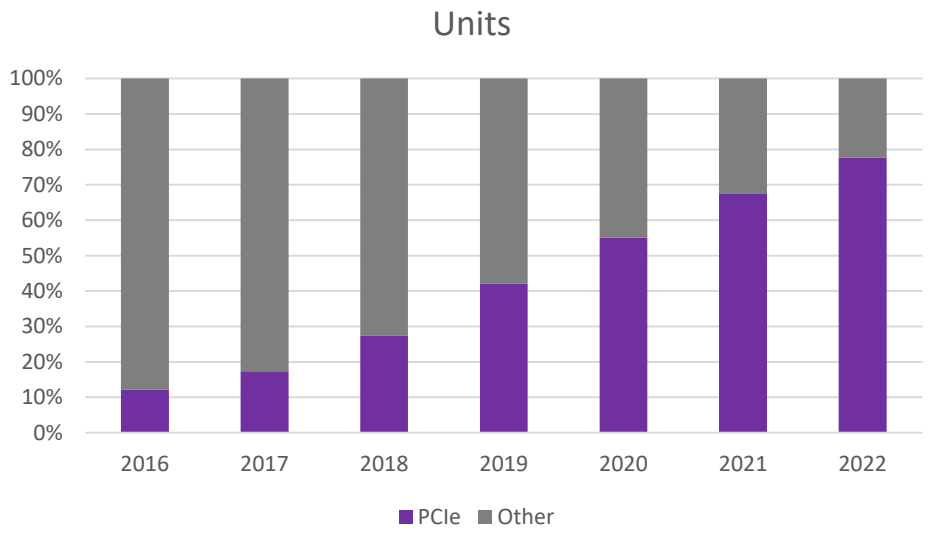


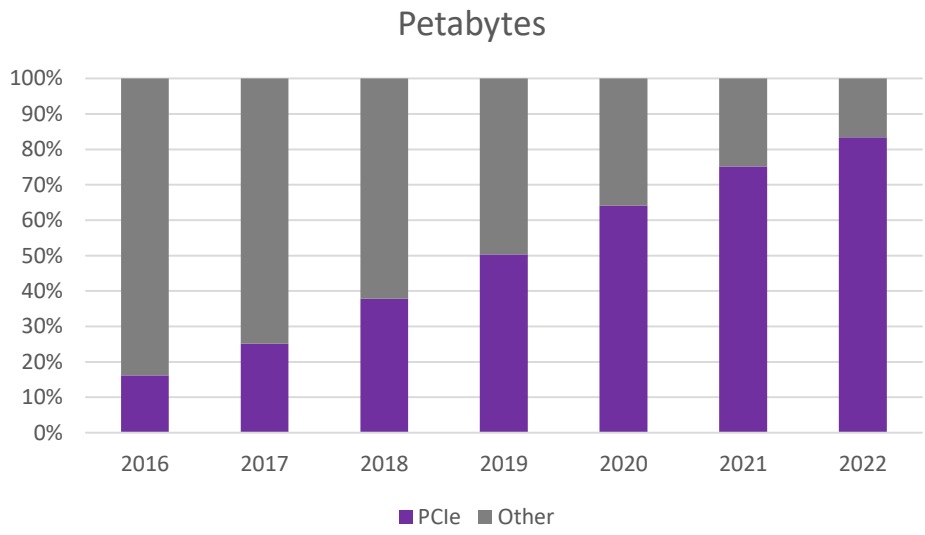
PCI-SIG

Back-Up Slides

NVM Express™ Driving PCIe® SSDs in the Data Center

- Data explosion is driving SSD adoption
  - SSD market CAGR of 14.8% during 2016-2021 *Source*: IDC
  - PCIe SSD market to surpass a CAGR of 33% during 2016-2020 *Source*: Technavio
- PCIe adoption is accelerating

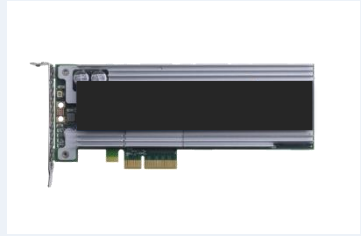




Source: SSD Insights Q1/18, Forward Insights

Official PCI Express® Form Factors

Design for a Range of Objectives

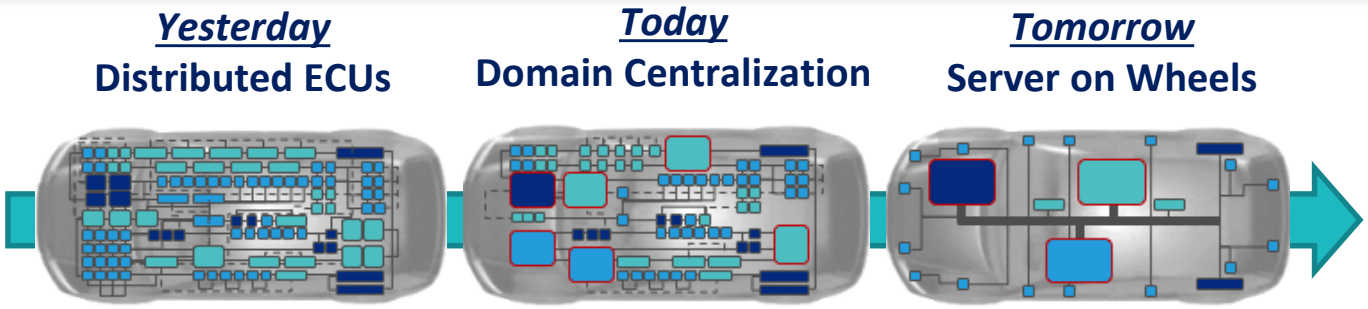
	Low Power	Server Performance	High Performance
PCIe® Form Factors	**M.2**	**U.2**	**CEM Add-in-card**
			
	42, 80, and 110mm lengths, smallest footprint of PCIe connector form factors, use for boot, for max storage density, for PXI/AXIe ecosystem	2.5in makes up the majority of SSDs sold today because of ease of deployment, hotplug, serviceability, and small form factor Single-Port x4 or Dual-Port x2	Add-in-card (AIC) has maximum system compatibility with existing servers and most reliable compliance program. Higher power envelope, and options for height and length

PCIe® in Automotive

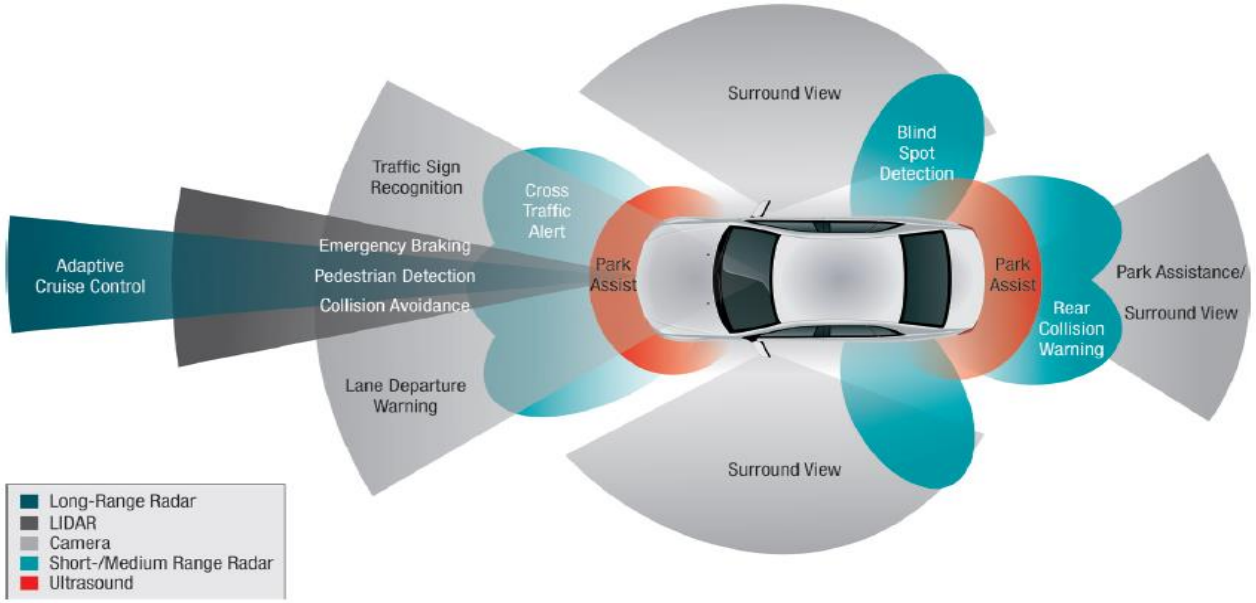
- **Distributed ECUs with point-to-point links transitioning to centralized compute architectures**

- **Exploding bandwidth requirement**
  - Video resolution: From 720p to 4K+
  - Displays: From 3 to 8+
  - Sensor nodes: From 4 to 12+
  - RADAR (RAdio Detection and Ranging) / LIDAR (LIght Detection And Ranging)

- **PCIe as Multi-Gigabit connectivity bus**
  - SoC-to-SoC : ADAS (Advanced Driver Assistance Systems), IVI (In-vehicle Infotainment)
  - SoC-to-sensor, SoC-to-I/O connectivity



Source: Delphi, Astera Labs

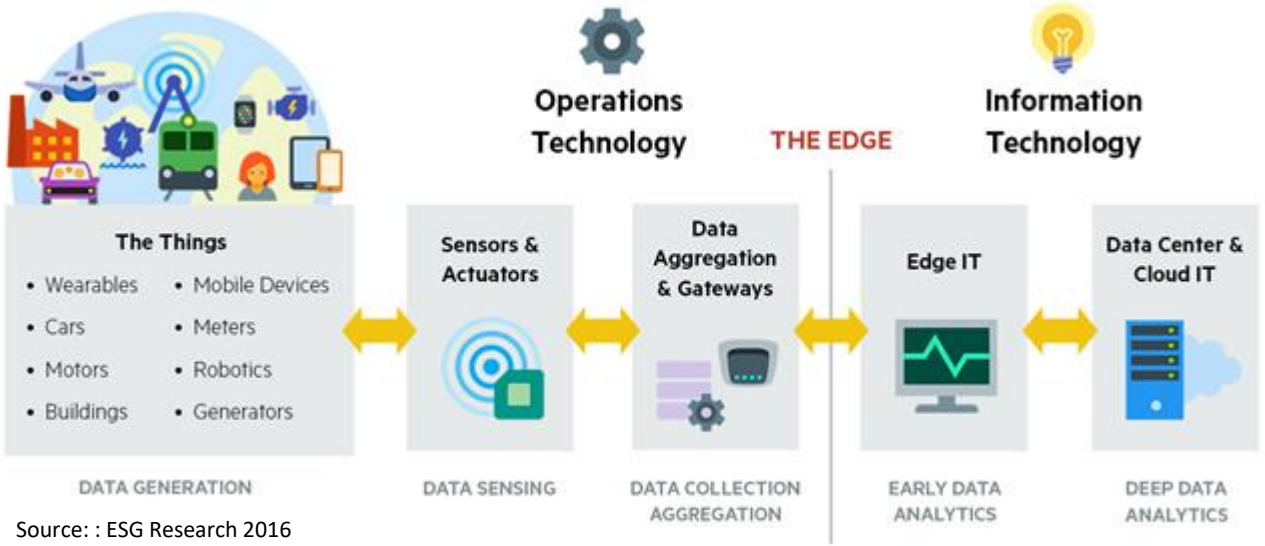


Source: TI Whitepaper Vision Enabled Automotive Technologies

PCIe® in IoT

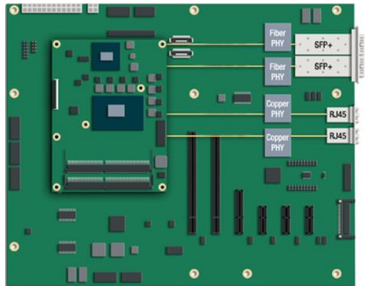
- **Data deluge from IoT driving intelligence and processing to the *Edge***
  - 45% of IoT data processed at edge* by 2020
- **Industrial PCs or COM (Computer-on-Module) Express module form-factor**
  - COM express Type 7 : 32 lanes, PCIe Gen 3.0
  - Proposed COM-HD : 64 lanes, PCIe Gen 5.0
- **PCIe as Multi-Gigabit connectivity bus**
  - IO expansion for CPUs
  - Interconnect between data processors (CPU/FPGA/Accelerators/SoC)
  - Storage (NVMe) connectivity

*IDC



Source: : ESG Research 2016

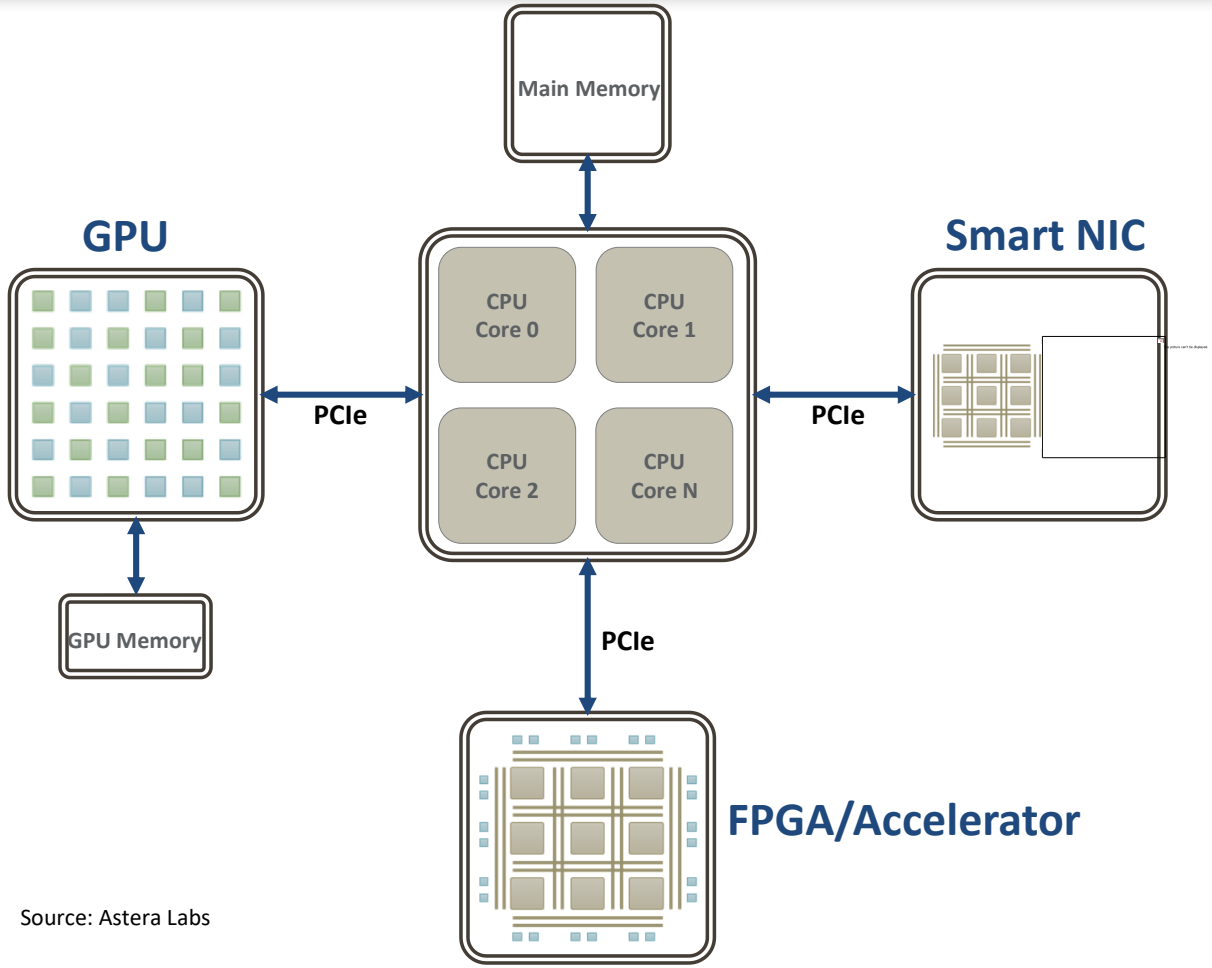
Industrial PCs



COM (Computer-on-Module) Express

PCIe® in Machine Learning and AI

- **Computation-intensive workloads demand data-centric system design**
  - Big data analytics growing at 11.9% CAGR*
  - AI and ML key drivers
- **Heterogeneous computing and workload-optimized platforms redefining connectivity backbone in servers**
  - PCIe 5.0 delivers 32 GT/sec bandwidth
  - Alternate protocol support included in PCIe 5.0
- **PCIe as Multi-Gigabit connectivity bus**
  - Processor-to-Processor interconnect
  - Processor I/O expansion
  - Storage (NVMe) connectivity



Source: Astera Labs

*IDC