PCIe® 5.0 Protocol and Electrical Compliance Testing Deep Dive

PCI-SIG® Educational Webinar Series

Presented by
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Speakers

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Agenda

Part 1: PCI Express® 5.0 Protocol Compliance Testing

- Compliance Test Overview and New Features
- Form Factors
- Link and Transaction Layer Tests
- Lane Margining Testing

Part 2: PCIe® 5.0 Electrical Compliance Testing

- Electrical Compliance Test Overview
- Test Procedures and Details:
  - Transmitter Electrical
  - Transmitter Link Equalization
  - Receiver Link Equalization
  - PLL Bandwidth
  - Reference Clock Jitter

Part 1: PCIe® 5.0 Protocol Compliance

WHAT IS COMPLIANCE?

PCI Express® Compliance Test overview

Test name	Notes
Lane Margining Tests	Protocol Test runs on Protocol Exerciser
Link Layer Tests	Protocol Exerciser
Transaction Layer Tests	Protocol Exerciser
Configuration Space Tests (PCIECV)	Runs on PC
Transmitter Signal Quality	Automated using SigTest Phoenix
Transmitter Jitter (Pulse Width Jitter)	Automated using SigTest Phoenix
Transmitter Preset	Automated using SigTest Phoenix
Transmitter Initial Tx Equalization	Add-in card only
Transmitter Link Equalization response	
Receiver Link Equalization	
PLL Bandwidth	Add-in card only
Reference Clock Jitter	System only - new for PCIe® 5.0 compliance
PCB Impedance	Informative only – VNA test

(PCI Express 5.0 PHY test spec, Rev 0.9)

What is PCIe® Compliance?

Definition

Compliance means that a product meets the standards set forth by the PCI-SIG® in its PCI Express® Test Specifications

Compliance Program

The PCI-SIG Compliance Workshops host interoperability and compliance tests

- Interoperability tests enable members to test their products against other members' products
- Compliance tests allow for product testing against the five PCI-SIG test areas
- Both testing types issue "pass" or "fail" results for each test area examined. To formally label products as compliant, they must score a minimum of 80 percent on interoperability tests and pass all required compliance tests

Source: PCI-SIG

Goal: System Integrators List

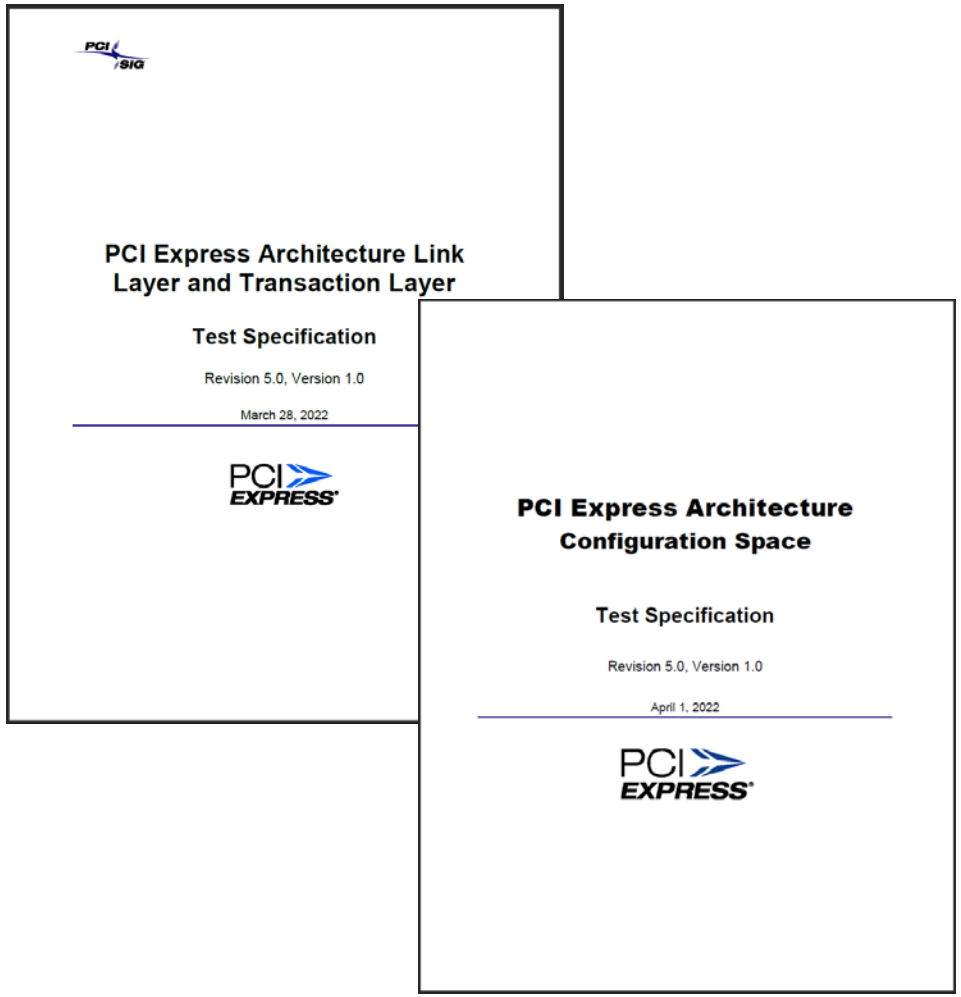
Integrators List

- Another valuable benefit of the Compliance Program is inclusion on the PCI-SIG® Integrators List
- This list includes all products that have successfully completed the rigorous testing procedures of the Compliance Workshop.
- Inclusion on the list is only available to PCI-SIG member companies and cannot be used for individual marketing programs

Source: PCI-SIG

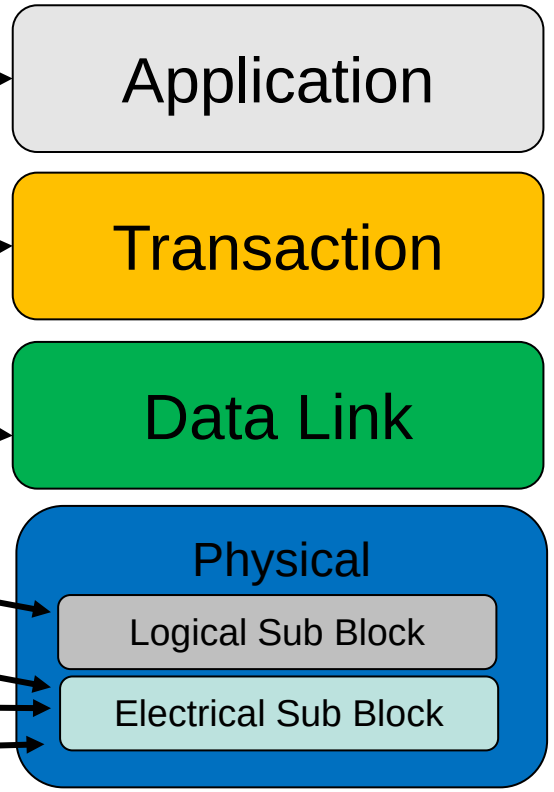
PCI Express® 5.0 Compliance Testing

- PCI-SIG® Serial Enabling Workgroup defines tests
- Test specifications are available from PCI-SIG website
- Preliminary PCIe® 5.0 Testing started at February 2021 Interoperability event
- Official PCIe 5.0 Testing started at the April 2022 workshop
- Electrical Testing requires new test fixtures
- Link and Transaction layer protocol testing uses Exerciser/Analyzer – same concept as PCIe 4.0 testing
- Lane Margining test now mandatory for PCIe 5.0 testing



PCI-SIG® Compliance Testing

- How does this fit into the layered model?
- Compliance testing is split out into sections:
  - Configuration Space
    - Using PCIECV tool from PCI-SIG
  - Link and Transaction Layer
    - Transaction Layer testing
    - Data Link Layer testing
    - Testing Link Training
    - Lane Margining Test
  - Electrical
    - Link Equalization/De-emphasis testing
    - Transmitter Signal Quality
    - Receiver Jitter Tolerance
  - Note: BIOS Testing was discontinued from PCIe® 4.0 specification onwards



PCIe® 5.0 Configuration (CV) and Link/Transaction Layer

- Link/Transaction Layer Tests
  - Add-In card test suite is complete and available
  - No System testing for Link/Transaction Layer
- Lane Margining Tests Add In Cards (No Device Driver) – Test included with Link/Transaction
  - Add In Cards (Device Driver) – Test run using Lane Margining Tool
  - Systems – Test run using Lane Margining Tool
- PCIe 5.0 Config Tests
  - Preliminary FYI began at Interoperability Workshop in February 2021

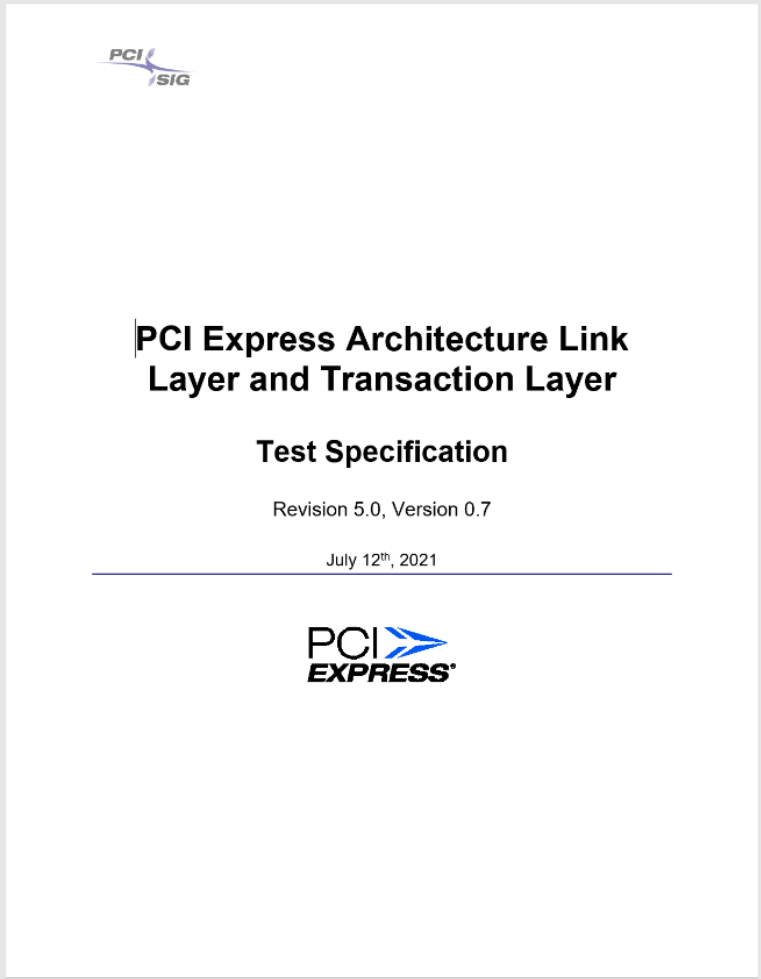
PCI Express® 5.0 Specification

LINK AND TRANSACTION LAYER TESTS

4/27/2023

Link and Transaction Layer

- What are the Link/Transaction tests?
  - Link Layer Tests
  - Transaction Layer Tests
  - Logical PHY layer tests (Equalization Protocol)
  - Logical PHY layer tests (Reserved Bits in TS)
  - Lane Margining Test – Functional test
  - Precoding Test
- Which conditions are being tested?
  - Error handling at each layer
  - Validation that capability is implemented



PCI Express Architecture Link Layer and Transaction Layer

Test Specification

Revision 5.0, Version 0.7

July 12th, 2021

Link Layer Tests

- Link Layer Tests have been run since PCIe® 1.0a specification
- Test Link Layer mechanisms
  - Replay Timer/Replay Number/Replay on NAK
  - Bad DLLP's
  - Replay Counter
  - Bad LCRC
  - AER Reporting of Errors

	Test Name	Test Reference on Teledyne LeCroy Test Suite	Test Reference in Test Spec
3.1.1	ReservedFieldsDLLPReceive	Link_41-20_ReservedFieldsDLLPReceive	41-20
3.2.1	ReTransmitonNAK	Link_52-10_RetransmitOnNak	52-10
3.2.2	ReplayTimerTest	Link_52-11_REPLAY_TIMER	52-11
3.2.3	ReplayNumTest	Link_52-12_REPLAY_NUM	52-12
3.2.4	LinkRetrainOnRetryFail	Link_52-20_LinkRetrainOnRetryFail	52-20
3.2.5	ReplayTLPOrder	Link_52-100_ReplayTLPOrder	52-100
3.2.6	CorruptedDLLP	Link_52-150_CorruptedCRC_DLLP	52-150
3.2.7	UndefinedDLLPEncoding	Link_52-160_UndefinedDLLPEncoding	52-160
3.2.8	WrongSeqNumberInACKDLLP	Link_52-170_WrongSeqNumInAckDLLP	52-170
3.3.1	BadLCRC	Link_53-20_BadLCRC	53-20
3.3.2	DuplicateTLPSeqNum	Link_53-31_DuplicateTLP	53-31

Example Link Layer Test – 53-20 Bad LCRC

Example log file from LinkExpert:

Test Description

Verification of each stage

PASS or FAIL result

```
Run test: Link 53-20 BadLCRC
Executing stimulus: C:\Users\Public\Documents\LeCroy\PCIe Protocol
Suite\ScriptAutomationTestTool\TrainerScripts\Endpoint\LinkLayer\link_53-20_BadLCRC.peg
Trace captured - starting Verification

-----------------------------------------------------------------------------
C:\Users\Public\Documents\LeCroy\PCIe Protocol
Suite\ScriptAutomationTestTool\VerificationScripts\Endpoint\LinkLayer\link_53-20_BadLCRC.pevs
-----------------------------------------------------------------------------


Running verification script...
...

Test Description :
PE Compliance, Link Layer Test 53-20 - BadLCRC.
The intent of this test is to verify that a receiver discards a TLP with bad CRC by NAKing it and
reports a BAD TLP error associated with the port.


ASSERTIONS COVERED: DLL.5.3#2
Testing Link Layer 53-20 - BadLCRC.

Verifying test stage 1 (Enabling Error Reporting).
Verifying test stage 2 (Clearing Advanced Uncorrectable Error bits).
Verifying test stage 3 (Clearing Advanced Correctable Error bits).
Verifying test stage 4 (sending Cfg Read with bad LCRC).
Verifying test stage 5 (Reading Device Status Register).
Verifying test stage 6 (Reading Advanced Uncorrectable Error Status).
Verifying test stage 7 (Reading Advanced Correctable Error Status).
Verifying test stage 8 (Disabling Error Reporting).
Verifying test stage 9 (Not Enabling Error Reporting).
Verifying test stage 10(Clearing Advanced Uncorrectable Error bits).
Verifying test stage 11(Clearing Advanced Correctable Error bits).
Verifying test stage 12(sending Cfg Read with bad LCRC, error reporting disabled).
Verifying test stage 13(Reading Device Status Register).
Verifying test stage 14(Reading Advanced Uncorrectable Error Status).
Verifying test stage 15(Reading Advanced Correctable Error Status).
Verifying test stage 16(Disabling Error Reporting).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Example Link Layer Test – 53-20 Bad LCRC

PTC/Exerciser Injects LCRC error into Config Read TLP

Packet																							
94721	R→	32.0 x1	Packet Error LCRCErr	TLP 3	Cfg	CfgRd0 000:00100	Length 1	RequesterID 000:00:0	Tag 3	DeviceID 001:00:0	Register 0x000	1st BE 1111	LCRC 0x00ABCDEF	Time Delta 488.000 ns	Time Stamp 0001 . 394 888 944 000 s								
94722	R←	32.0 x1	DLLP	NAK	AckNak_Seq_Num 2	CRC 16 0x1A32	Idle 237.930 ns	Time Stamp 0001 . 394 889 432 000 s															
94723	R←	32.0 x1	TLP 3	Msg	Msg 001:10000	Msg Routing To RC	Length 0	RequesterID 001:00:0	Tag 0	Message Code ERR_COR	LCRC 0x975D0D70	592.000 ns	0001 . 394 889 672 000 s										
94724	R→	32.0 x1	DLLP	ACK	AckNak_Seq_Num 3	CRC 16 0x504E	Idle 132.560 us	Time Stamp 0001 . 394 890 264 000 s															
94725	R→	32.0 x1	TLP 3	Cfg	CfgRd0 000:00100	Length 1	RequesterID 000:00:0	Tag 3	DeviceID 001:00:0	Register 0x078	1st BE 1100												
94726	R←	32.0 x1	DLLP	ACK	AckNak_Seq_Num 3	CRC 16 0x504E	Idle 607.930 ns	Time Stamp 0001 . 395 023 298 000 s															
94727	R←	32.0 x1	TLP 4	Cpl	CplID 010:01010	Length 1	Requ 000							Byte Cnt 4	Lwr Addr 0x00	Register Data 0x0011002F	LCRC 0x648E1DF8	Time Delta 592.000 ns	Time Stamp 0001 . 395 023 908 000 s				
94728	R→	32.0 x1	DLLP	ACK	AckNak_Seq_Num 4	CRC 16 0x370C																	

DUT Sends NAK

DUT reports error by sending ERR_COR Message TLP

Config Read TLP is replayed

Link Tests at Different Data Rates

- The Link and Transaction layer test specification states that for some of the tests, they should be run at all applicable link speeds
- This does not apply to all tests
- During testing, the test cases will choose the appropriate speeds and run accordingly.
- Otherwise, if not stated, tests will be run at the maximum speed supported

☑ Link 61-20 FLR 2-16_0	Verify that the DUT correctly handles the FLR completes FLR in 100 ms and no more than 1 sec in case of a Configu...
☑ Link 61-20 FLR 2-2_5	Verify that the DUT correctly handles the FLR completes FLR in 100 ms and no more than 1 sec in case of a Configu...
☑ Link 61-20 FLR 2-32_0	Verify that the DUT correctly handles the FLR completes FLR in 100 ms and no more than 1 sec in case of a Configu...
☑ Link 61-20 FLR 2-5_0	Verify that the DUT correctly handles the FLR completes FLR in 100 ms and no more than 1 sec in case of a Configu...
☑ Link 61-20 FLR 2-8_0	Verify that the DUT correctly handles the FLR completes FLR in 100 ms and no more than 1 sec in case of a Configu...

Transaction Layer Tests

- Poisoned TLP
- Wrong TLP Sequence Number
- Nullified TLP

	Test Name	Test Reference on Teledyne LeCroy Test Suite	Test Reference in Test Spec
3.4.1	TXN_BFT_RequestCompletion	Trans_1-2_TXN_BFT_RequestCompletion_UR	TXN_01-02
3.4.2	BadECRC	Link 54-20 BadECRC	54-20
3.4.3	Poisoned TLP	Link 54-30_Poisoned_TLP	54-30
3.3.3	WrongTLPSeqNum	Link_53-32 WrongTLPSeqNum	53-32
3.3.4	Nullified TLP	Link_53-40 Nullified TLP	53-40

Transaction Layer Test Example – 54-30 Poisoned TLP

Test Description

Verification of each stage

PASS or FAIL result

```
Run test: Link 54-30 PoisonedTLP
Executing stimulus: C:\Users\Public\Documents\LeCroy\PCIe Protocol
Suite\ScriptAutomationTestTool\TrainerScripts\Endpoint\LinkLayer\link_54-30_PoisonedTLP.peg
Trace captured - starting Verification

-----------------------------------------------------------------------------------
C:\Users\Public\Documents\LeCroy\PCIe Protocol Suite\ScriptAutomationTestTool\VerificationScripts\Endpoint\LinkLayer\link_54-30_PoisonedTLP.pevs
-----------------------------------------------------------------------------------


Running verification script...
...

Test Description :
PE Compliance, Transaction Layer Test 54-30 -PoisonedTLP.
The intent of this test is to verify that the DUT will check the EP bit
in a received TLP containing a data payload that targets the DUT and if the bit is set it logs
a Received Poisoned TLP Received error associated with the port, also that an uncorrectable
error message is controlled by the enable, mask, and severity bits.
Transaction Layer Test 54-30 -PoisonedTLP
Verifying TEST CASE 1 (SERR# Disabled, Non-Fatal enabled, Poisoned unmasked, Severity Non-Fatal).
Verifying TEST CASE 2 (SERR# Enabled, Non-Fatal disabled, Poisoned unmasked, Severity Non-Fatal).
Verifying TEST CASE 3 (SERR# Disabled, Non-Fatal disabled, Poisoned unmasked, Severity Non-Fatal).
Verifying TEST CASE 4 (SERR# Disabled, Non-Fatal enabled, Poisoned masked, Severity Non-Fatal).
Verifying TEST CASE 5 (SERR# Disabled, Fatal enabled, Poisoned unmasked, Severity Fatal).
Verifying TEST CASE 6 (SERR# Enabled, Fatal disabled, Poisoned unmasked, Severity Fatal).
Verifying TEST CASE 7 (SERR# Disabled, Fatal disabled, Poisoned unmasked, Severity Fatal).
Verifying TEST CASE 8 (SERR# Disabled, Fatal enabled, Poisoned masked, Severity Fatal).


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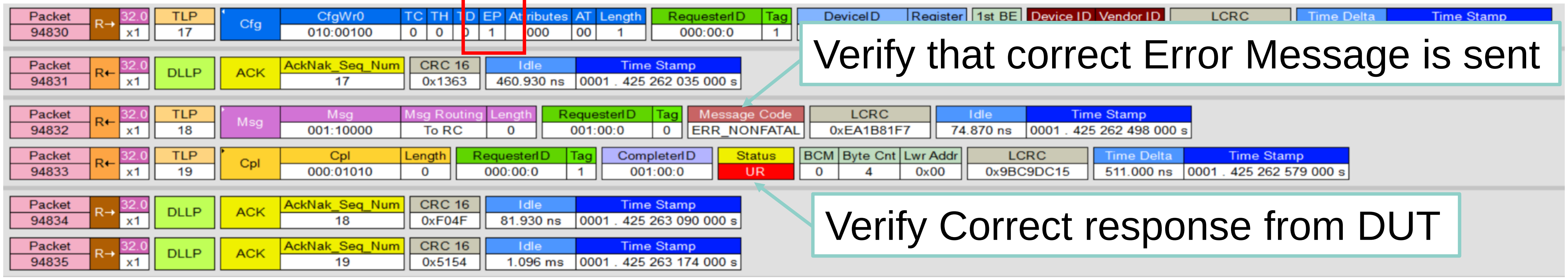
Transaction Layer Example – 54-30 Poisoned TLP

PTC/Exerciser Sends Config
Write with Poisoned bit set



Packet	R→	32.0	TLP	Cfg	CfgWr0	TC	TH	TD	EP	Attributes	AT	Length	RequesterID	Tag	DeviceID	Register	1st BE	Device ID	Vendor ID	LCRC	Time Delta	Time Stamp
94830		x1	17		010:00100	0	0	0	1	000	00	1	000:00:0	1								

Packet	R←	32.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Idle	Time Stamp
94831		x1			17	0x1363	460.930 ns	0001 . 425 262 035 000 s

Packet	R←	32.0	TLP	Msg	Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Idle	Time Stamp
94832		x1	18		001:10000	To RC	0	001:00:0	0	ERR_NONFATAL	0xEA1B81F7	74.870 ns	0001 . 425 262 498 000 s

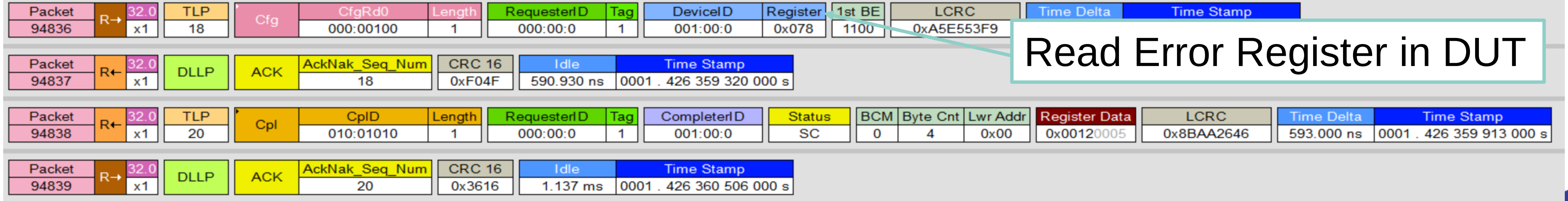
Packet	R←	32.0	TLP	Cpl	Cpl	Length	RequesterID	Tag	CompleterID	Status	BCM	Byte Cnt	Lwr Addr	LCRC	Time Delta	Time Stamp
94833		x1	19		000:01010	0	000:00:0	1	001:00:0	UR	0	4	0x00	0x9BC9DC15	511.000 ns	0001 . 425 262 579 000 s

Packet	R→	32.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Idle	Time Stamp
94834		x1			18	0xF04F	81.930 ns	0001 . 425 263 090 000 s

Packet	R→	32.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Idle	Time Stamp
94835		x1			19	0x5154	1.096 ms	0001 . 425 263 174 000 s

Verify that correct Error Message is sent

Verify Correct response from DUT



Packet	R→	32.0	TLP	Cfg	CfgRd0	Length	RequesterID	Tag	DeviceID	Register	1st BE	LCRC	Time Delta	Time Stamp
94836		x1	18		000:00100	1	000:00:0	1	001:00:0	0x078	1100	0xA5E553F9		

Packet	R←	32.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Idle	Time Stamp
94837		x1			18	0xF04F	590.930 ns	0001 . 426 359 320 000 s

Packet	R←	32.0	TLP	Cpl	CplD	Length	RequesterID	Tag	CompleterID	Status	BCM	Byte Cnt	Lwr Addr	Register Data	LCRC	Time Delta	Time Stamp
94838		x1	20		010:01010	1	000:00:0	1	001:00:0	SC	0	4	0x00	0x00120005	0x8BAA2646	593.000 ns	0001 . 426 359 913 000 s

Packet	R→	32.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Idle	Time Stamp
94839		x1			20	0x3616	1.137 ms	0001 . 426 360 506 000 s

Read Error Register in DUT

Equalization Tests

- The equalization tests are different from the Link EQ electrical tests
- The Protocol Equalization tests validate that different combinations of presets and coefficients are properly handled and abide by the rules set out in the specification
- These tests check the contents of the TS1 Ordered Sets during the Recovery. Equalization substate
- Test results are determined by log of LTSSM in PTC, rather than by interpreting trace file
- Trace can be captured for debug purposes

Equalization Test Example – 58-12 Adjust Presets 32.0 GT/s

```
Run test: Link 58-12 AdjustPresets 32.0 GTs 02
Executing stimulus: C:\Users\Public\Documents\LeCroy\PCIe Protocol
Suite\ScriptAutomationTestTool\TrainerScripts\Endpoint\LinkLayer\link_58-12_AdjustingPresets32G-02.peg
Trace captured - starting Verification

-----------------------------------------------------------------------------------------
C:\Users\Public\Documents\LeCroy\PCIe Protocol
Suite\ScriptAutomationTestTool\VerificationScripts\Endpoint\LinkLayer\link_58-12_AdjustingPresets32G.pevs
-----------------------------------------------------------------------------------------


Running verification script...
...

Test Description :
58-12 Adjusting Presets at 32 GT/s
Verifying Test 58-12 Adjusting Presets for 32.0 GT/s, Test case 2.
SPD 2.5G | State: Detect
SPD 2.5G | State: Polling
SPD 2.5G | State: Polling
SPD 2.5G | State: Polling
SPD 2.5G | State: Configuration
SPD 2.5G | State: Configuration
SPD 2.5G | State: Configuration
SPD 2.5G | State: Configuration
SPD 2.5G | State: Configuration
SPD 2.5G | State: Configuration
SPD 2.5G | State: Configuration
SPD 2.5G | State: L0
SPD 2.5G | State: L0
SPD 2.5G | State: Recovery , SubState: Unknown
SPD 2.5G | State: Recovery , SubState: Lock
SPD 2.5G | State: Recovery , SubState: Config
SPD 8.0G | State: Recovery , SubState: Speed
SPD 8.0G | State: Recovery , SubState: Lock
SPD 8.0G | State: Recovery , SubState: EQ1 , EC 3, TxPres 15, PreCursor 63, Cursor 63, PostCursor 63, REJ
SPD 8.0G | State: Recovery , SubState: EQ1 , EC 1, TxPres 5, FS 48, LF 16, PostCursor 0, UPD CP
SPD 8.0G | State: Recovery , SubState: EQ2 , EC 1, TxPres 5, FS 48, LF 16, PostCursor 0
SPD 8.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 5, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 8.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 4, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 8.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 5, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 8.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 6, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 8.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 7, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 8.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 5, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 8.0G | State: Recovery , SubState: EQ2 , EC 3, TxPres 5, PreCursor 5, Cursor 43, PostCursor 0, UPD CP
SPD 8.0G | State: Recovery , SubState: EQ3 , EC 3, TxPres 5, PreCursor 5, Cursor 43, PostCursor 0
SPD 8.0G | State: Recovery , SubState: Lock
SPD 8.0G | State: Recovery , SubState: Config
```

```
SPD 8.0G | State: Recovery , SubState: Idle
SPD 8.0G | State: L0
SPD 8.0G | State: L0
SPD 8.0G | State: L0
SPD 8.0G | State: Recovery , SubState: Unknown
SPD 8.0G | State: Recovery , SubState: Lock
SPD 8.0G | State: Recovery , SubState: Config
SPD 16.0G | State: Recovery , SubState: Speed
SPD 16.0G | State: Recovery , SubState: Lock
SPD 16.0G | State: Recovery , SubState: EQ1 , EC 3, TxPres 5, PreCursor 5, Cursor 43, PostCursor 0
SPD 16.0G | State: Recovery , SubState: EQ1 , EC 1, TxPres 5, FS 48, LF 16, PostCursor 0, UPD CP
SPD 16.0G | State: Recovery , SubState: EQ2 , EC 1, TxPres 5, FS 48, LF 16, PostCursor 0
SPD 16.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 5, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 16.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 9, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 16.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 5, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 16.0G | State: Recovery , SubState: EQ2 , EC 3, TxPres 5, PreCursor 5, Cursor 43, PostCursor 0, UPD CP
SPD 16.0G | State: Recovery , SubState: EQ3 , EC 3, TxPres 5, PreCursor 5, Cursor 43, PostCursor 0
SPD 16.0G | State: Recovery , SubState: Lock
SPD 16.0G | State: Recovery , SubState: Config
SPD 16.0G | State: Recovery , SubState: Idle
SPD 16.0G | State: L0
SPD 16.0G | State: Recovery , SubState: Unknown
SPD 16.0G | State: Recovery , SubState: Lock
SPD 16.0G | State: Recovery , SubState: Config
SPD 32.0G | State: Recovery , SubState: Speed
SPD 32.0G | State: Recovery , SubState: Lock
SPD 32.0G | State: Recovery , SubState: EQ1 , EC 3, TxPres 5, PreCursor 5, Cursor 43, PostCursor 0
SPD 32.0G | State: Recovery , SubState: EQ1 , EC 1, TxPres 1, FS 48, LF 16, PostCursor 8, UPD CP
SPD 32.0G | State: Recovery , SubState: EQ2 , EC 1, TxPres 1, FS 48, LF 16, PostCursor 8
SPD 32.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 5, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 32.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 5, PreCursor 2, Cursor 36, PostCursor 0, UPD CP
SPD 32.0G | State: Recovery , SubState: EQ2 , EC 2, TxPres 5, PreCursor 4, Cursor 36, PostCursor 0, UPD CP
SPD 32.0G | State: Recovery , SubState: EQ2 , EC 3, TxPres 1, PreCursor 0, Cursor 40, PostCursor 8, UPD CP
SPD 32.0G | State: Recovery , SubState: EQ3 , EC 3, TxPres 1, PreCursor 0, Cursor 40, PostCursor 8
SPD 32.0G | State: Recovery , SubState: Lock
SPD 32.0G | State: Recovery , SubState: Config
SPD 32.0G | State: Recovery , SubState: Idle
SPD 32.0G | State: L0
PASSED Test Case 2 for test preset value 1.


------- P A S S E D -------
```

Reserved Bits Test

- The intention of the Reserved Bits in TS test is to validate that Reserved bits are ignored, and that the link successfully reaches the L0 state
- This test was added for PCIe® 2.0 specification when it was discovered that some PCIe 1.0a devices did not link when plugged into PCIe 2.0 systems because they did not ignore the 5GT/s capable bit in the TS1 Ordered Set

Complete List of Tests

- Please refer to the test specification and MOI (Test Procedure)
- Tests are mandatory unless stated otherwise
- No waivers will be granted
- PCIe® 5.0 MOI posted to PCI-SIG® Serial Enabling Group Document folder

PCI Express® 5.0 Protocol Compliance

NEW FEATURES

4/27/2023

PCIe® 5.0 Protocol Compliance

- Add new requirement to run all existing Link/Transaction Layer tests at 32.0 GT/s for PCIe 5.0 specification
- Add new 32.0 GT/s detection and configuration algorithm
  - Add Procedure to Reach L0 at 32.0 GT/s (A.2.6)
  - Updated tests L1 for D3 State (65-10) and Test ASPM-L1 (66-10) to support 32.0 GT/s
  - Update test Data Link Feature Packet (68-10) to support 32.0 GT/s
- Change Training set field definitions for 32.0 GT/s
  - Update TS Reserved bit test (55-10) to remove Data Rate Identifier bit 5 (32.0 GT/s data rate) for PCIe 5.0 testing
  - Update TS Reserved bit test (55-10) to remove Training Control bits 6-7 (Enhanced Link Behavior Control) and to remove for TS1 only, Training Control bit 5 (Transmit Modified Compliance Pattern in Loopback)
- Add Precoding Test (Test 69-12)

PCIe® 5.0 Protocol Compliance

- Support for link equalization at 32.0 GT/s
  - Add new test Adjusting Initial Presets at 32.0 GT/s (57-12) based on Adjusting Initial Presets at 16.0 GT/s (57-11).
  - Add new test Adjusting Presets at 32.0 GT/s (58-12) based on Adjusting Presets at 16.0 GT/s (58-11).
  - Add new test Adjusting Coefficients at 32.0 GT/s (59-12) based on Adjusting Coefficients at 16.0 GT/s (59-11)
  - Add new test Equalization Redo for 32.0 GT/s (71-12) based on Equalization Redo for 16.0 GT/s (71-11).
- Test Enhancements for existing data rates
  - Add new test Equalization Redo for 8.0 GT/s (70-10).
  - Add new test Equalization Redo for 8.0 GT/s (71-10) based on Equalization Redo for 16.0 GT/s (71-11).

PCI Express® 5.0 Specification

LANE MARGINING TESTING

4/27/2023

Lane Margining at Receiver

- Lane Margining at Receiver is mandatory for all Ports supporting 16.0 GT/s Data Rate and above, including Retimers
- Lane Margining at Receiver enables system software to obtain the margin information of a given Receiver while the Link is in L0 (Active) state
- The margin information includes both voltage and time, in either direction from the current Receiver position
- For all Ports that implement Lane Margining at Receiver, Lane Margining at Receiver for timing and voltage is required, while support of Lane Margining at Receiver for voltage is optional for PCIe® 4.0 architecture
- Software mechanism to “step” through different sampling points in the receiver
- Hardware reports errors, not a hardware mechanism like the Recovery.Equalization state

Lane Margining Testing

- Lane Margining Test is defined in the Electrical Test Specification
  - Test run with the Link/Transaction tests for Add-In Cards
  - Systems tested using Software Tool
- 3 flavors of testing
  - Add In Card – No Device Driver Required
  - Add In Card – Device Driver Required
  - System Lane Margining Testing
- Lane Margining **testing** is FYI only for PCIe® 4.0 specification, and is **mandatory** for PCIe 5.0 specification

Part 2: Electrical Compliance Testing

TRANSMITTER ELECTRICAL TESTS

PCI Express® Transmitter Electrical Tests

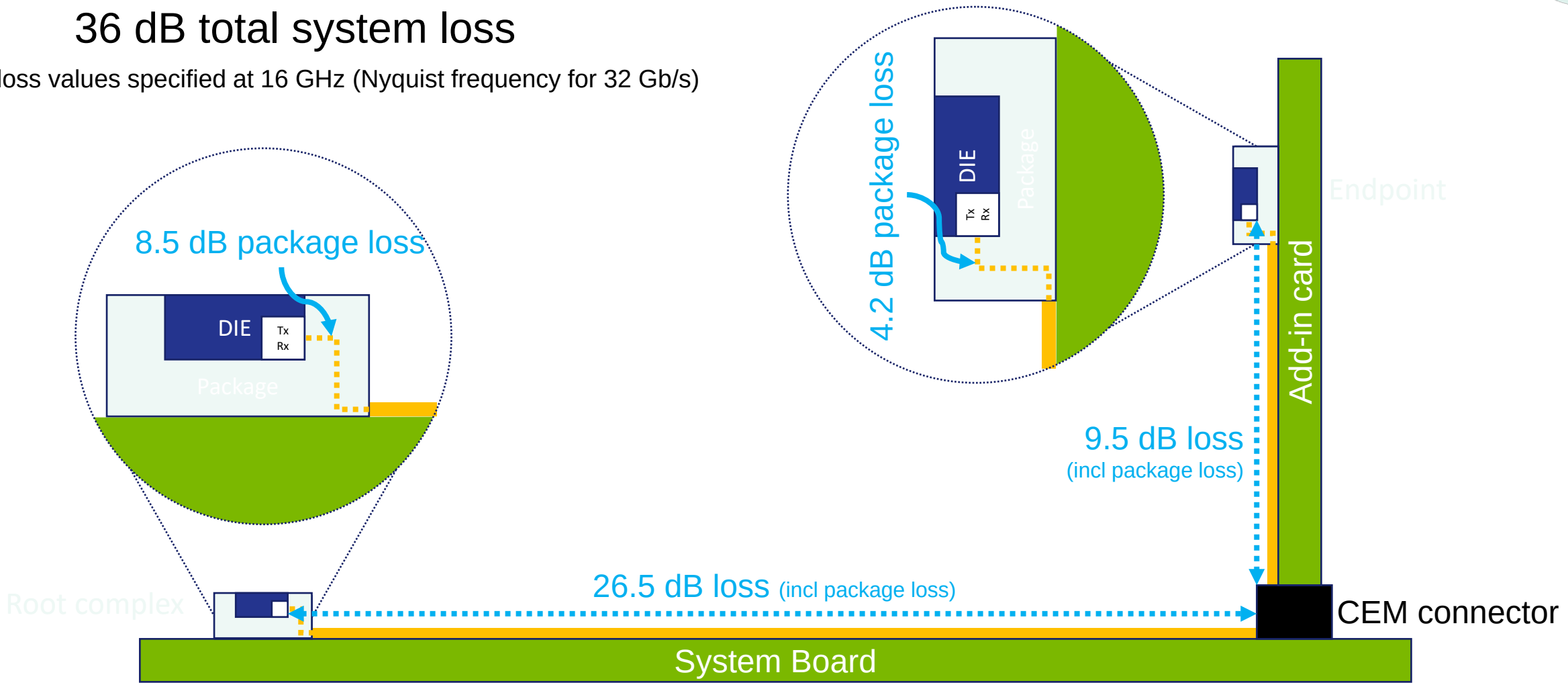
Test name	Notes
Lane Margining Tests	Protocol Test runs on Protocol Exerciser
Link Layer Tests	Protocol Exerciser
Transaction Layer Tests	Protocol Exerciser
Configuration Space Tests (PCIECV)	Runs on PC
Transmitter Signal Quality	Automated using SigTest Phoenix
Transmitter Jitter (Pulse Width Jitter)	Automated using SigTest Phoenix
Transmitter Preset	Automated using SigTest Phoenix
Transmitter Initial Tx Equalization	Add-in card only
Transmitter Link Equalization response	
Receiver Link Equalization	
PLL Bandwidth	Add-in card only
Reference Clock Jitter	System only - new for PCIe® 5.0 compliance
PCB Impedance	Informative only – VNA test

(PCI Express 5.0 PHY test spec, Rev 0.9)

PCIe® 5.0 Nominal Channel

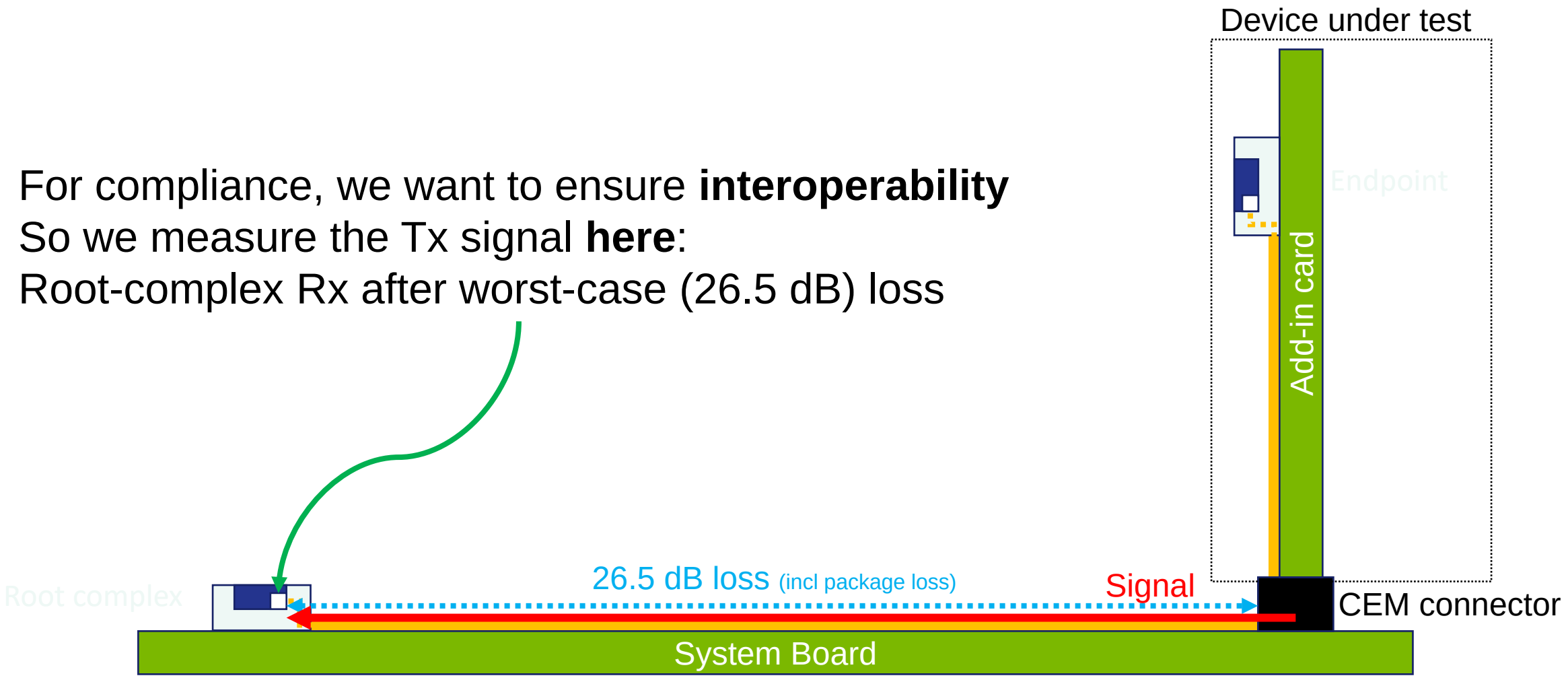
36 dB total system loss

All loss values specified at 16 GHz (Nyquist frequency for 32 Gb/s)



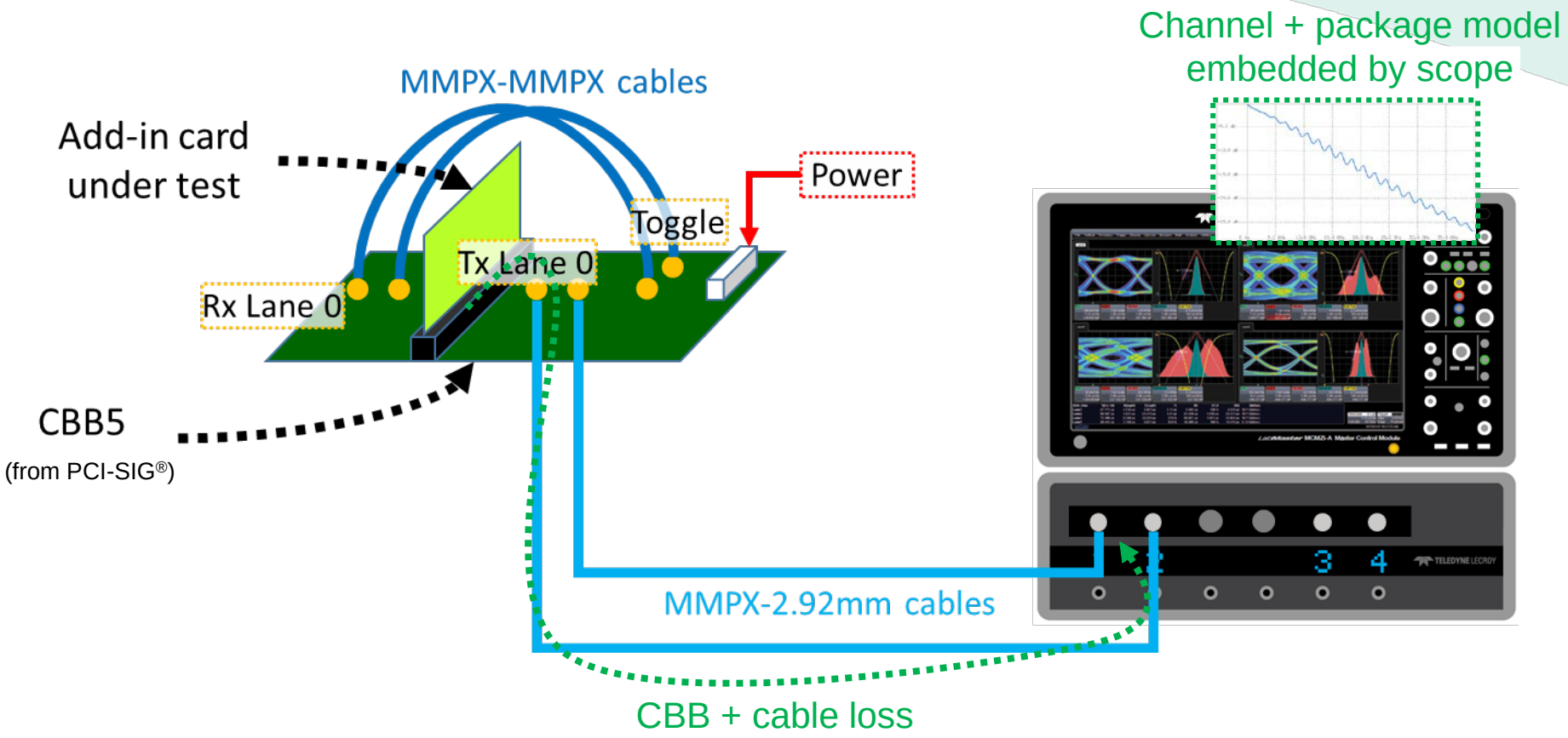
Transmitter Signal Quality Test

For compliance, we want to ensure **interoperability**
So we measure the Tx signal **here**:
Root-complex Rx after worst-case (26.5 dB) loss



Transmitter Signal Quality Test
Connection schematic

- Worst-case channel + package loss is emulated by embedding s-parameter files in oscilloscope software
- Different reference s-parameter files are available – correct model is selected based on measured CBB/cable loss so that entire channel loss sums to 26.5 dB



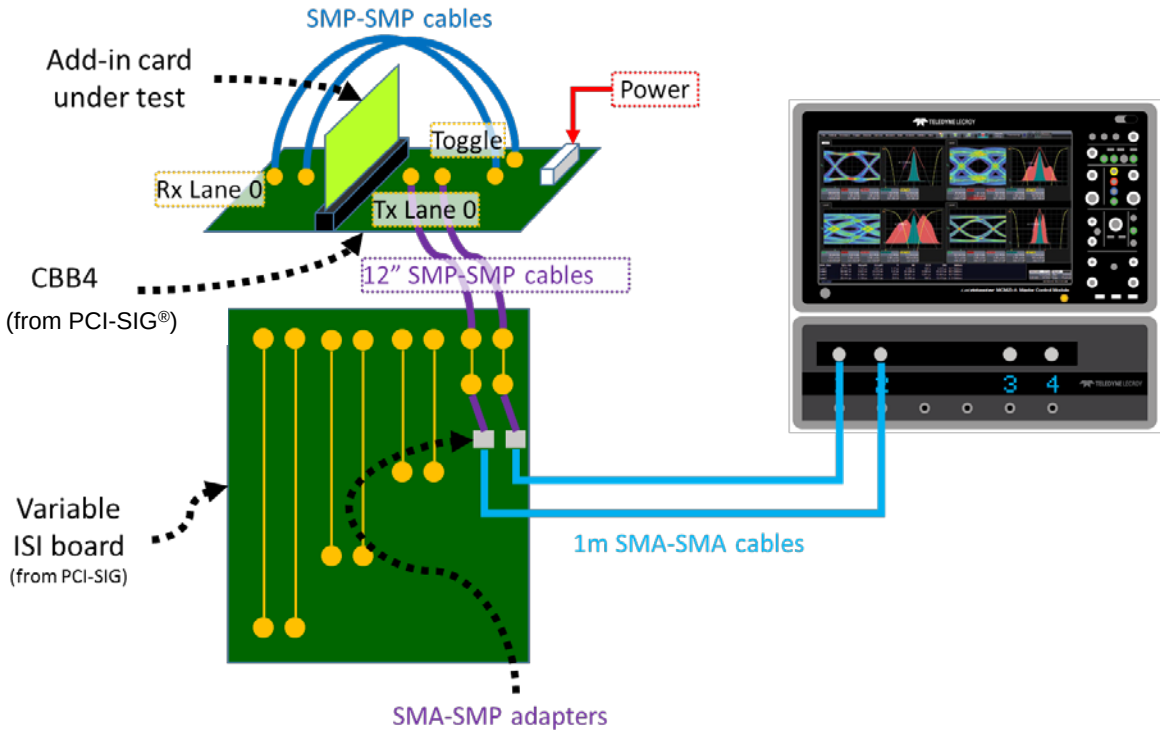
CBB + cable loss + emulated channel + package loss = 26.5 dB

Physical channel — Emulated in software

Transmitter Signal Quality Test
Differences from PCIe® 4.0 specification

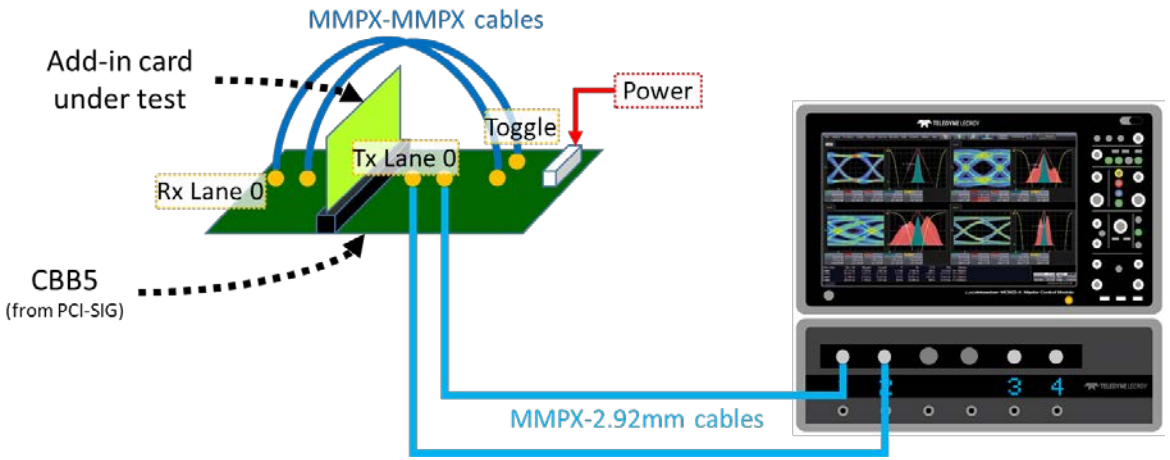
PCIe 4.0 specification at 16 GT/s:

- **Physical** loss channel
- Emulated package model



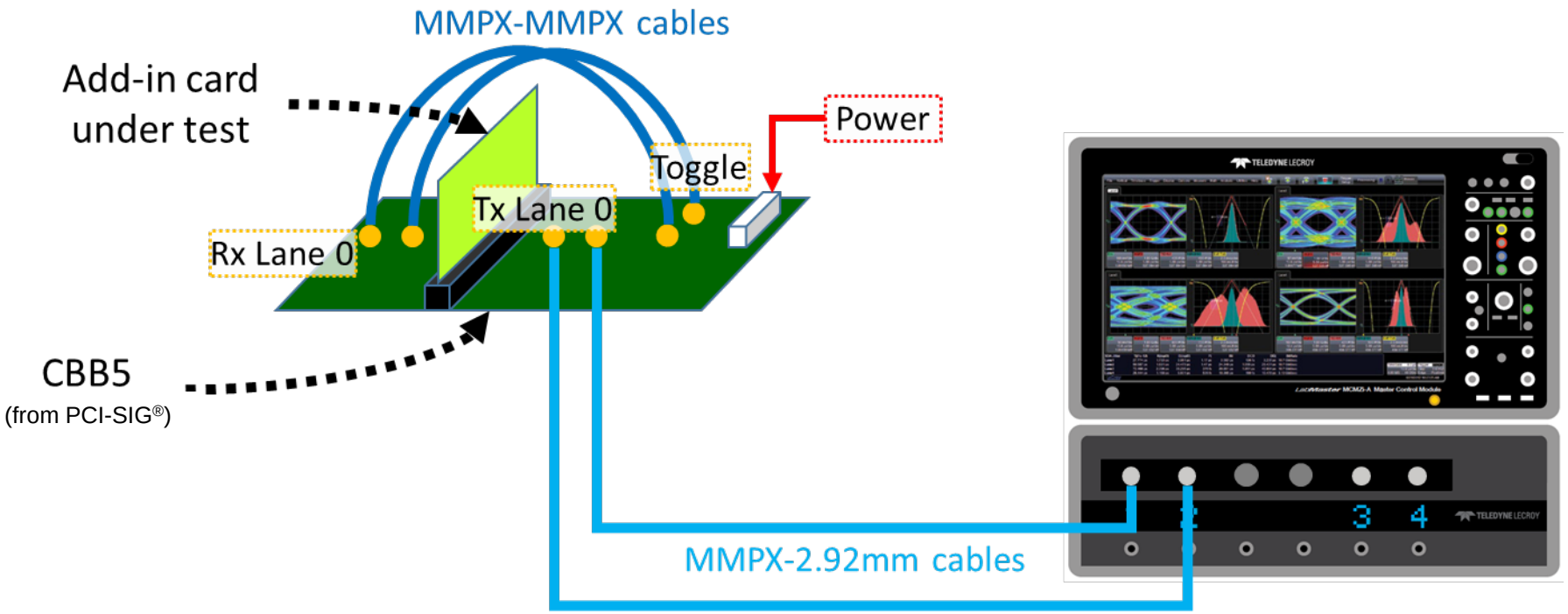
PCIe 5.0 specification at 32 GT/s:

- **Emulated** loss channel
- Emulated package model



Transmitter Preset and Jitter Tests
Connection schematic

- Direct connection from CBB/CLB output to oscilloscope input
- **No** package or channel embedding



Transmitter Preset Test

- Acquire one waveform at each Tx equalization preset
- Pass all waveforms to SigTest
- SigTest compares pre-shoot/de-emphasis of each waveform to P4 (0dB/0dB)

PCIe Gen 5 Preset Test AC Results

(PASS) Preset Test AC

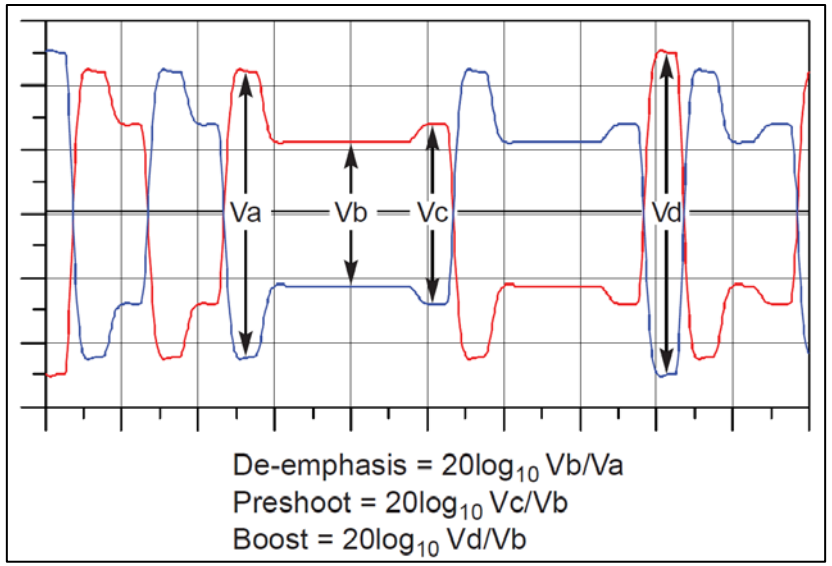
Preset Test AC — Overall Result: *PASS*

Preset	Waveform	Boost	Preshoot (dB)	De-emphasis	Lane	Prese	Pass/Fail
P00:	F1_L_TIDxxx_R1_32G_S1_Ln0_P00_d	5.60929	-0.37047	-5.79737	0	0	PASS
P01:	F1_L_TIDxxx_R1_32G_S1_Ln0_P01_d	3.06076	-0.17697	-3.18305	0	1	PASS
P02:	F1_L_TIDxxx_R1_32G_S1_Ln0_P02_d	4.02612	-0.45626	-4.30132	0	2	PASS
P03:	F1_L_TIDxxx_R1_32G_S1_Ln0_P03_d	2.01026	-0.40365	-2.31768	0	3	PASS
P04:	F1_L_TIDxxx_R1_32G_S1_Ln0_P04_d	0	0	0	0	4	PASS
P05:	F1_L_TIDxxx_R1_32G_S1_Ln0_P05_d	1.06074	1.18155	0.13855	0	5	PASS
P06:	F1_L_TIDxxx_R1_32G_S1_Ln0_P06_d	1.83417	2.14203	0.39595	0	6	PASS
P07:	F1_L_TIDxxx_R1_32G_S1_Ln0_P07_d	7.07178	2.25302	-5.85027	0	7	PASS
P08:	F1_L_TIDxxx_R1_32G_S1_Ln0_P08_d	5.12118	2.9801	-2.885	0	8	PASS
P09:	F1_L_TIDxxx_R1_32G_S1_Ln0_P09_d	2.67789	3.05972	0.54824	0	9	PASS
P010:	F1_L_TIDxxx_R1_32G_S1_Ln0_P10_d	9.14259	-0.54986	-9.3266	Coul	Coul	PASS

Transmitter Preset Test Methodology

PCIe® 3.0 and 4.0 specifications vs. PCIe 5.0 specification

- Methodology for 16 GT/s and below:
  - Measure four amplitudes (Va, Vb, Vc, Vd) from specific points in the waveform
  - Calculate emphasis from these measurements as per below



Source: PCI Express® Base Specification Revision 5.0 Version 1.0

- Methodology for 32 GT/s:
  - Capture no-equalization (P4) waveform as baseline
  - Extract step response from both P4 waveform and signal to be measured
  - Determine equalization coefficients that minimize mean-square error between both step responses

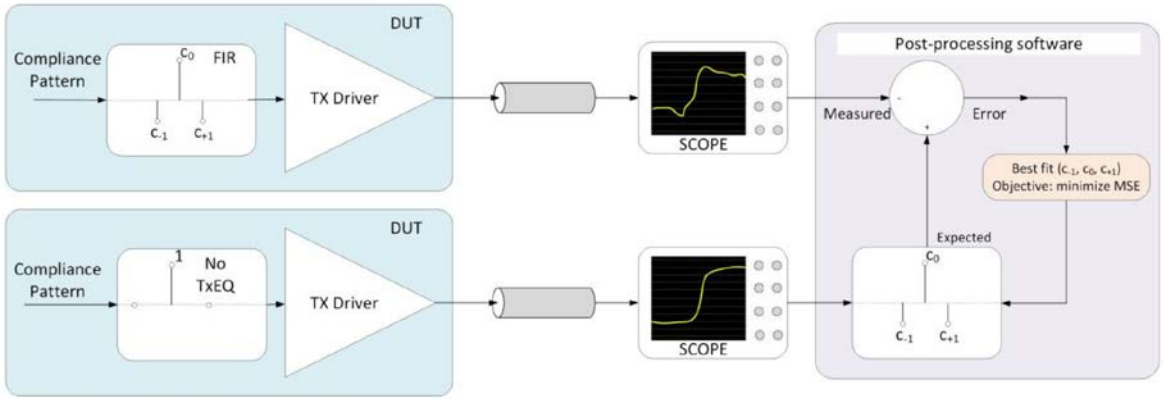
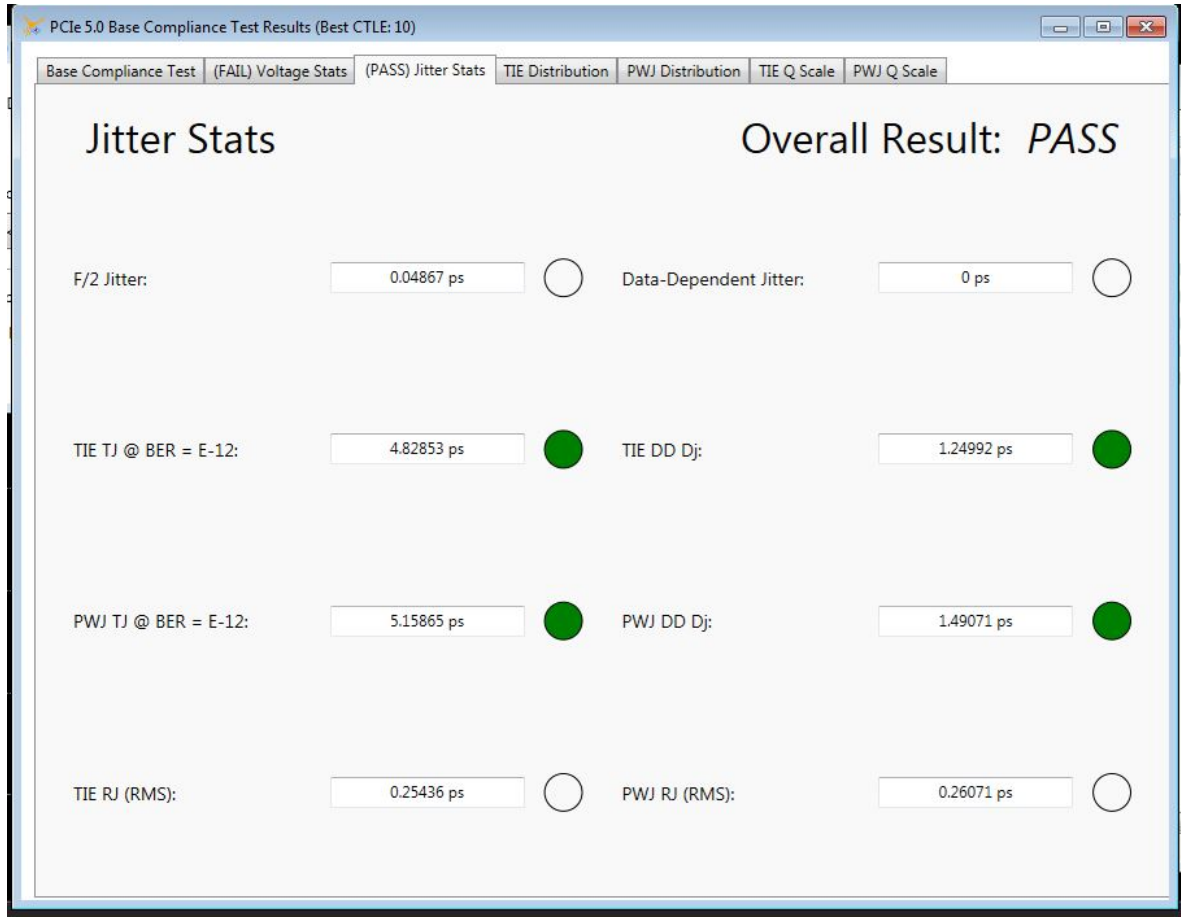


Figure Methodology for measuring Tx equalization coefficients and presets

Source: PCI Express Base Specification Revision 5.0 Engineering Change Request (ECR): *"Fitting-based Tx Preset Measurement Methodology for 8.0, 16.0, and 32.0 GT/s"*

Transmitter Jitter Test

- This test was added to the compliance program for add-in cards at PCIe® 4.0 architecture, and is being added for systems at PCIe 5.0 architecture
- Performed using the jitter measurement pattern:
  - 1010 (“clock-like”) pattern on the lane under test
  - Traffic on other lanes
- SigTest Phoenix is also used for this test



Transmitter Link Equalization Tests

PCI Express® Transmitter Link Equalization

Test name	Notes
Lane Margining Tests	Protocol Test runs on Protocol Exerciser
Link Layer Tests	Protocol Exerciser
Transaction Layer Tests	Protocol Exerciser
Configuration Space Tests (PCIECV)	Runs on PC
Transmitter Signal Quality	Automated using SigTest Phoenix
Transmitter Jitter (Pulse Width Jitter)	Automated using SigTest Phoenix
Transmitter Preset	Automated using SigTest Phoenix
Transmitter Initial Tx Equalization	Add-in card only
Transmitter Link Equalization response	
Receiver Link Equalization	
PLL Bandwidth	Add-in card only
Reference Clock Jitter	System only - new for PCIe® 5.0 compliance
PCB Impedance	Informative only – VNA test

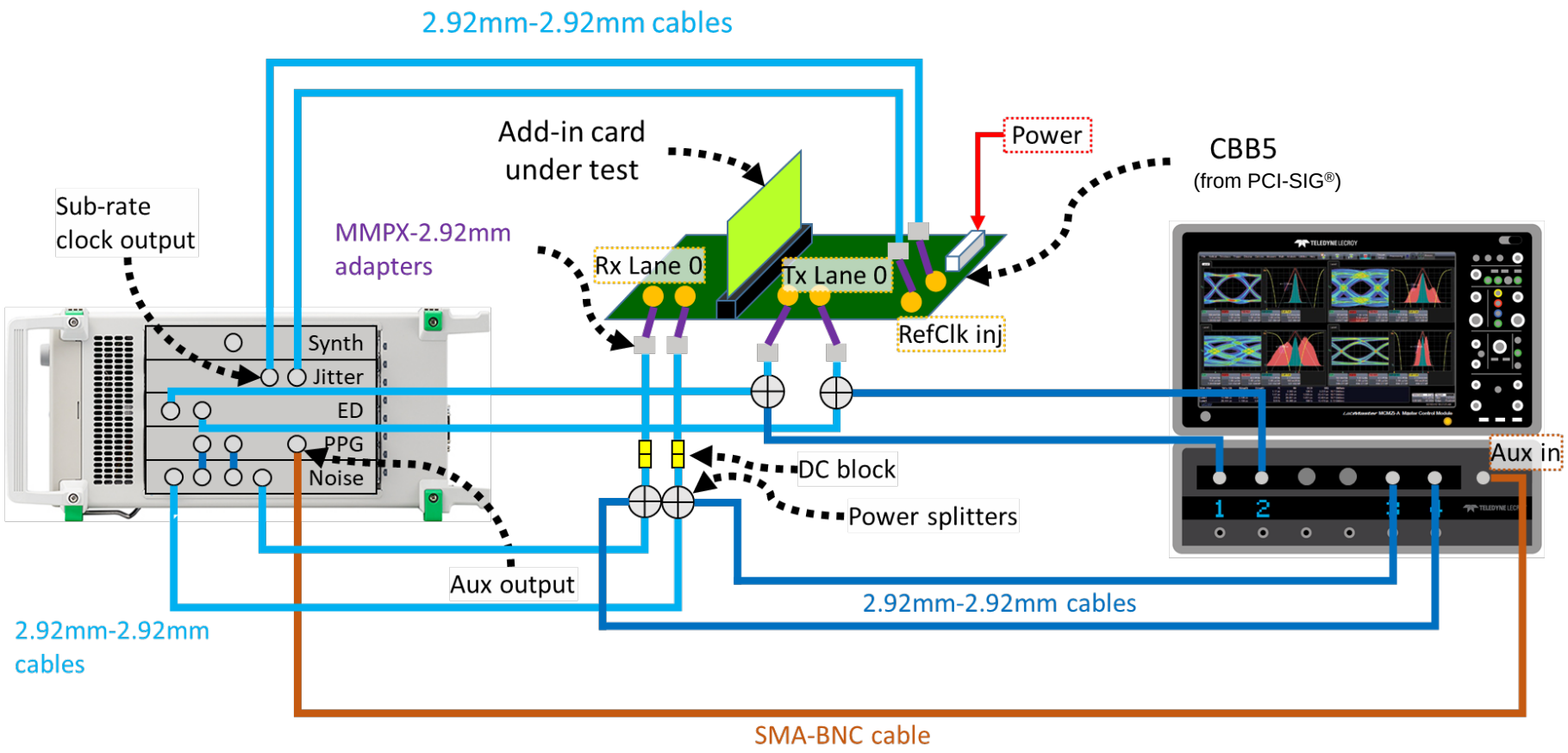
(PCI Express 5.0 PHY test spec, Rev 0.9)

Transmitter Link Equalization test

- **Initial preset test** (Add-in card only)
  1. Negotiate device to 32 GT/s with a requested initial TxEQ preset
  2. Ensure that the requested preset is produced
  3. Repeat steps 1 and 2 for all presets
- **Preset response test** (Add-in card and System)
  1. Negotiate device to 32 GT/s with any initial TxEQ preset
  2. Request change to a different preset
     a) Check that new preset is correct
     b) Check that preset change happened within require time
     c) Note DUT's reported TxEQ coefficients
  3. Repeat steps 1 and 2 for all presets
  4. Repeat steps 1-3, requesting TxEQ by coefficients noted in step 2c

Transmitter Link Equalization – Test Setup

- Signal from BERT to DUT and from DUT to BERT are split to the oscilloscope
- Trigger signal from BERT enables scope to be triggered at any point in the link training sequence

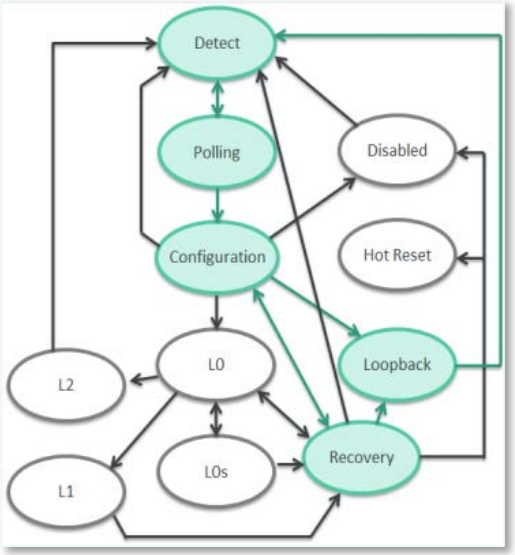


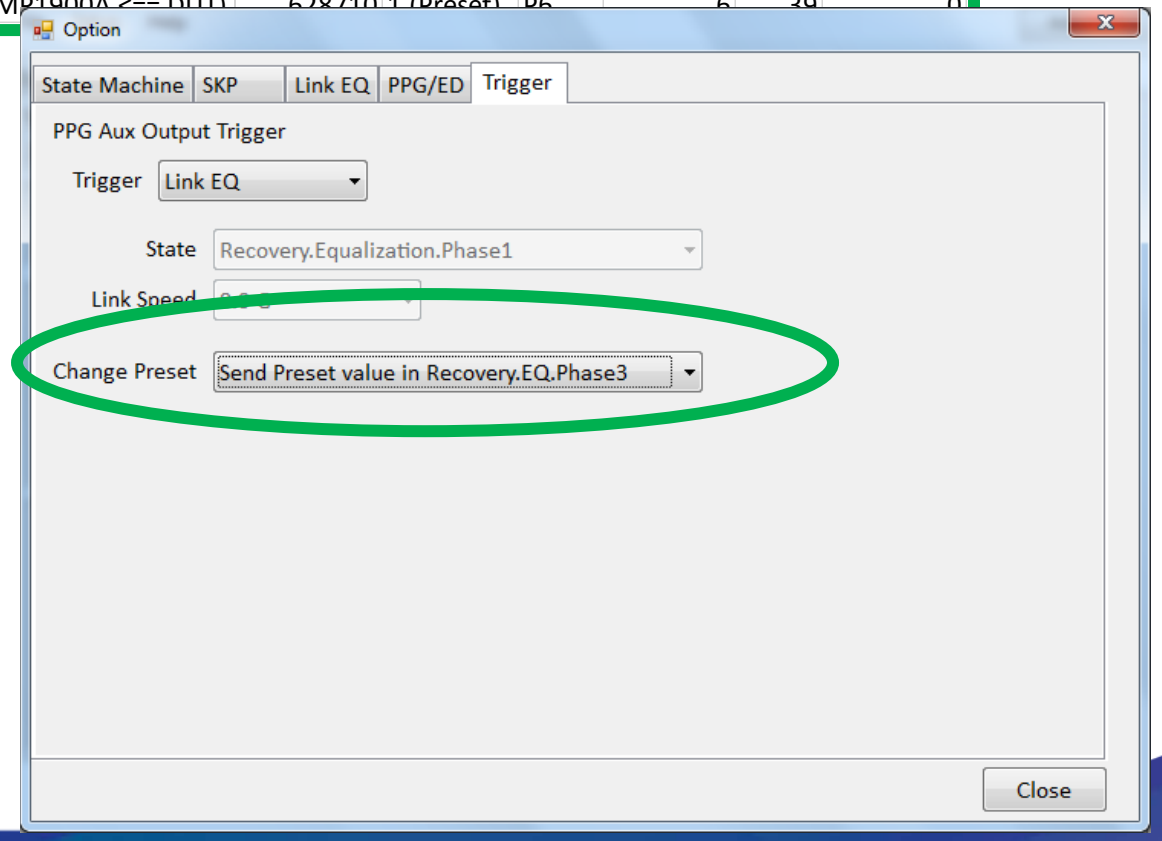
Preset Response Test

- BERT requests DUT change its Tx emphasis preset from P7 to P6

State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor
RECOVERY_EQUALIZATION_PHASE2	32	0 (MP1900A ==> DUT)	0	0 (Cursor)	P4	3	21	0
RECOVERY_EQUALIZATION_PHASE2	32	1 (MP1900A <== DUT)	0	0 (Cursor)	P4	2	22	0
RECOVERY_EQUALIZATION_PHASE2	32	0 (MP1900A ==> DUT)	0	0 (Cursor)	P4	2	22	0
RECOVERY_EQUALIZATION_PHASE3	32	0 (MP1900A ==> DUT)	0	1 (Preset)	P7	4	32	9
RECOVERY_EQUALIZATION_PHASE3	32	1 (MP1900A <== DUT)	629825	1 (Preset)	P7	5	31	9
RECOVERY_EQUALIZATION_PHASE3	32	0 (MP1900A ==> DUT)	0	1 (Preset)	P6	5	40	0
RECOVERY_EQUALIZATION_PHASE3	32	1 (MP1900A <== DUT)	628710	1 (Preset)	P6	6	39	0

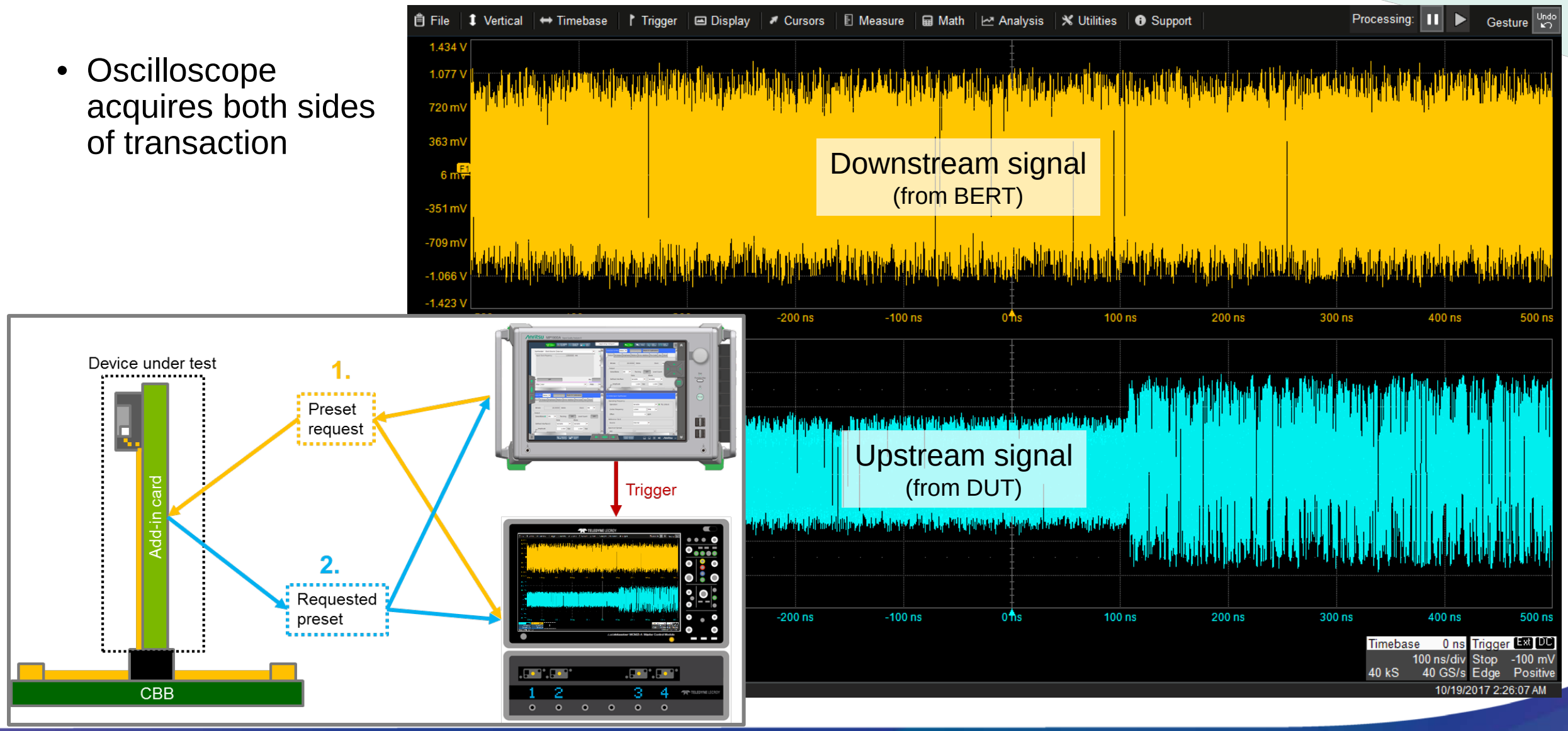
- BERT sends trigger to oscilloscope at the time of preset change request





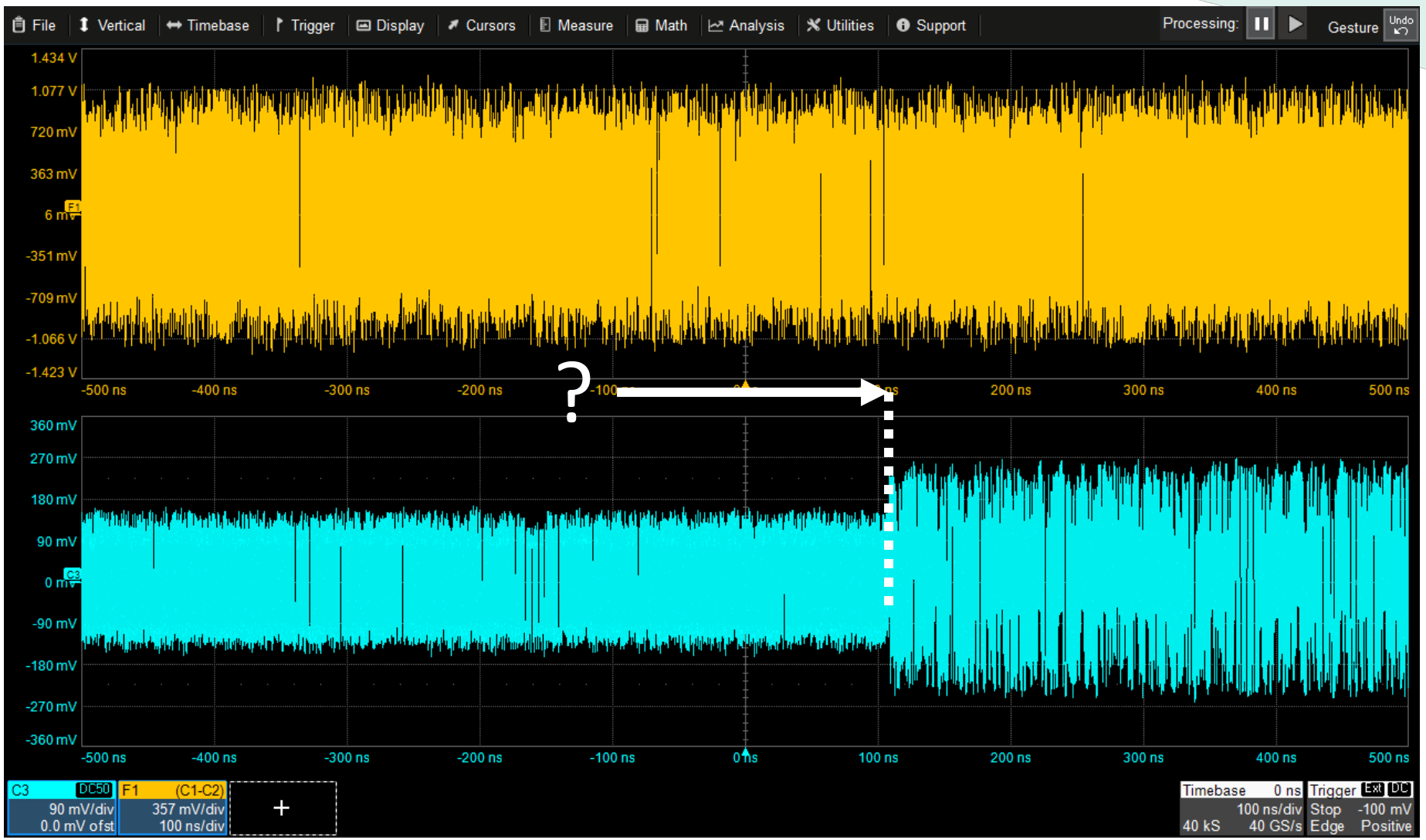
Preset Response Test

- Oscilloscope acquires both sides of transaction



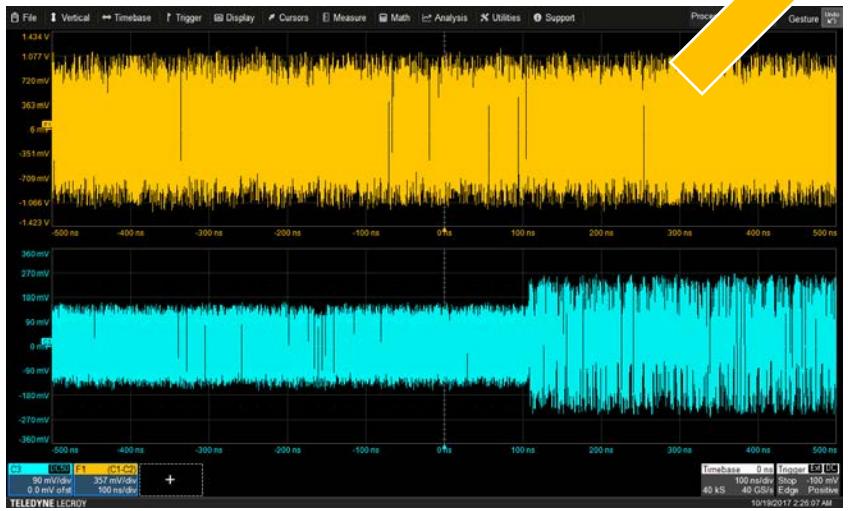
Preset Response Test

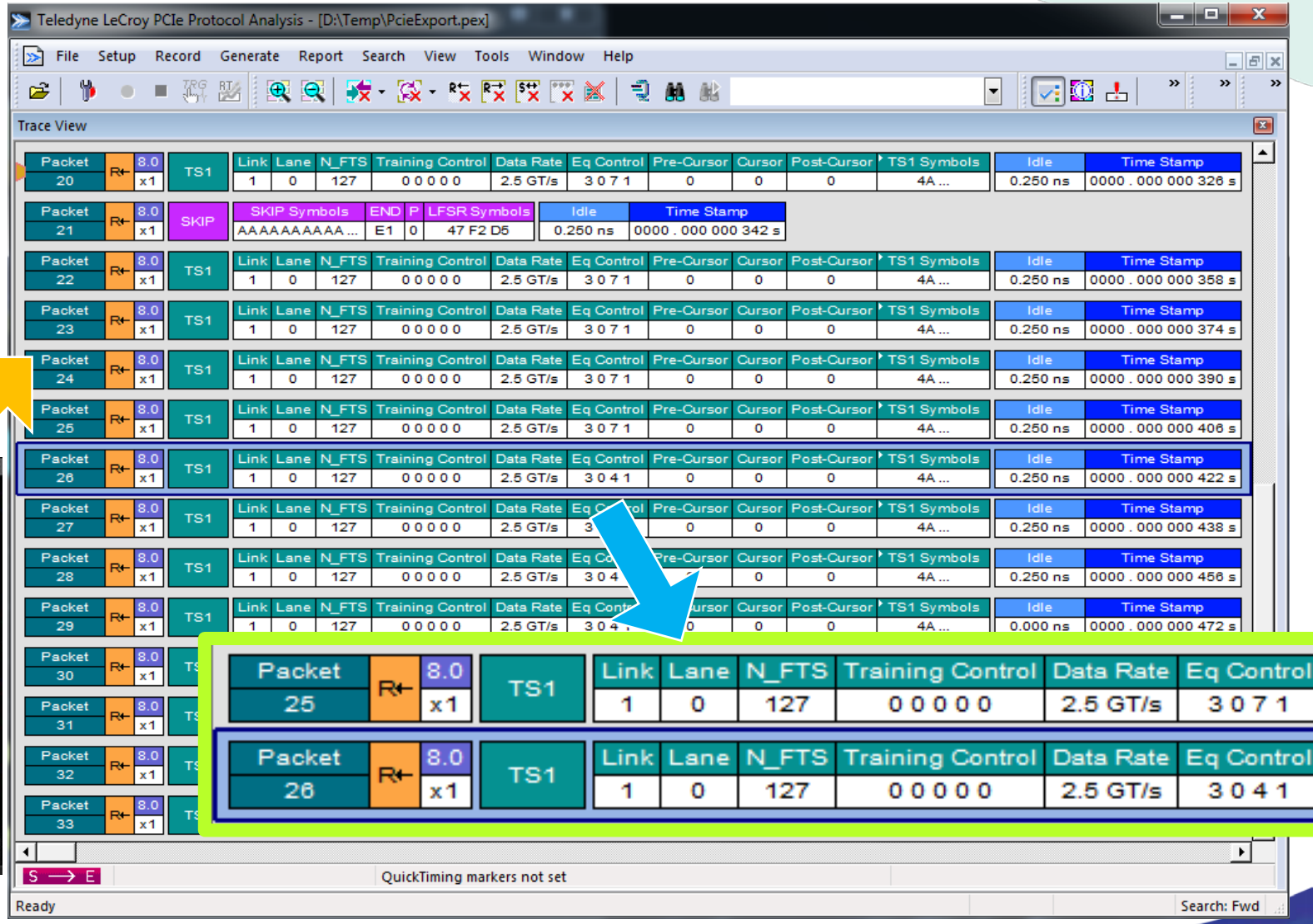
- The emphasis change is clearly visible: this is the end-point of the measurement
- But we need to determine the exact timing of the protocol-layer request, so we know where to start the measurement



Preset Response Test

- The oscilloscope decodes the downstream signal into digital data and passes it to the protocol analysis software that you are using





Preset Response Test

[redacted]

[redacted]

- Now it's trivial to measure the response time from protocol request to physical emphasis change

- This device's response time is 81.18ns – an easy pass

Receiver Link Equalization Test

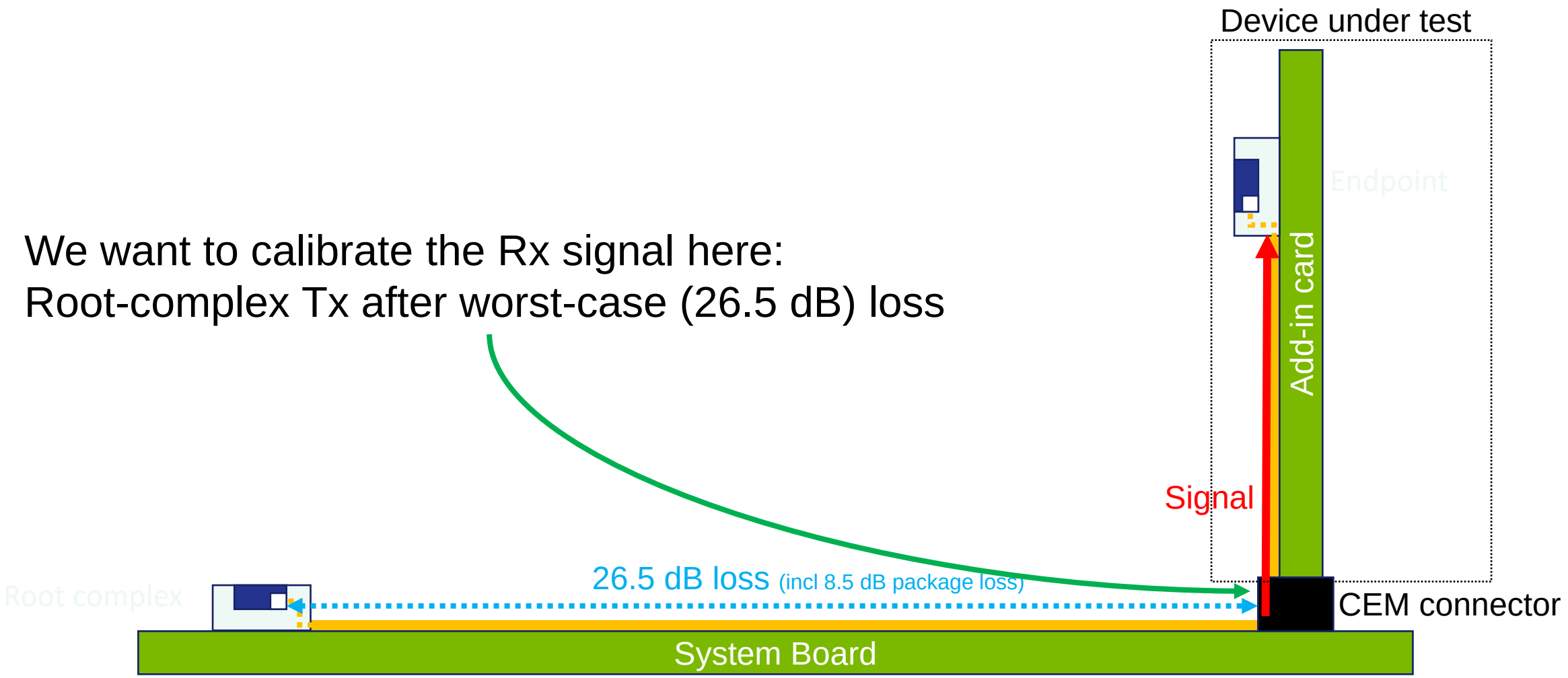
PCI Express® Receiver Link Equalization Test

Test name	Notes
Lane Margining Tests	Protocol Test runs on Protocol Exerciser
Link Layer Tests	Protocol Exerciser
Transaction Layer Tests	Protocol Exerciser
Configuration Space Tests (PCIECV)	Runs on PC
Transmitter Signal Quality	Automated using SigTest Phoenix
Transmitter Jitter (Pulse Width Jitter)	Automated using SigTest Phoenix
Transmitter Preset	Automated using SigTest Phoenix
Transmitter Initial Tx Equalization	Add-in card only
Transmitter Link Equalization response	
Receiver Link Equalization	
PLL Bandwidth	Add-in card only
Reference Clock Jitter	System only - new for PCIe® 5.0 compliance
PCB Impedance	Informative only – VNA test

(PCI Express 5.0 PHY test spec, Rev 0.9)

Add-In Card Receiver Test

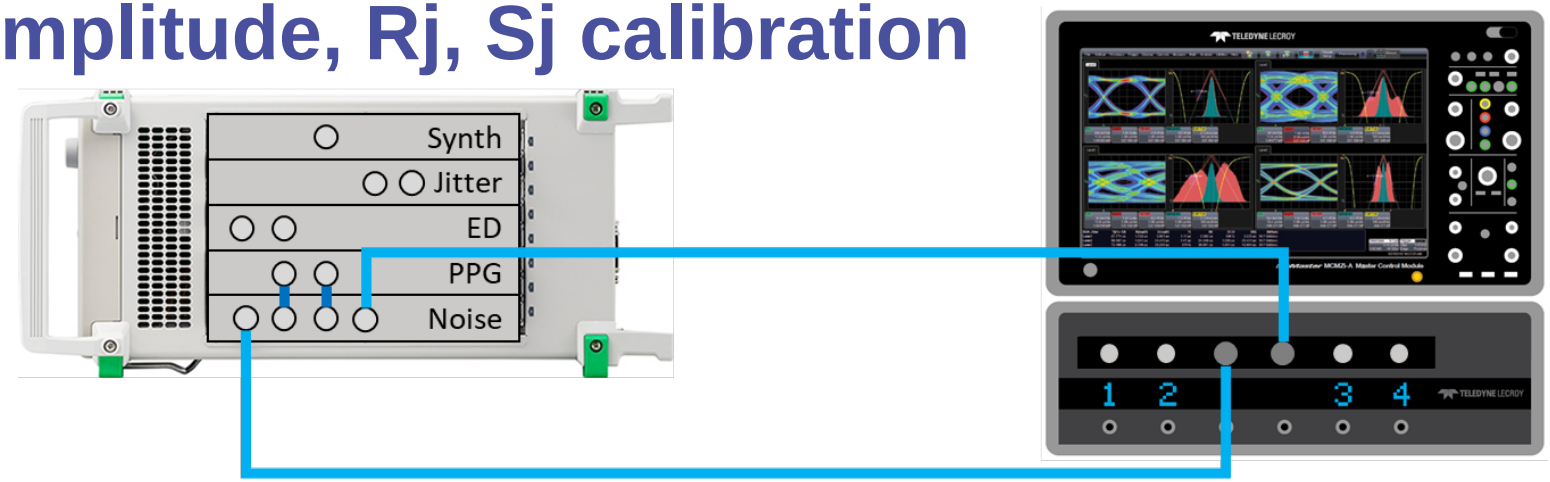
We want to calibrate the Rx signal here:
Root-complex Tx after worst-case (26.5 dB) loss



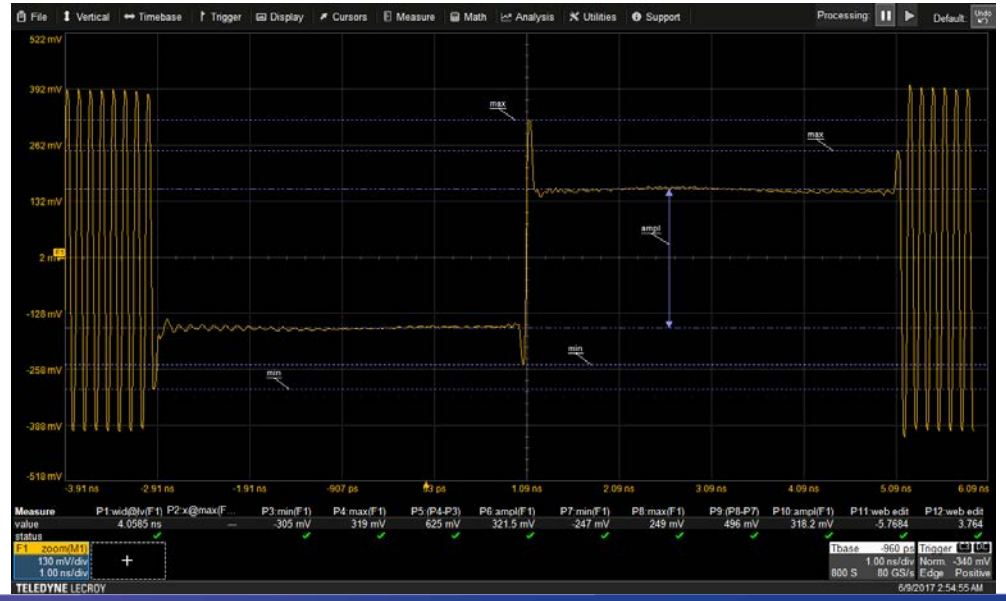
Receiver Test “Philosophy”

1. Use oscilloscope to calibrate BERT output for:
   - Correct voltage swing and emphasis presets
   - Maximum jitter permitted at a **compliant** transmitter
2. Add an appropriate loss channel such that:
   - The transmitter and receiver equalization are both working as hard as possible to recover an open eye at the receiver (scope)
   - The eye width and height are **barely** above the target at the receiver (scope)
3. Change BERT transmitter settings (jitter, noise, amplitude) to achieve target EH/EW values at the receiver (scope)
4. Remove scope and place DUT in system – BERT links with DUT and requires it to negotiate correct transmitter equalization
5. Perform BER test

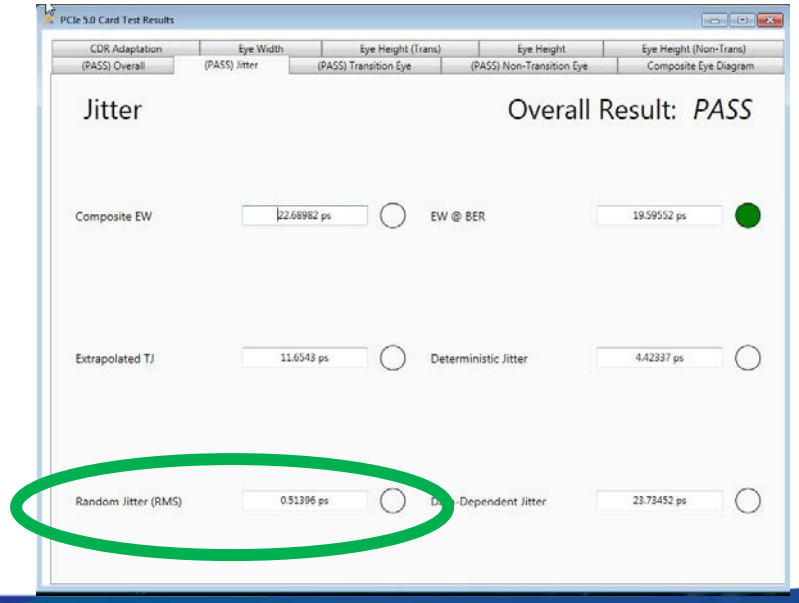
Add-in Card Receiver Test
Preset, Amplitude, Rj, Sj calibration



Preset + amplitude calibration

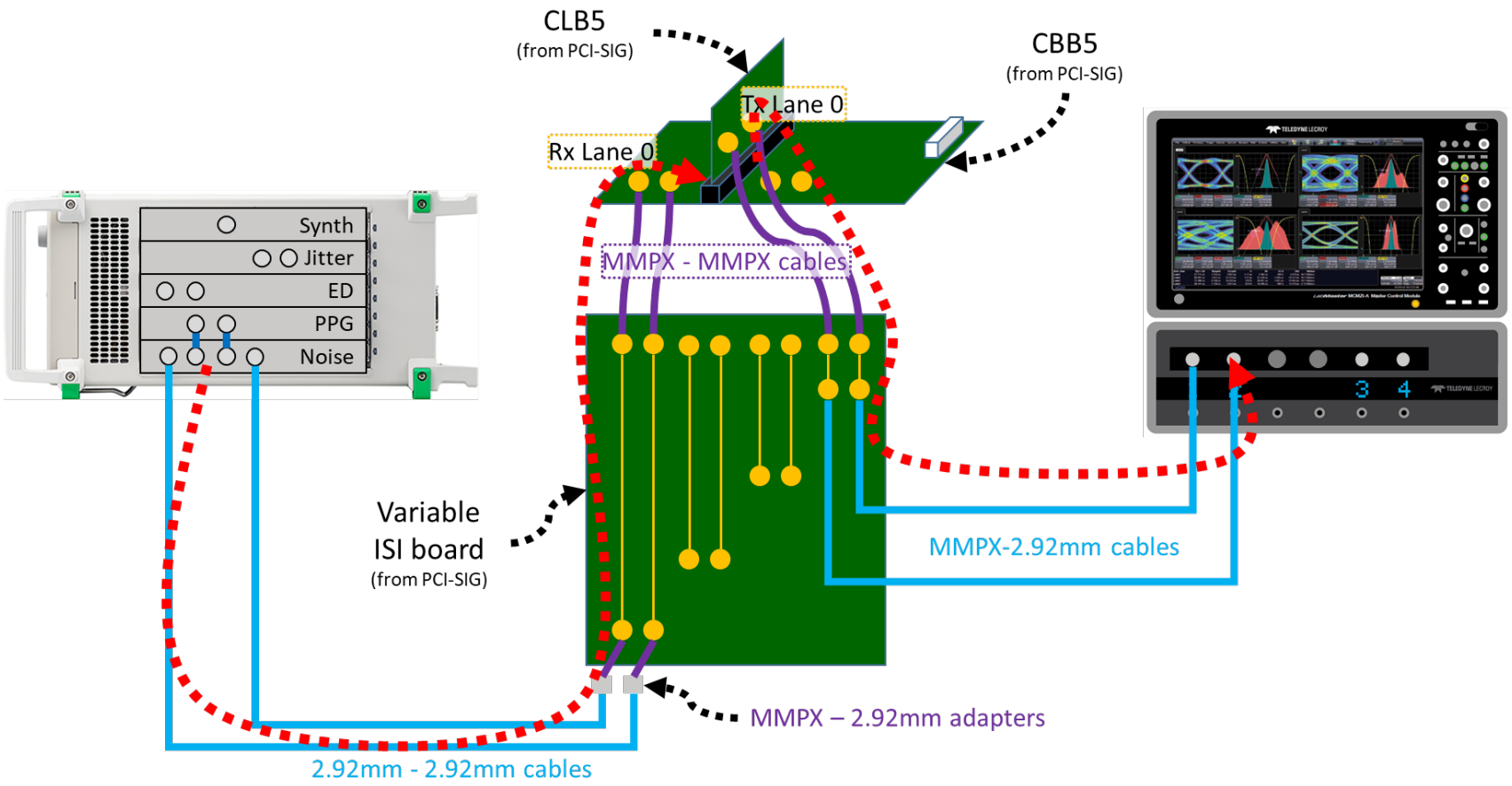


Jitter calibration



Add-in Card Receiver Test
DMI, CMI calibration

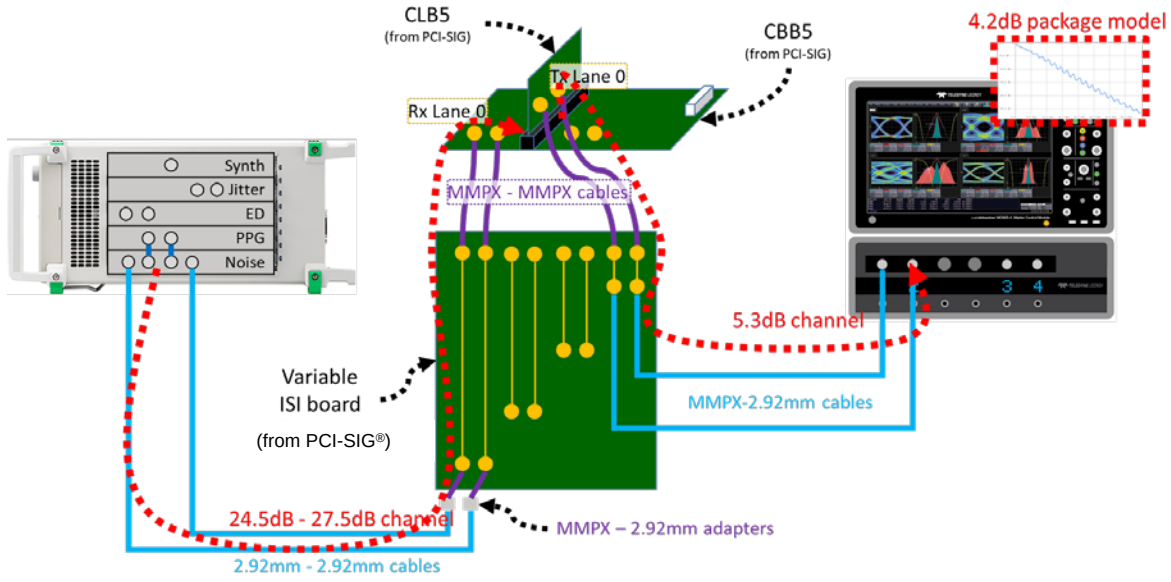
- Differential-mode and common-mode noise are calibrated with a 31.8 dB channel



Add-in Card Receiver Test Eye calibration

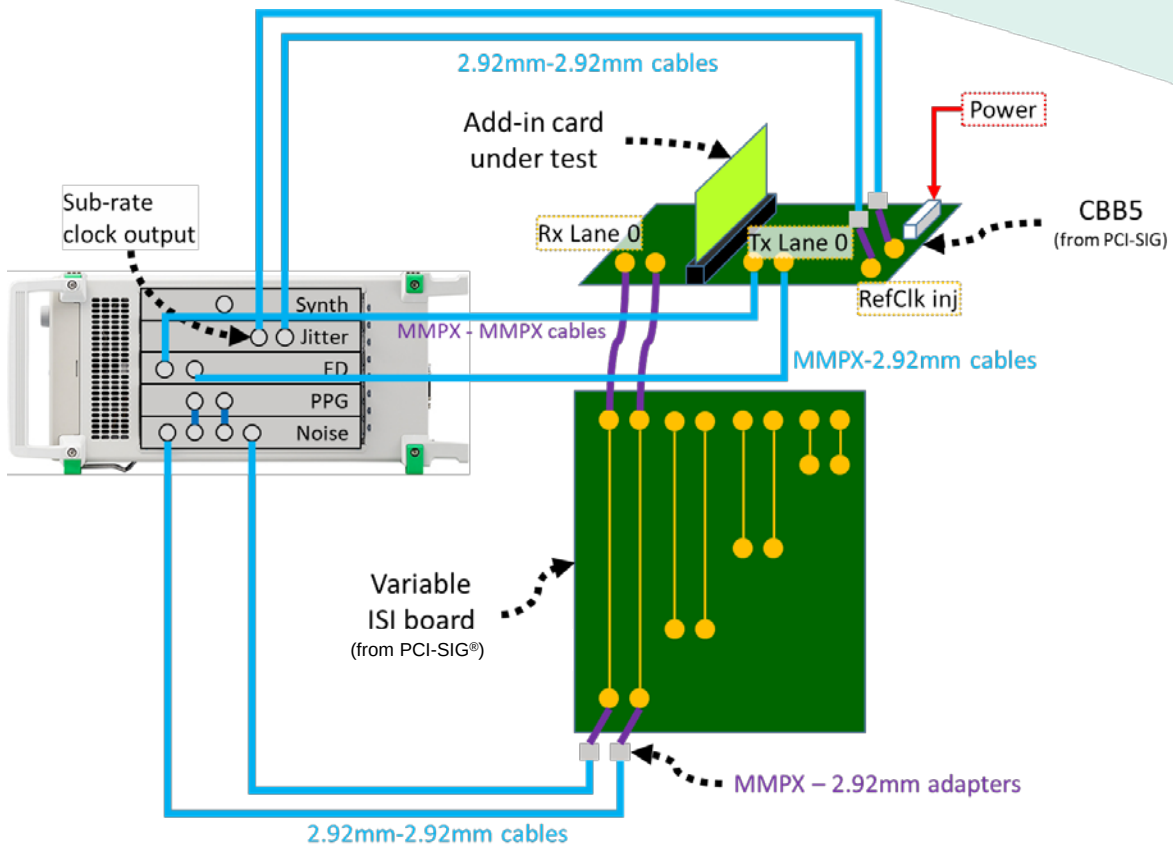
- Objective is to achieve eye height and width targets by varying parameters:
  - Channel loss
  - Sinusoidal Jitter (Sj)
  - Differential mode noise (DMI)
  - Amplitude

Targets	Min	Max
Eye Height (1e-12)	13.5mV	16.5mV
Eye Width (1e-12)	8.875ps	9.975ps



Add-in Card Receiver Test Negotiate into loopback

- The DUT must now be negotiated into loopback by the BERT
  - This **must** happen through the “Recovery path”, where the device performs link training and requests the optimal transmitter preset from the BERT



Training Log Viewer

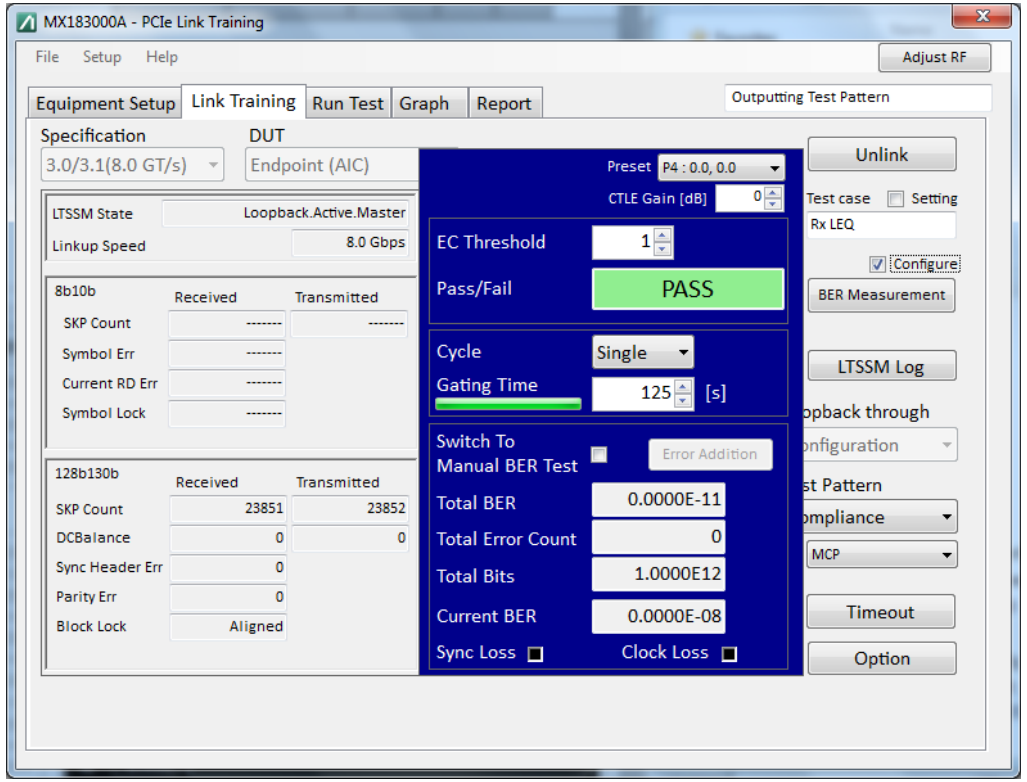
Time [ns]	Δ Time [ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Pre...	Preset	Pre-cursor	Cursor	Post-cursor
300,085,168	128	CONFIGURATION_LINKWIDTH_ACCEPT	2.5	---	---	---	---	---	---	---
300,085,296	3,856	CONFIGURATIONS_LANE_WAIT	2.5	---	---	---	---	---	---	---
300,089,152	128	CONFIGURATIONS_LANE_ACCEPT	2.5	---	---	---	---	---	---	---
300,089,280	4,528	CONFIGURATION_COMPLETE	2.5	---	---	---	---	---	---	---
300,093,808	448	CONFIGURATION_IDLE	2.5	---	---	---	---	---	---	---
300,094,256	24	L0	2.5	---	---	---	---	---	---	---
300,094,280	4,392	RECOVERY_RCVR_LOCK	2.5	---	---	---	---	---	---	---
300,098,672	2,408	RECOVERY_RCVR_CFG_EQTS2	2.5	---	---	---	---	---	---	---
300,101,080	8,619,928	RECOVERY_SPEED	2.5	---	---	---	---	---	---	---
308,721,008	32	RECOVERY_SPEED	8.0	---	---	---	---	---	---	---
308,721,040	8	RECOVERY_RCVR_LOCK	8.0	---	---	---	---	---	---	---
308,721,048	1,070,320	RECOVERY_EQUALIZATION_PHASE1	8.0	---	241	---	---	---	---	---
309,791,368	2,528	RECOVERY_EQUALIZATION_PHASE2	8.0	1	0	0	7	0	0	0
309,793,896	2,000,016	RECOVERY_EQUALIZATION_PHASE2	8.0	1	0	1	5	5	34	9
311,793,912	10,193,408	RECOVERY_EQUALIZATION_PHASE2	8.0	1	0	1	7	5	34	9
321,987,320	2,000,000	RECOVERY_EQUALIZATION_PHASE3	8.0	1	0	1	7	0	0	0
323,987,320	2,000,000	RECOVERY_EQUALIZATION_PHASE3	8.0	1	0	1	4	0	0	0
325,987,320	2,656	RECOVERY_RCVR_LOCK	8.0	---	---	---	---	---	---	---
325,989,976	648	RECOVERY_RCVR_CFG_TS2	8.0	---	---	---	---	---	---	---
325,990,624	3,512	LOOPBACK_ENTRY_MASTER_TS1	8.0	---	---	---	---	---	---	---
325,994,136	10,510,669,...	LOOPBACK_ACTIVE_MASTER	8.0	---	---	---	---	---	---	---
10,836,663,624	0	INITIAL	8.0	---	---	---	---	---	---	---

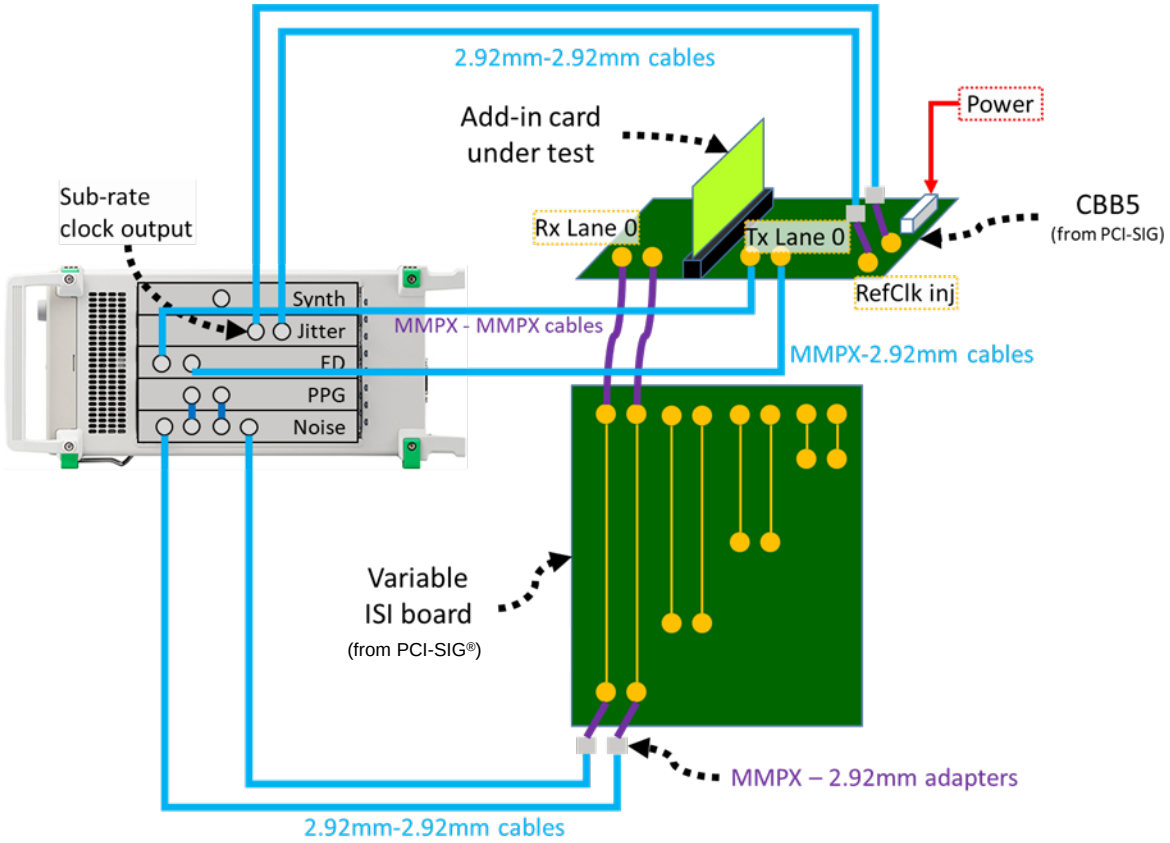
Export CSV Stop Close

RECOVERY_EQUALIZATION_PHASE1	8.0	---	241	---	---
RECOVERY_EQUALIZATION_PHASE2	8.0	1	0	0	7
RECOVERY_EQUALIZATION_PHASE2	8.0	1	0	1	5
RECOVERY_EQUALIZATION_PHASE2	8.0	1	0	1	7
RECOVERY_EQUALIZATION_PHASE3	8.0	1	0	1	7
RECOVERY_EQUALIZATION_PHASE3	8.0	1	0	1	4
RECOVERY_RCVR_LOCK	8.0	---	---	---	---
RECOVERY_RCVR_CFG_TS2	8.0	---	---	---	---
LOOPBACK_ENTRY_MASTER_TS1	8.0	---	---	---	---
LOOPBACK_ACTIVE_MASTER	8.0	---	---	---	---

Add-in Card Receiver Test Perform BER test

- Once in loopback, a BER test is run
- A PASS is defined as no more than one error in 4 x 10^{12} bits





PLL Bandwidth Test

(ADD-IN CARD ONLY)

PCI Express® Transmitter PLL Bandwidth

Test name	Notes
Lane Margining Tests	Protocol Test runs on Protocol Exerciser
Link Layer Tests	Protocol Exerciser
Transaction Layer Tests	Protocol Exerciser
Configuration Space Tests (PCIECV)	Runs on PC
Transmitter Signal Quality	Automated using SigTest Phoenix
Transmitter Jitter (Pulse Width Jitter)	Automated using SigTest Phoenix
Transmitter Preset	Automated using SigTest Phoenix
Transmitter Initial Tx Equalization	Add-in card only
Transmitter Link Equalization response	
Receiver Link Equalization	
PLL Bandwidth	Add-in card only
Reference Clock Jitter	System only - new for PCIe® 5.0 compliance
PCB Impedance	Informative only – VNA test

(PCI Express_5.0 PHY test spec, Rev 0.9)

PLL Bandwidth Overview

- “The test verifies that the add-in card PLL bandwidth and peaking are within the limits allowed by the PCI Express® specifications”

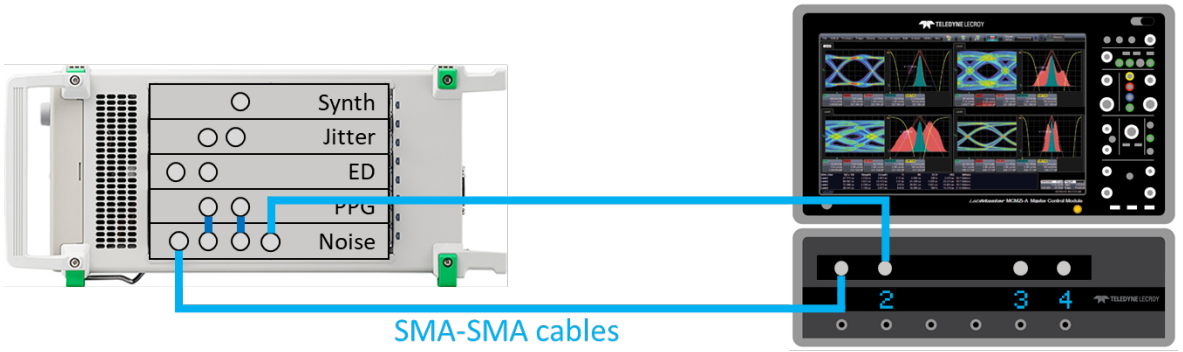
- This is essentially a jitter transfer function measurement, with the intention of checking:
  - That the -3dB point of the DUT’s jitter transfer function is within an acceptable frequency range
  - That the DUT’s jitter transfer function does not have excessive peaking

- To perform this test, we use the BERT’s output to apply calibrated amounts of jitter to the reference clock used by the DUT

PLL Bandwidth: Calibration

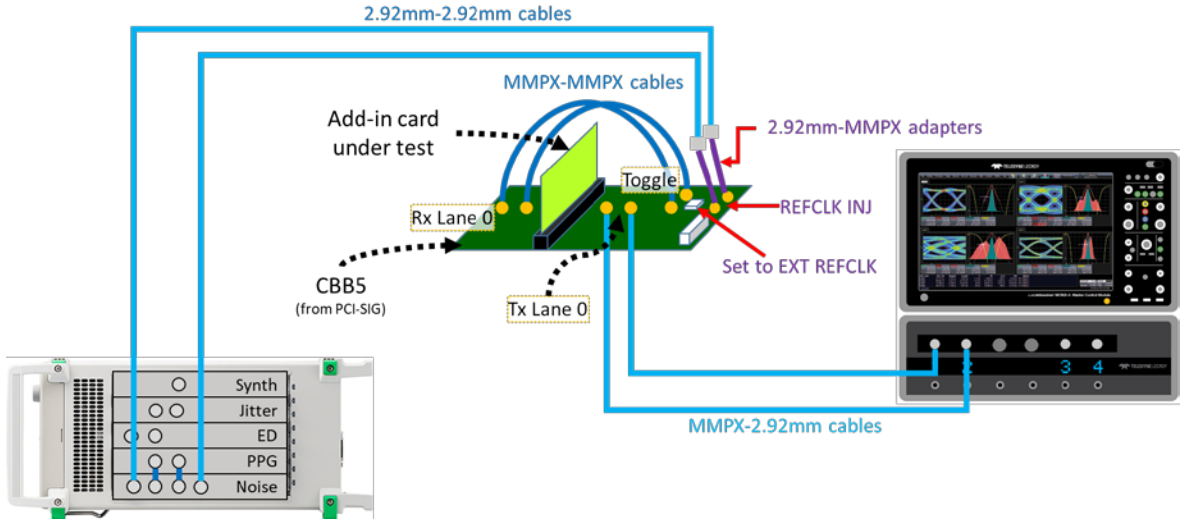
- Apply a defined amount of sinusoidal jitter (Sj) at various frequencies across the PLL bandwidth measurement range to a 100MHz clock

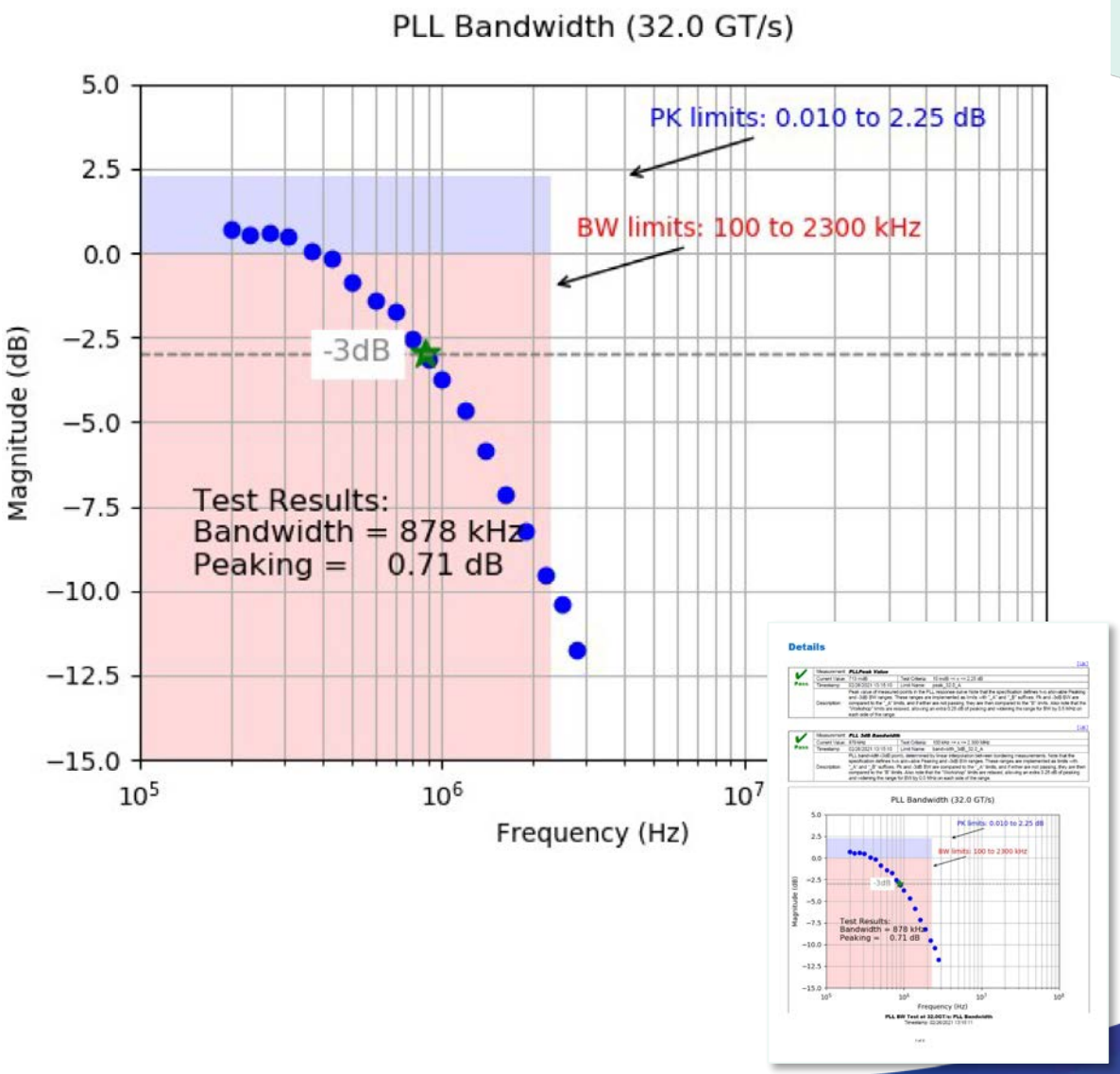
- Measure the applied jitter at each frequency using the oscilloscope



PLL Bandwidth: Test

- For each applied calibrated Sj value, measure the periodic jitter (Pj) at the device transmitter
- Plot a curve of the jitter transfer for each frequency, and compare to the specification limits





Reference Clock Jitter Test

(SYSTEM ONLY)

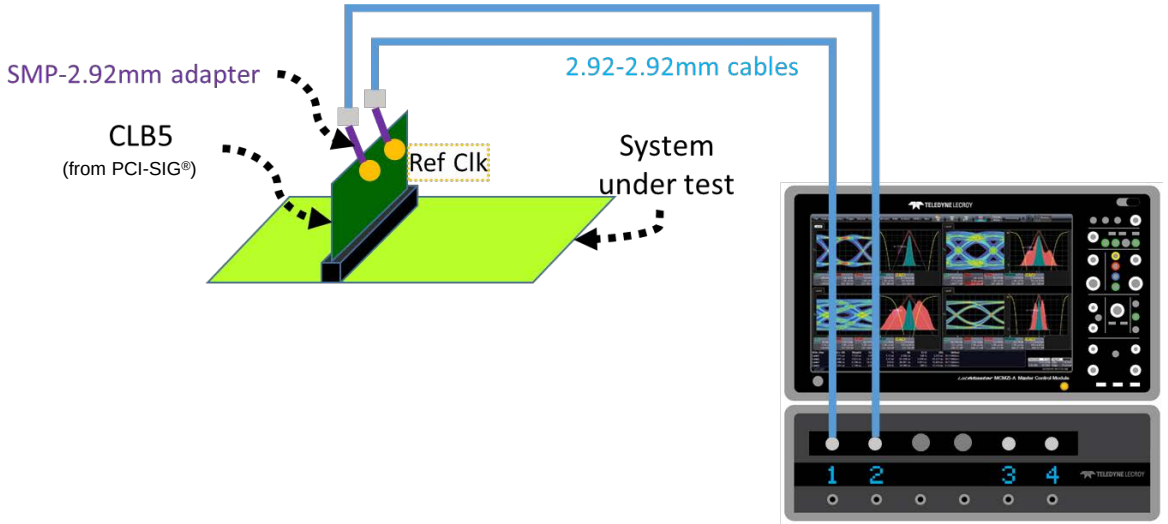
PCI Express® Transmitter Reference Clock Jitter Test

Test name	Notes
Lane Margining Tests	Protocol Test runs on Protocol Exerciser
Link Layer Tests	Protocol Exerciser
Transaction Layer Tests	Protocol Exerciser
Configuration Space Tests (PCIECV)	Runs on PC
Transmitter Signal Quality	Automated using SigTest Phoenix
Transmitter Jitter (Pulse Width Jitter)	Automated using SigTest Phoenix
Transmitter Preset	Automated using SigTest Phoenix
Transmitter Initial Tx Equalization	Add-in card only
Transmitter Link Equalization response	
Receiver Link Equalization	
PLL Bandwidth	Add-in card only
Reference Clock Jitter	System only - new for PCIe® 5.0 compliance
PCB Impedance	Informative only – VNA test

(PCI Express 5.0 PHY test spec, Rev 0.9)

Reference Clock Jitter

- This is a new *compliance* test for PCIe® 5.0 specification
  - It has existed in Base (non-compliance) testing for many generations
- Tests the jitter of the system's 100 MHz reference clock
- Process is relatively simple:
  - Acquire a long (~ 2 ms) waveform of reference clock using 5 GHz bandwidth limit on oscilloscope
  - Pass to external clock jitter tool for analysis
- Clock jitter tool emulates 32 reference PLL "templates"
- System must pass reference clock jitter tests for **all** 32 templates



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