PCI-SIG® 2023 Update

Al Yanes, President and Board Chair

June 2023

PCI-SIG® Snapshot

- Organization that **defines the PCI Express® (PCIe®) I/O bus specifications and related form factors**
- PCI-SIG began 31 years ago in 1992
- The PCIe specification was first released in 2003
- **950** member companies located worldwide
  - Highest number of member companies in thirteen years
- Creating specifications and mechanisms to **support compliance** and **interoperability**

Board of Directors
2023 –2024

AMD
arm
DELL EMC
IBM
intel
KEYSIGHT TECHNOLOGIES
NVIDIA
Qualcomm
SYNOPSYS®
Silicon to Software™

PCI-SIG® DevCons & Highlights

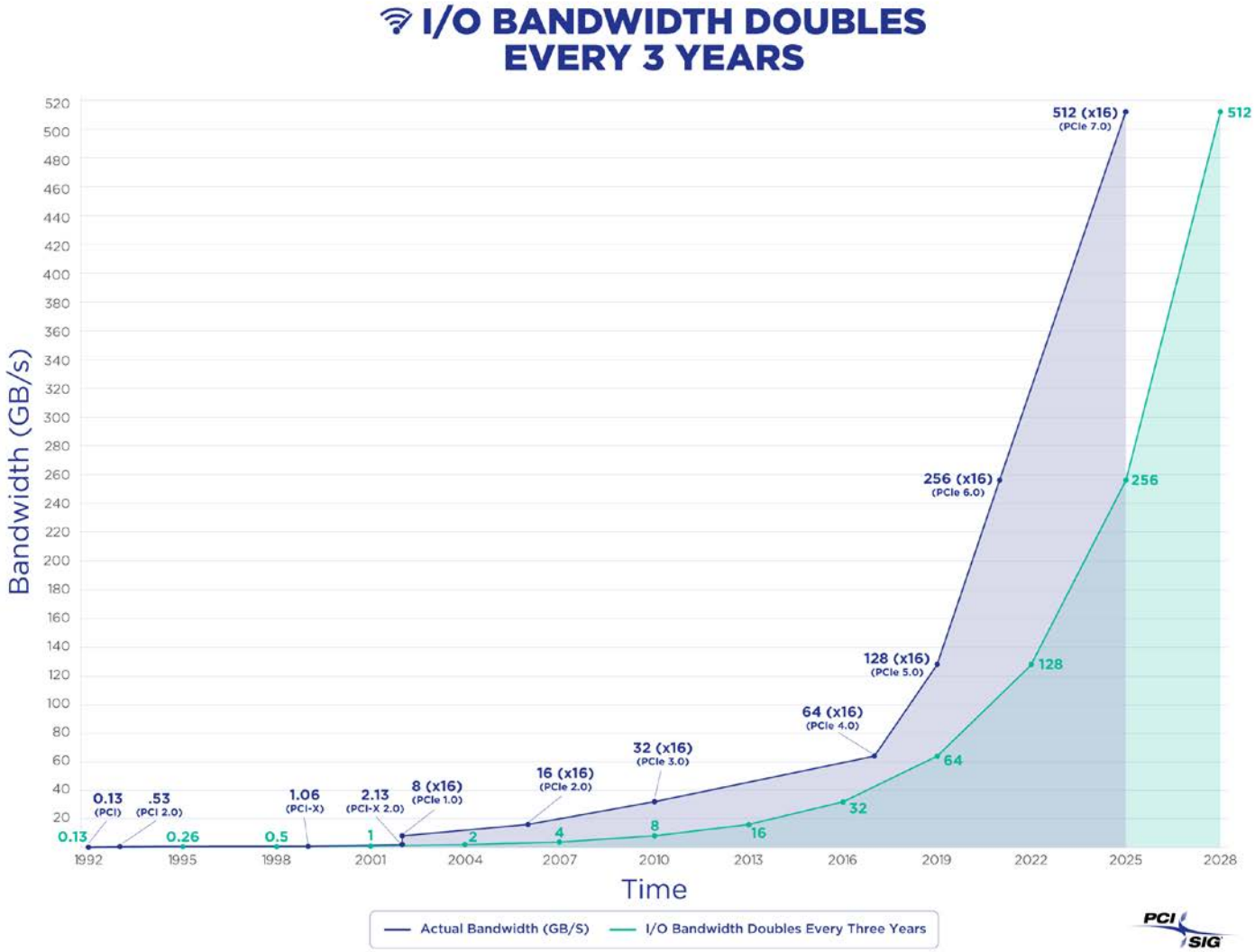
- Why does PCI-SIG host DevCons?
  - The PCI-SIG Developers Conferences are a free members only event to help members develop and bring to market new products utilizing PCI Express® technology. It is an opportunity to learn directly from the industry's PCIe® technology experts and participate in technical trainings to gain best practices to improve product roll-out and interoperability.

- PCI-SIG DevCon attendance is stronger than ever:
  - **335 in person attendees** at U.S. DevCon 2022
  - **674 in person attendees** at Taiwan 2023 DevCon, making it the top attended in person DevCon in history

- DevCon global expansion:
  - In addition to our U.S. DevCons, recent DevCons occurred in **Japan, South Korea, Israel and Europe**

- DevCon presentation topic trends / highlights:
  - Explain the **PCIe 5.0 compliance program**
  - Finalizing the **PCIe 6.0 compliance program**
  - Finding innovative ways to **address new challenges** (i.e. PAM4, Flit mode, etc.)

PCI-SIG® Roadmap



PCIe® Speeds/Feeds - Pick Your Bandwidth

- **Flexible to meet needs from handheld/client to server/HPC**
- **~Max Total Bandwidth = Max RX bandwidth + Max TX bandwidth**
- **35 Permutations yielding 11 unique bandwidth profiles**
- **Encoding overhead and header efficiency not included**

Specifications	Lanes				
	x1	x2	x4	x8	x16
2.5 GT/s (PCIe 1.x +)	500 MB/S	1 GB/S	2 GB/S	4 GB/S	8 GB/S
5.0 GT/s (PCIe 2.x +)	1 GB/S	2 GB/S	4 GB/S	8 GB/S	16 GB/S
8.0 GT/s (PCIe 3.x +)	2 GB/S	4 GB/S	8 GB/S	16 GB/S	32 GB/S
16.0 GT/s (PCIe 4.x +)	4 GB/S	8 GB/S	16 GB/S	32 GB/S	64 GB/S
32.0 GT/s (PCIe 5.x +)	8 GB/S	16 GB/S	32 GB/S	64 GB/S	128 GB/S
64.0 GT/s (PCIe 6.x +)	16 GB/S	32 GB/S	64 GB/S	128 GB/S	256 GB/S
128.0 GT/s (PCIe 7.x +)	32 GB/S	64 GB/S	128 GB/S	256 GB/S	512 GB/S

+ = data rate supported by this and subsequent spec revisions.

PCI-SIG® Specification Progress: At a Glance

- Specification release and compliance program tracking to 3 years
- Early products are available prior to compliance program dates, but product availability generally tracks with compliance program dates

Specification Revision	Version 1.0 of Specification Completed	Compliance Program Live
PCIe 4.0	October 2017	August 2019
PCIe 5.0	March 2019	April 2022
PCIe 6.0	January 2022	Est. March 2024
PCIe 7.0	Est. for 2025	2027

PCI Express® 7.0 Specification & Status

PCIe 7.0 specification, version 0.3 is now live for PCI-SIG members; The full PCIe® 7.0 specification is targeted for release in 2025

- **What does Version 0.3 mean?**
  - The first review draft of the specification is complete and has received work group approval

Feature Goals:

- Delivering 128 GT/s data rate and up to 512 GB/s bi-directionally via x16 configuration
- Utilizing PAM4 signaling
- Defining the channel parameters
- Continuing to deliver the low-latency and high-reliability targets
- Improving power efficiency
- Maintaining backwards compatibility with all previous generations of PCIe technology

Revision	Max Data Rate	Encoding	Signaling
PCIe 7.0 (2025)	128.0 GT/s	1b/1b (Flit Mode*)	PAM4
PCIe 6.0 (2022)	64.0 GT/s	1b/1b (Flit Mode*)	PAM4
PCIe 5.0 (2019)	32.0 GT/s	128b/130b	NRZ
PCIe 4.0 (2017)	16.0 GT/s	128b/130b	NRZ
PCIe 3.0 (2010)	8.0 GT/s	128b/130b	NRZ
PCIe 2.0 (2007)	5.0 GT/s	8b/10b	NRZ
PCIe 1.0 (2003)	2.5 GT/s	8b/10b	NRZ

(*Flit Mode also enabled in other Data Rate with their respective encoding)

PCI Express® 6.0 Specification & Status

PCIe® 6.0 specification was released to members on January 11, 2022

Key Features:

- 64 GT/s raw data rate and up to 256 GB/s via x16 configuration; doubles the bandwidth and power efficiency from PCIe 5.0 specification (32GT/s)
- Pulse Amplitude Modulation with 4 levels (PAM4) signaling and leverages existing PAM4 already available in the industry
- Lightweight Forward Error Correct (FEC) and Cyclic Redundancy Check (CRC) mitigate the bit error rate increase associated with PAM4 signaling
- Flit (flow control unit) based encoding supports PAM4 modulation and enables more than double the bandwidth gain
- Updated Packet layout used in Flit Mode to provide additional functionality and simplify processing
- Maintains backward compatibility with all previous generations of PCIe architecture

Adoption:

- Various PCIe 6.0 specification enabled products available in the industry; visit our sponsors for more information

Compliance Program Progress:

- FYI Testing targeted for Q1 2024

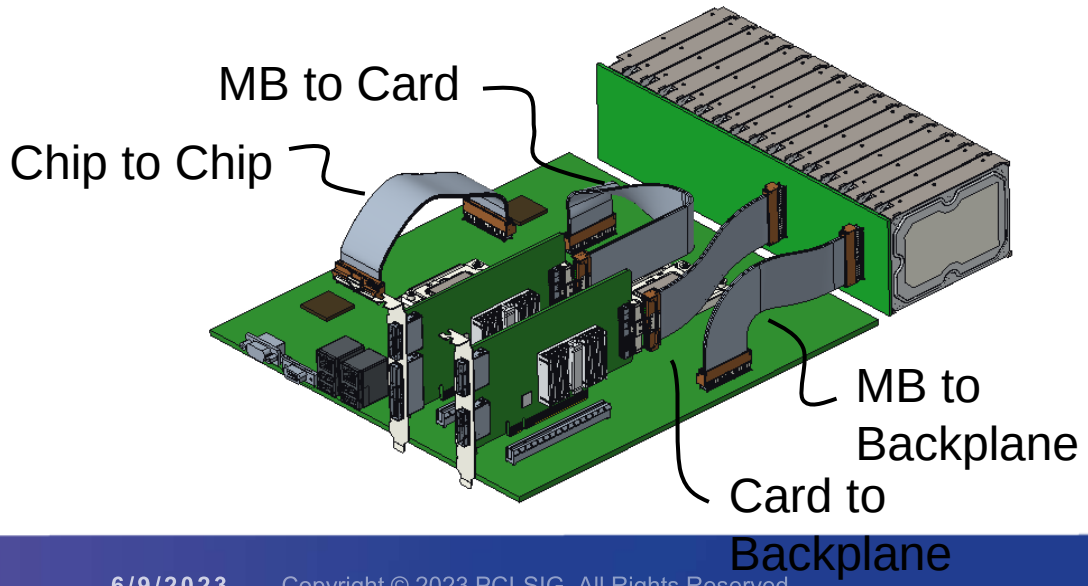
PCI Express® 5.0/6.0 Cabling Specifications

Internal and external cables targeted for release in Q4 2023

Motivation for New Cabling Specifications

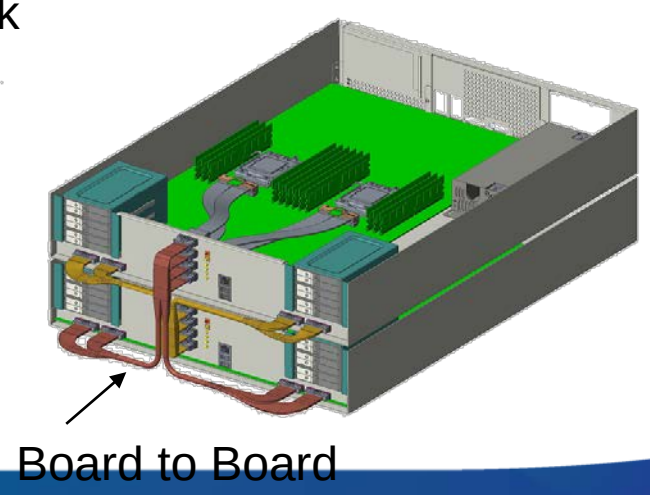
- High-bandwidth applications require longer channel reach and topological flexibility
- At 32 and 64 GT/s, PCB loss reduces channel reach and limits platform flexibility
- Cable is another option to give flexibility to system designers and boost innovation
- Targeted applications: data centers, servers, storage, networking and accelerators

Internal Cable Usages



External Cable Usages

- Connecting boards within a rack
- Rack-to-rack



PCIe® Architecture: One Interconnect – Infinite Opportunities

HPC / Cloud

Data Center / Enterprise Servers

Artificial Intelligence / Machine Learning

Automotive

Internet of Things

Military / Aerospace

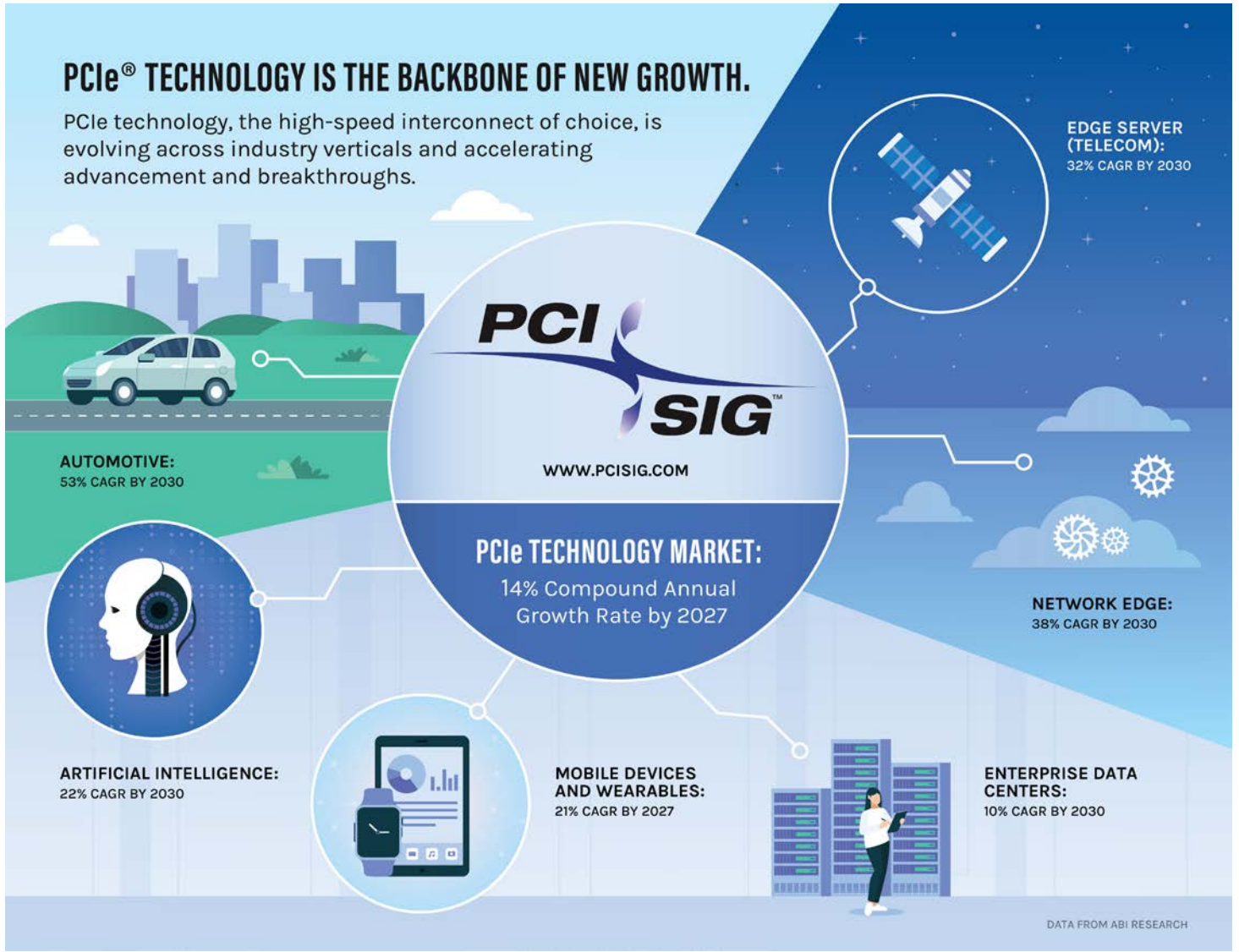
Storage

PCIe® Technology Market Data Forecasted Through 2027

Key Highlights from the Report Developed by ABI Research:

- **Automotive and network edge** verticals offer the highest growth opportunities for PCIe technology, with total addressable market (TAM) compound **annual growth rates (CAGRs) of 53% and 38**
- High-performance applications such as **data centers will contribute to sustained long-run demand** for new PCIe generation deployment. Performance is not the only driver of PCIe technology adoption, as verticals increasingly look at **power efficiency, security and "time-to-value" as crucial issues**
- **AI industry adoption will be high**, as PCIe technology offers decision makers agility through forwards and backwards compatibility, **improving time-to-value and lowering deployment risk**
- PCIe technology will **perform well in the mobile devices vertical**, as the quick pace of market innovation will **necessitate a discrete component interconnect**
- **The PCIe 6.0 specification low power feature (L0p) will be a major driver of deployment**, as power efficiency becomes a central strategy for adopters with a closer **focus on sustainability and lowering operational costs**

PCIe® Technology Market Forecast



Engage with PCI-SIG® on Social Media

@PCI_SIG

https://www.linkedin.com/company/pcisig/

PCI-SIG

https://pcisig.com/blog

https://www.brighttalk.com/channel/17656/

Q&A

Sponsor Slides

Allion

Through this sponsorship, Allion Labs will showcase our unique PCI Express® 5.0 fixtures and PCIe® Measurement System (APMS), while also providing relevant technical consultations. PCIe Measurement System (APMS) is an automated verification solution exclusively developed by Allion. This solution speeds up PCIe testing, shortens the test cycle, and improves the productivity and turnover rate of measurement equipment.

Allion PCIe® Measurement System (APMS) Advantages

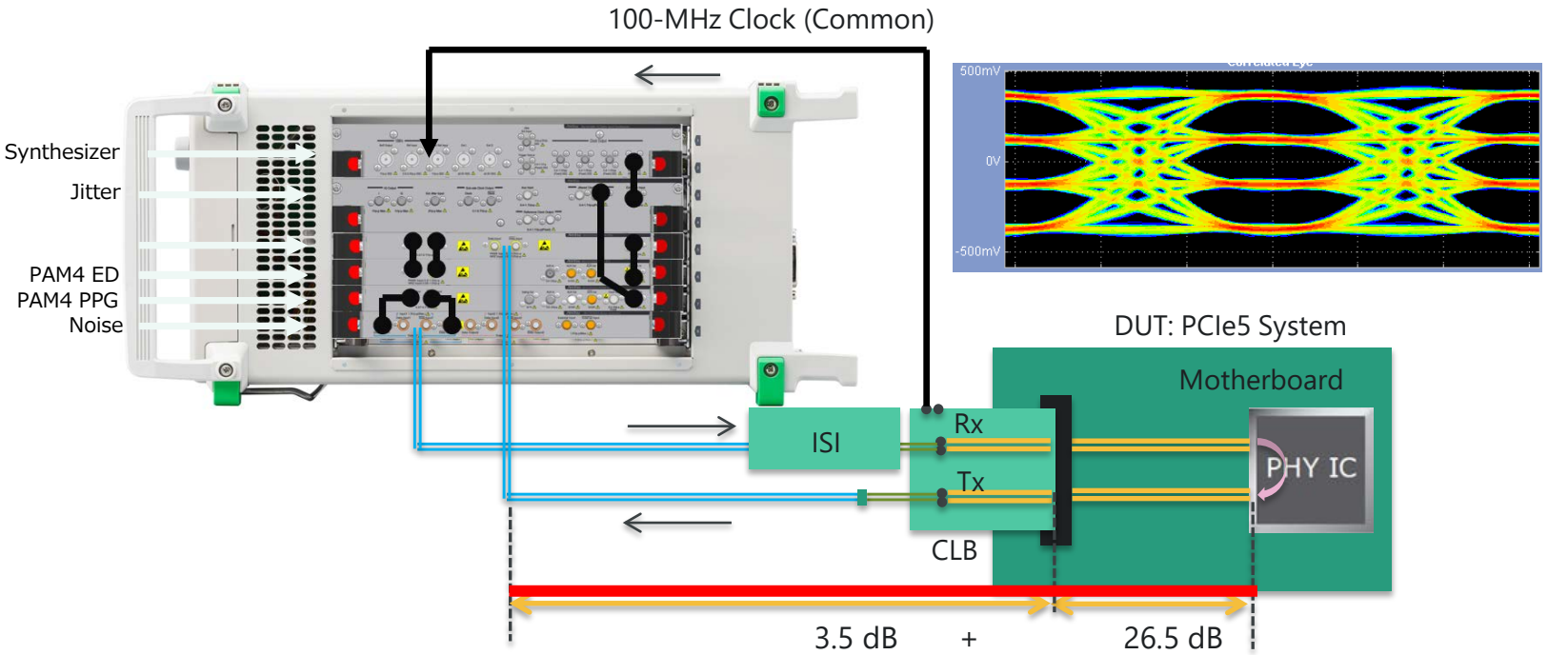
- **Higher Time Efficiency**
  Shortens project schedule and speeds up turnaround time
- **Consistent Quality**
  Get consistent test quality without human errors
- **Expand Equipment Usage**
  Maximizes the utilization of high-value investment

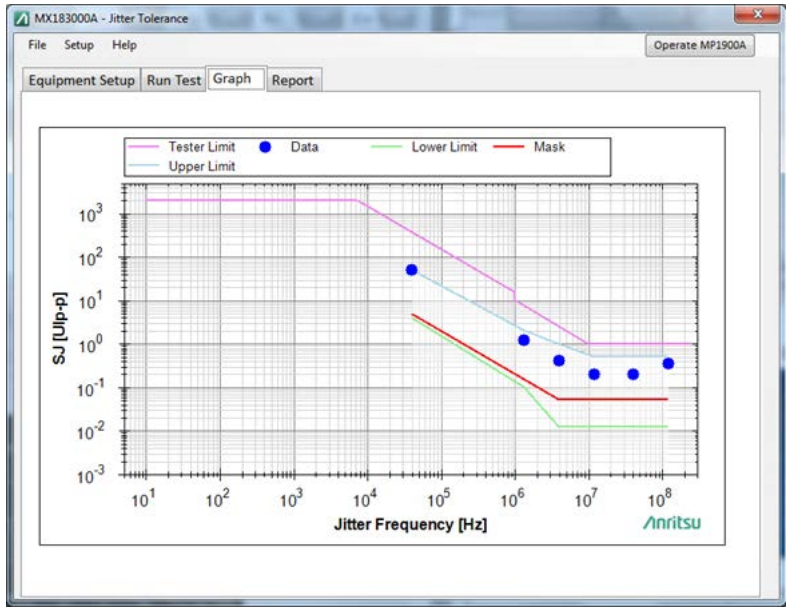
Allion PCIe® Measurement System (APMS) Advantages

- **PCIe CBB**
  CEM, M.2, U.2/U.3, OCP NIC 3.0 (Backward Compatible for E1/E3)
- **PCIe CLB**
  CEM, M.2, U.2/U.3, EDSFF E1/E3, OCP NIC 3.0

Anritsu

1. PCIe® 6.0 (64GTPS) CEM and Base RX LEQ Compliance Test
   - PAM4 BER and Jitter Tolerance test
   - Flit FEC Burst Error Analysis (Raw and Post FEC BER/SER)
2. PCIe 5.0 Optical Signal Transmission for OBO over Internal Optical Fiber Cable





Granite River Labs

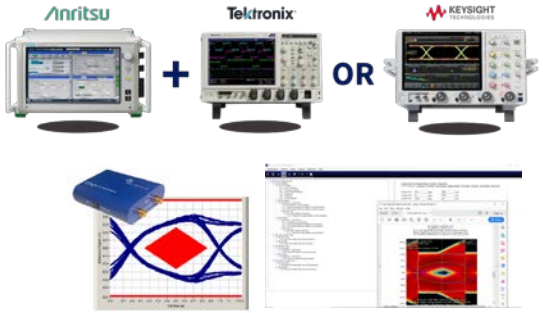
Gold Sponsor | Booth: #11

GRL PCI Express®
Test Services & Solutions

Comprehensive Lab Services and Software Automation Solutions for PCIe compliance testing and debugging

GRL PCIe® 6.0 Test Automation Software Solutions

Compatible with Keysight & Tektronix Scopes and Anritsu MP1900A BERT

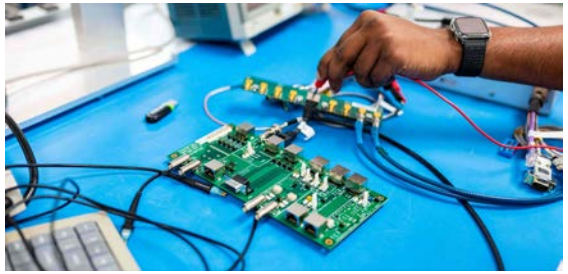


- GRL PCI Express® Transmitter Test Software (GRL-PCIE-TX)
- PCI Express® 6.0 Base Specification Receiver Test Software (GRL-PCIE6-BASE-RXA)
- GRL PCI Express® PLL Test Software (GRL-PCIE-PLL)

GRL PCIe 6.0 Test Services – 9 Labs World-Wide

GRL has the expertise and equipment to test & debug your PCIe 6.0 design

- IC Characterization
- Electrical Compliance and Stress Testing
- Protocol Compliance
- Configuration Space
- Platform BIOS
- Performance Benchmarking



graniteriverlabs.com

Discover the software offerings that give developers freedom to use the test equipment of their choice here

iPASS
Professional Technical & Methodology Provider

PCI SIG

iPasslabs Technology Co. Ltd. Booth 4

Services:

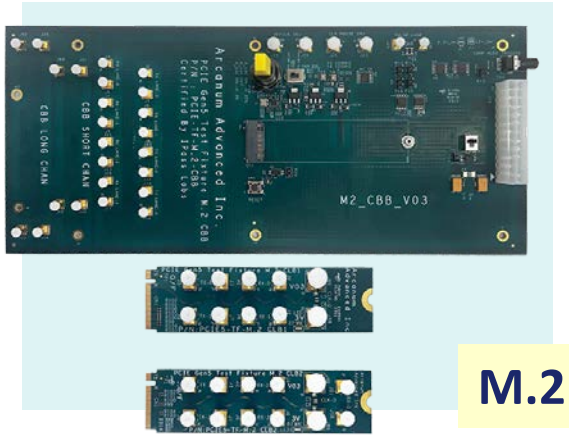
- ✓ Simulation
- ✓ Validation
  - PCIe® 1.0/2.0 3.0/4.0/5.0

Products:

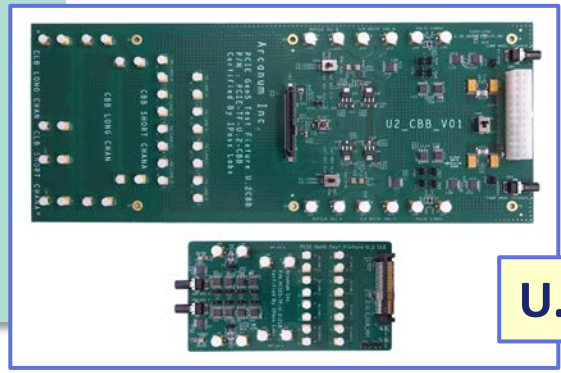
- ✓ PCIe 5.0 Test Fixtures
  - M.2
  - U.2(NVMe®)
  - U.3(NVMe)
  - OCP3.0
  - EDSFF(E1.S/E1.L)

Manufactured by Arcanum Advanced

arcanum Advanced Inc.



M.2



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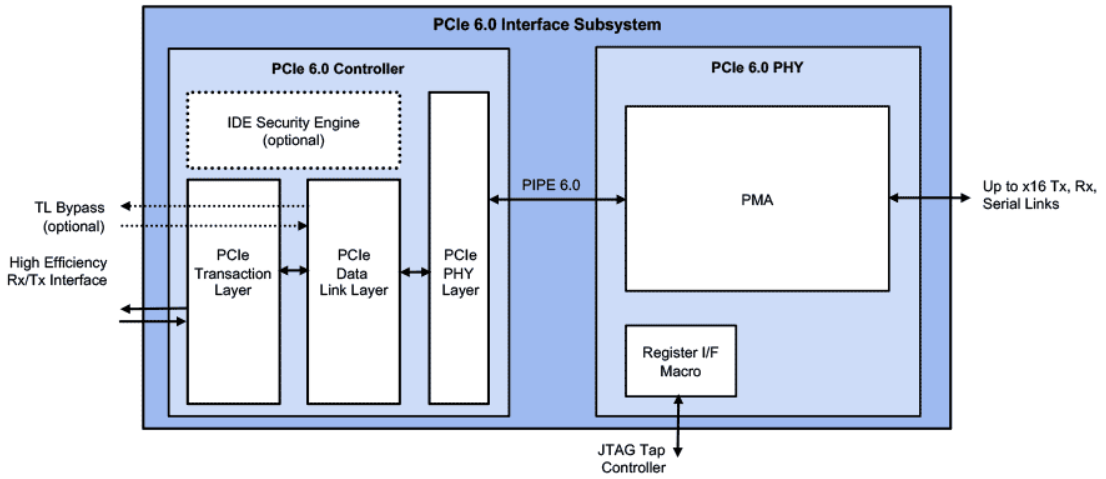
Rambus Booth #8

- PCIe® 6.0 Interface Subsystem (PHY and Controller IP)*
- PCIe 5.0 Interface Subsystem (PHY & Controller IP)
- PCIe 5.0 Retimer IP
- Bring up and test solutions
  - Inspector for PCIe 5.0
  - PCIe 5.0 architecture HOST
  - PCIe 5.0 architecture ENDPOINT
  - XpressAGENT
- PCIe 5.0 Multi-port Switch IP



PCIe 6.0 Interface Subsystem Solution

***Visit us for live demos at Rambus Booth #8**

Synopsys, Gold Sponsor

Synopsys Booth #19

- **Synopsys 128GT/s PHY TX Performance Using Tektronix Oscilloscope**
  Synopsys and Tektronix will be taking a sneak peek at the upcoming PCIe 7.0 data rate of 128 GT/s
- **PCIe® 6.0 End-to-End Hardware Linkup and Performance**
  Synopsys PCIe 6.0 Controller and PHY IP in an end-to-end host to device system, using Teledyne LeCroy's Interposer and Analyzer showing impact of payload size on throughput
- **Synopsys Verification IP for PCIe 6.0 & CXL 3.0**
  Industry leading PCIe 6.0 protocol verification solutions including VIP, transactors, speed adaptors, virtual system adaptors, and protocol interface cards for early RTL verification

Don’t miss the Synopsys 128 GT/s PHY TX using Tektronix Oscilloscope

Partner Booths

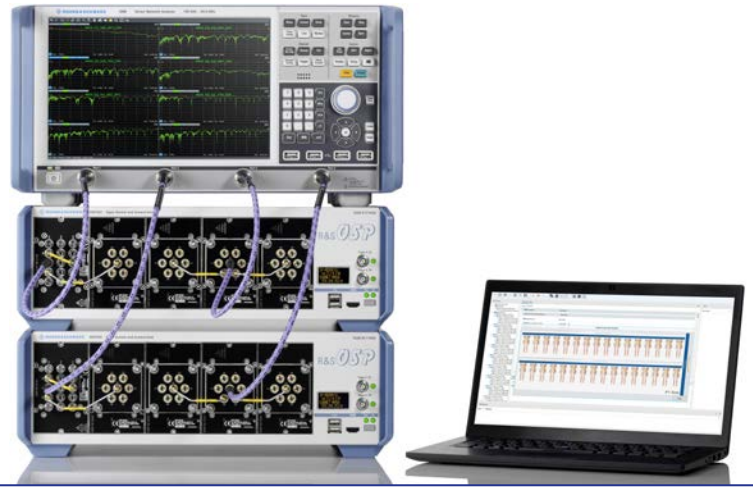
- **Teledyne LeCroy Booth #2**
  Synopsys PCIe 6.0 Controller and PHY IP in an end-to-end host to device system, showing successful link up and detailed performance metrics using Teledyne LeCroy's Interposer and Analyzer

  Synopsys PCIe 6.0 Transmitter and Receiver out-of-the-box Electrical Performance with preset, jitter, signal quality and receiver link equalization tests using Teledyne LeCroy Solutions
- **Tektronix Booth #6**
  Synopsys PCIe 6.0 IP transmitter and receiver showing excellent performance on a PCIe 5.0 ISI channel, using Tektronix’s oscilloscope and Anritsu’s BERT
- **Granite River Labs Booth #11**
  Synopsys PCIe 6.0 receiver performance w/ GRL’s PCIe 6.0 base RX calibration & test SW & Anritsu MP1900A BERT
- **Anritsu Booth #10**
  Synopsys PCIe 6.0 PHY & Controller IP in an end-to-end system showcasing pre-FEC and post-FEC BER with Anritsu BERT and TX performance with Tektronix real time oscilloscope
- **Keysight Booth #14**
  Synopsys PCIe 6.0 TX showing excellent PAM4 Eye measurements & receiver jitter tolerance test with Keysight BERT & Oscilloscope

Rohde & Schwarz

Automated Compliance Test Solution for PCIe® 5.0/6.0 Cable testing

- ZNB43 VNA with OSP320 Switch Matrix
  - 43GHz Bandwidth and expanded port configuration satisfies channel test needs (THRU, NEXT, FEXT) for larger lane configuration (x4,x8,x16)
- ZN-Run Test Software
  - Automates hardware setup in intuitive GUI
  - Calculates parameters (iRL, ccICN, EIPS,etc) and creates comprehensive test report

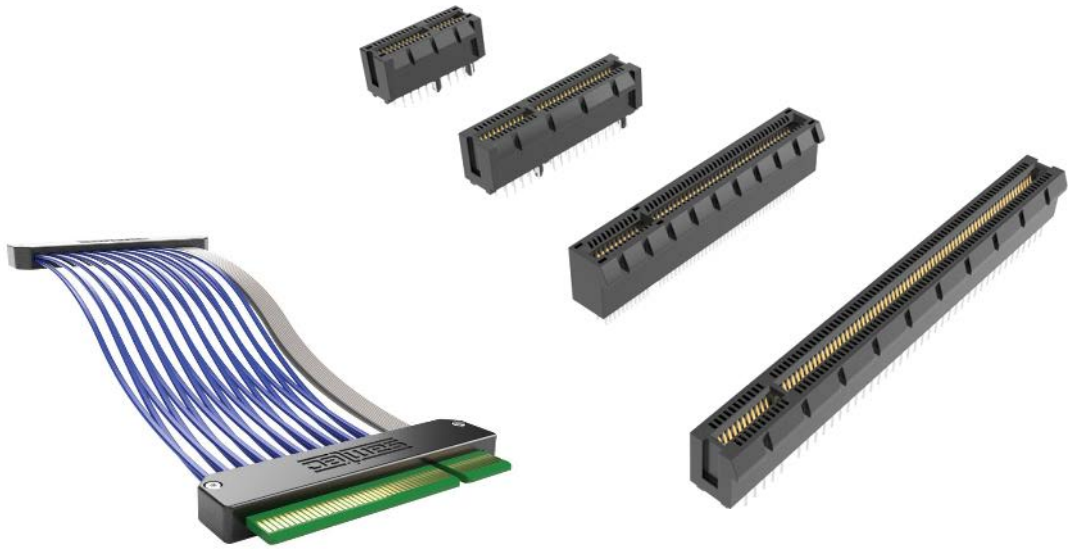


Correlating SI and PI Measurements

- RT-ZPR power rail probe
  - 4 GHz bandwidth, +/- 60V offset, AC coupling option
  - 1:1 attenuation
  - Solder-in and browser
- RTP164 oscilloscope
  - 16 GHz analog bandwidth
  - Live eye diagram with digital hardware CDR
  - Real-time de-embedding
- Advanced model-based signal integrity software
  - Accurate measurements on highly stressed eyes
  - Step/frequency response measurement

PCI Express® Interconnect Solutions

- A global manufacturer of a broad line of electronic interconnect solutions
- PCIe® 5.0 Capable Edge Card Sockets and Cables Assemblies
  - PCIe 6.0 solutions under development
- PCIe 4.0 Adaptor Card with Optical FireFly™
  - PCIe 5.0 solutions under development
- For more information, please visit: http://www.samtec.com/pcie



Teledyne LeCroy

New Features for PCIe® Protocol Test and Development

- PCI Express® 6.0 Protocol Analyzer/ Exerciser
- New Interposers for Protocol Analysis
  - -PCIe 6.0 CEM Interposer
  - -PCIe 6.0 OCP NIC 3.0 Interposer and Host adapter
  - -PCIe 6.0 EDSFF Interposer and Host adapter

New Features for PCIe Electrical Test and Development

- PCI Express 6.0 Base Transmitter and Receiver Testing
  - -PCIe 6.0 Base Tx Measurements
  - -PCIe 6.0 Oscilloscope Decoder
  - -PCIe 6.0 Base Rx Calibration
  - -PCIe 6.0 Base Rx BER/JTOL Tests
  - -Fully Automated PCIe 6.0 Base Tx/Rx Test Solutions

Back-Up Slides & ABI Research Report Vertical TAMs

PCI Express® 5.0 Specification & Status

Released in May 2019

Key Features:

- Doubles bandwidth over PCIe® 4.0 specification to deliver 32 GT/s
- Electrical changes to improve signal integrity and mechanical performance of connectors

Adoption:

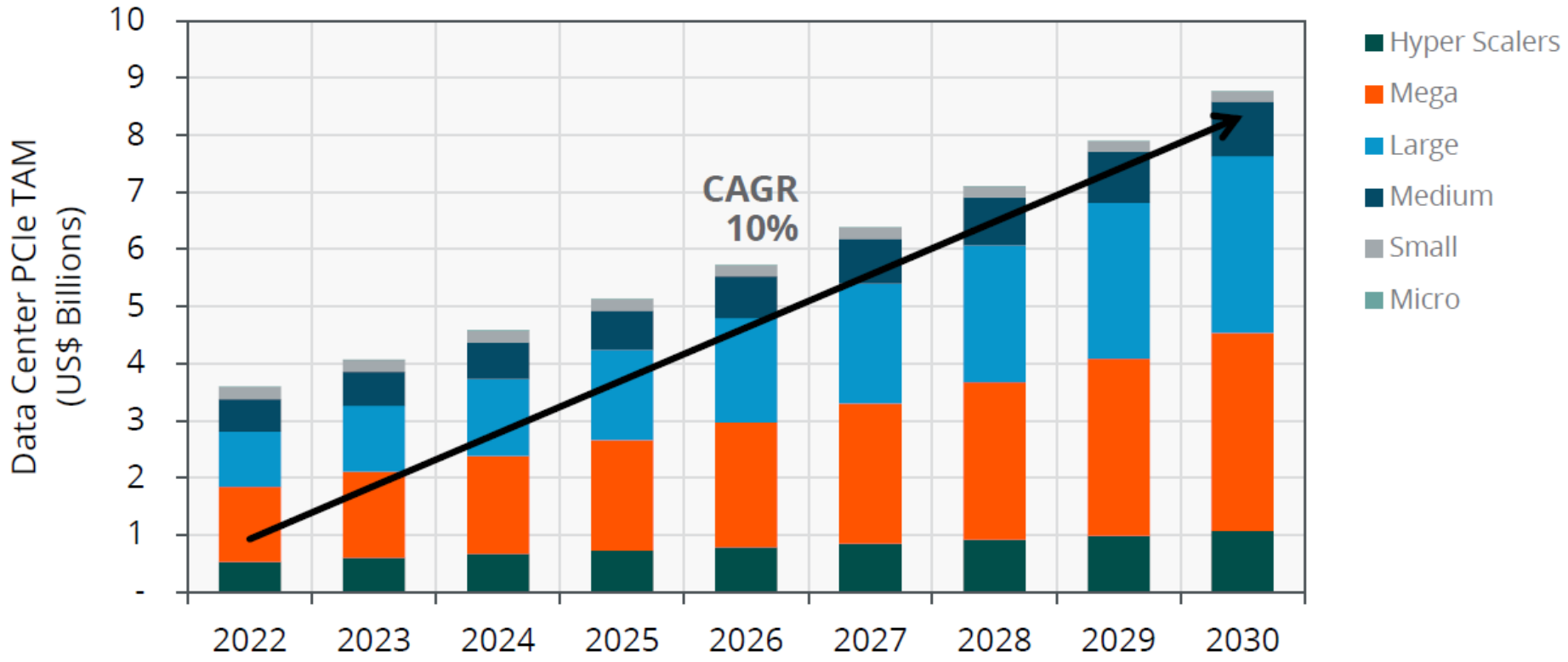
- Silicon ecosystem is available for product development and test equipment is available
- Member companies have publicly announced and are showcasing PCIe 5.0 solutions in Storage, Enterprise, AI/ML and Cloud markets
- Adoption is well under way; growing rapidly due to demand from high-performance applications
- Multiple compliance workshop with PCIe 5.0 testing take place each year; 80+ products currently listed on the Integrators List

PCIe® Revision	Total Channel Insertion Loss Budget	Root Package	CEM Connector	Add-in Card (AIC)	Remaining System Base Board Budget
3.0 (8 GT/s)	22 dB	3.5 dB	1.7 dB	6.5 dB	10.3 dB
4.0 (16 GT/s)	28 dB	5.0 dB	1.5 dB	8.0 dB	13.5 dB
5.0 (32 GT/s)	36 dB	9.0 dB	1.5 dB	9.5 dB	16.0 dB

Data Center, Edge, And Telcos

Chart 2: Data Center PCIe Technology TAM

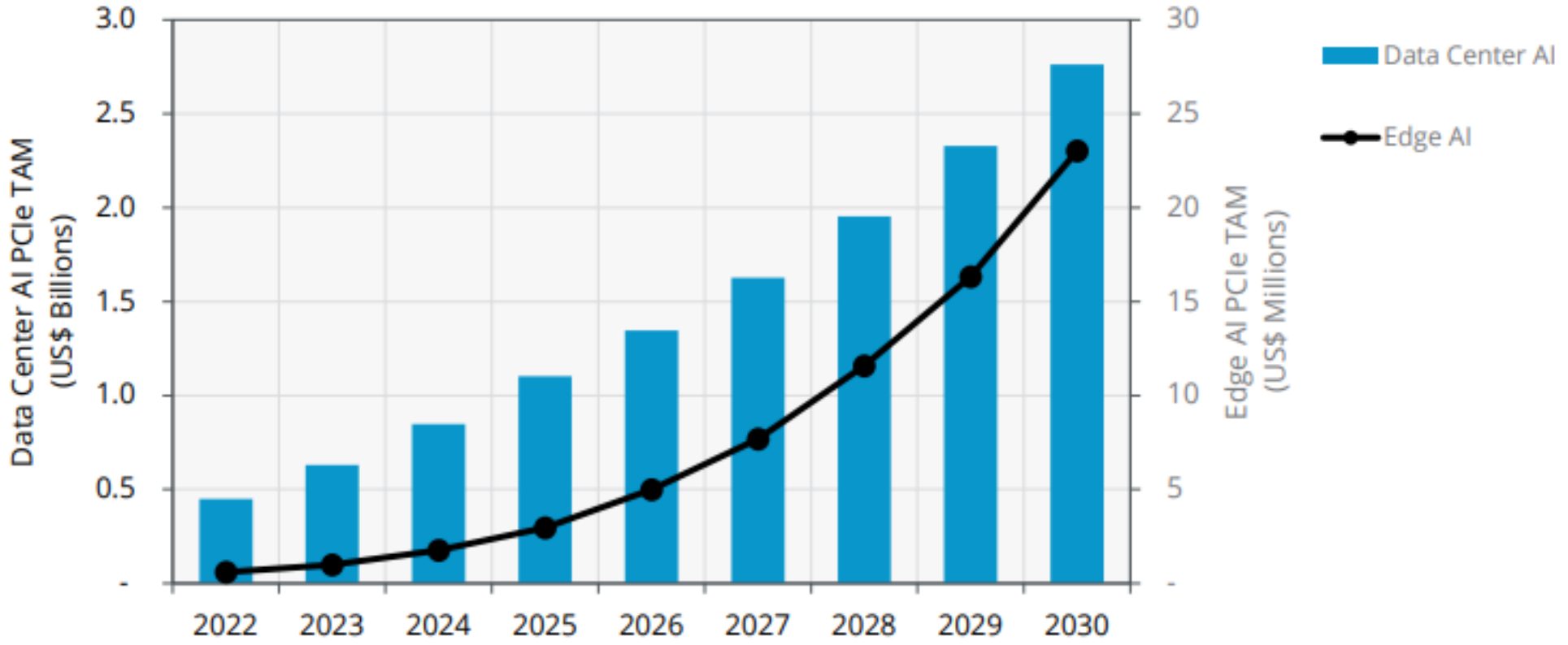
(Source: ABI Research)



Artificial Intelligence

Chart 5: Artificial Intelligence PCIe Technology TAM

(Source: ABI Research)

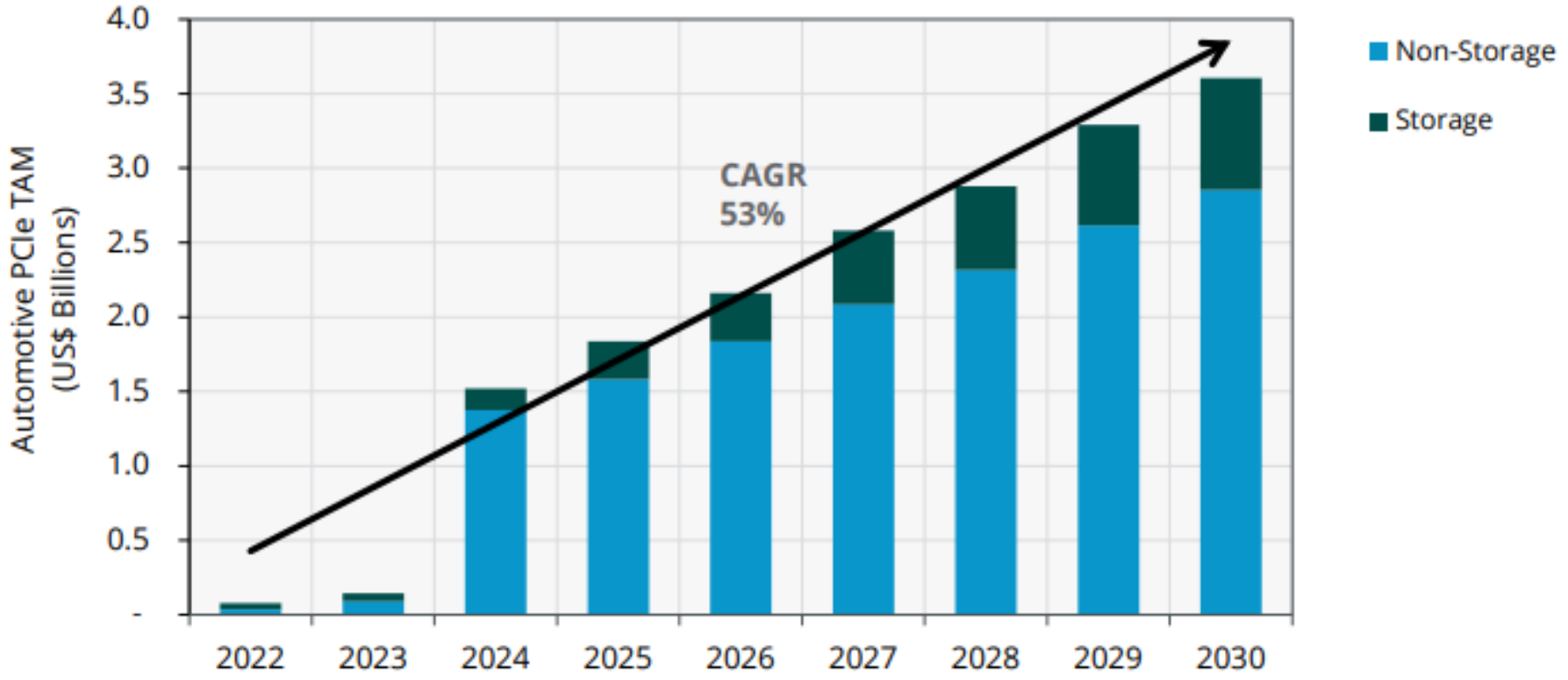


(N.B. AI PCIe technology TAM forecasts are subsets of data center and edge.)

Automotive

Chart 6: Automotive PCIe Technology TAM

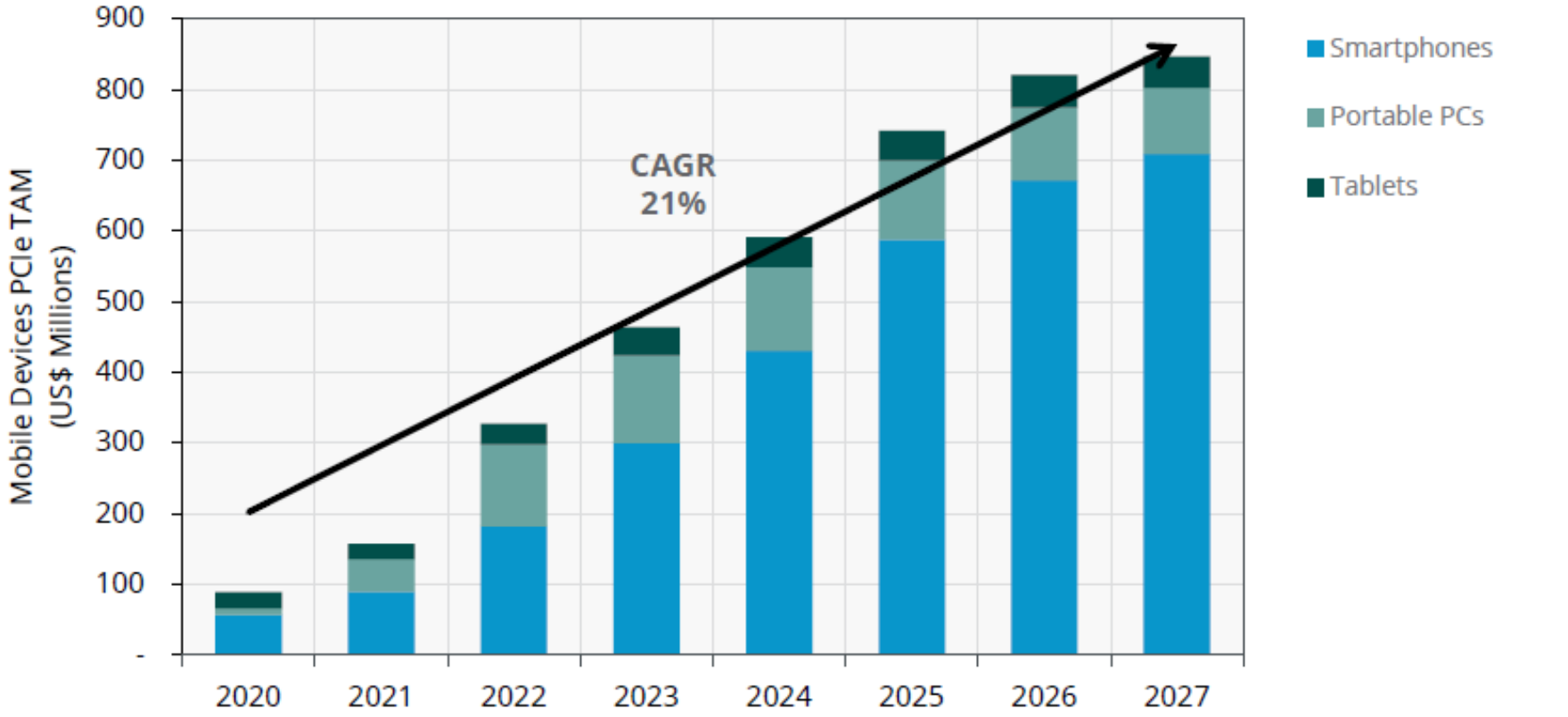
(Source: ABI Research)



Mobile Devices and Wearables

Chart 7: Mobile Devices and Wearables PCIe Technology TAM

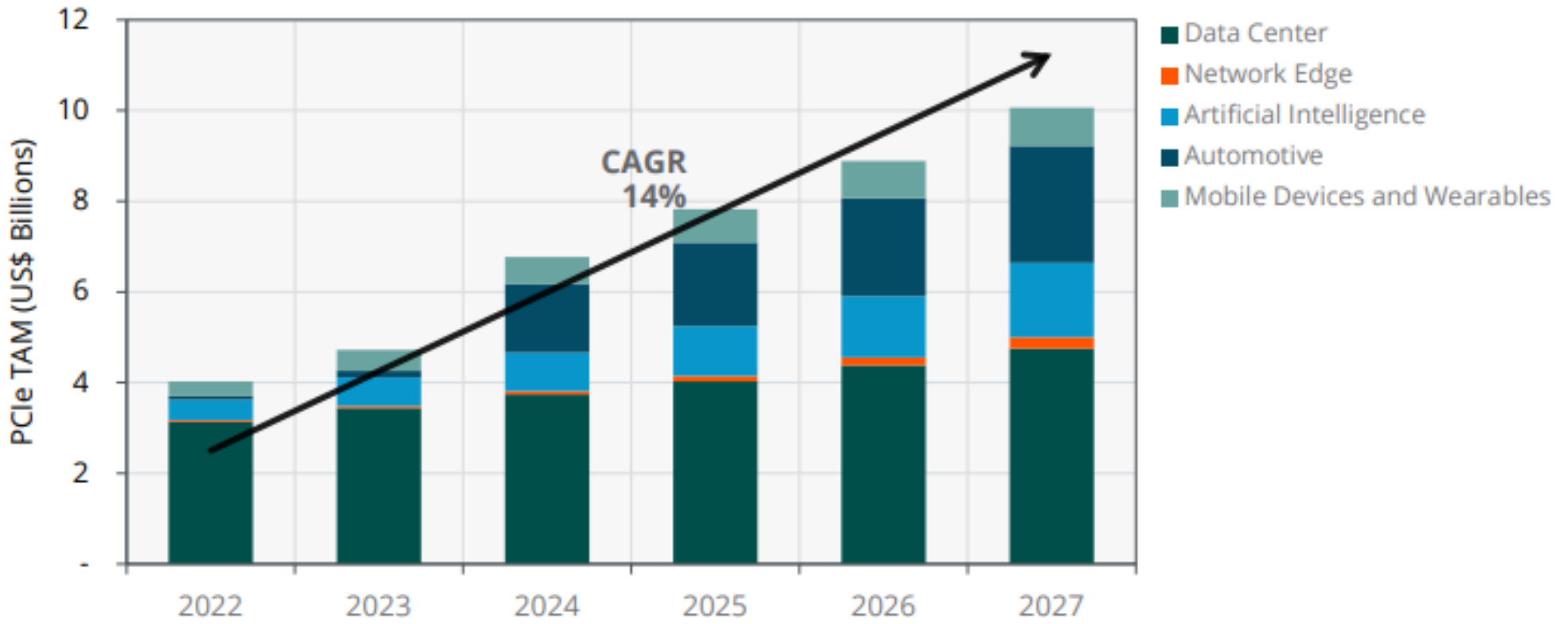
(Source: ABI Research)



Consolidated TAM by Vertical

Chart 8: PCIe Technology TAM Split by Market Vertical

(Source: ABI Research)



(N.B. AI PCIe technology TAM subset has been extrapolated from data center TAM and network edge TAM to avoid double counting.)