PCI-SIG® DevCon 2018 Update

Al Yanes

President and Board Chair

PCI-SIG® Snapshot

Organization that **defines the PCI Express® (PCIe®) I/O bus specifications and related form factors.**

750+ member companies located worldwide

Creating specifications and mechanisms to **support compliance** and **interoperability.**

- **Australia**
- **Austria**
- **Belgium**
- **Brazil**
- **Bulgaria**
- **Canada**
- **China**
- **Czech Republic**
- **Denmark**
- **Finland**
- **France**
- **Germany**
- **Hong Kong**
- **Hungary**
- **India**
- **Ireland**
- **Israel**
- **Italy**
- **Japan**
- **Malaysia**
- **Norway**
- **Russia**
- **Singapore**
- **Slovak Republic**
- **South Korea**
- **Sri Lanka**
- **Sweden**
- **Switzerland**
- **Taiwan**
- **The Netherlands**
- **Turkey**
- **United Kingdom**
- **United States**

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AMD
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Qualcomm
SYNOPSYS® Silicon to Software™

PCI-SIG DevCon Key Updates

- PCIe Markets and Drivers
- PCIe 4.0 Adoption Progress
- PCIe 5.0 Specification Update

Market Segments Addressed by PCIe

Enterprise Servers

Redundancy/Failover

- PCIe switches offer the right level of redundancy & failover in enterprise data centers

Ubiquity

- Interconnect of choice for the data center in enterprise processors and storage subsystems

Power Savings

- Dynamic software and hardware shut downs when no lane traffic is present

Cloud

Scalable Architecture

- Accommodates specific application needs via flexible lane and frequency offerings

Increased Performance

- Low latency between applications running in the servers and subsystems

Reduced TCO

- Eliminates idle power consumption, lowering overhead costs

Storage

Faster Data Transfer

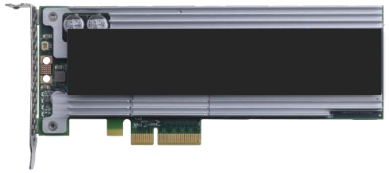
- PCIe 4.0 provides high performance 16GT/s data transfer

Better User Experience

- Applications using PCI technology keeps data closer to the CPU

Ubiquity

- Undisputed interconnect of choice for storage applications



PC/Mobile/IoT

Faster Performance

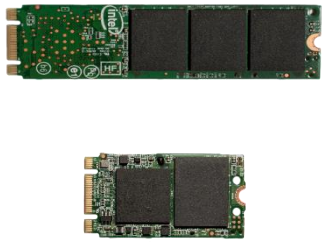
- 16GT/s data rates with PCIe 4.0
- Flexible lane width & speed selection

Power Efficiency

- L1 sub-states lowers power in idle mode (near 0 link idle power)
- High speed data transfer bursts with minimum idle power

Form Factors for PCI Express

M.2

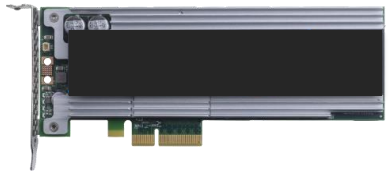


42, 80, and 110mm lengths, smallest footprint of PCIe connector form factors, use for boot, for max storage density, for PXI/AXIe ecosystem

U.2

2.5in makes up the majority of SSDs sold today because of ease of deployment, hotplug, serviceability, and small form factor Single-Port x4 or Dual-Port x2

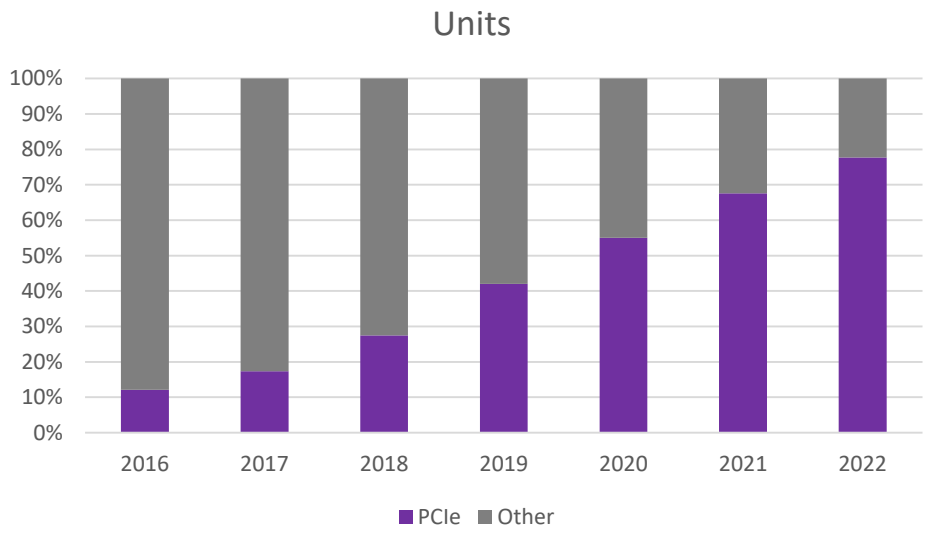
CEM Add-in-card

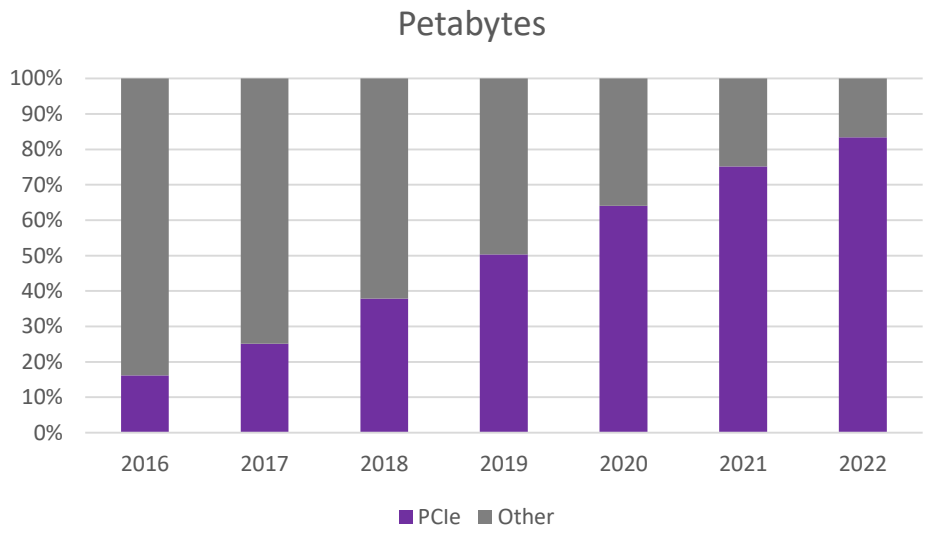


Add-in-card (AIC) has maximum system compatibility with existing servers and most reliable compliance program. Higher power envelope, and options for height and length

NVM Express™ Driving PCIe SSDs in the Data Center

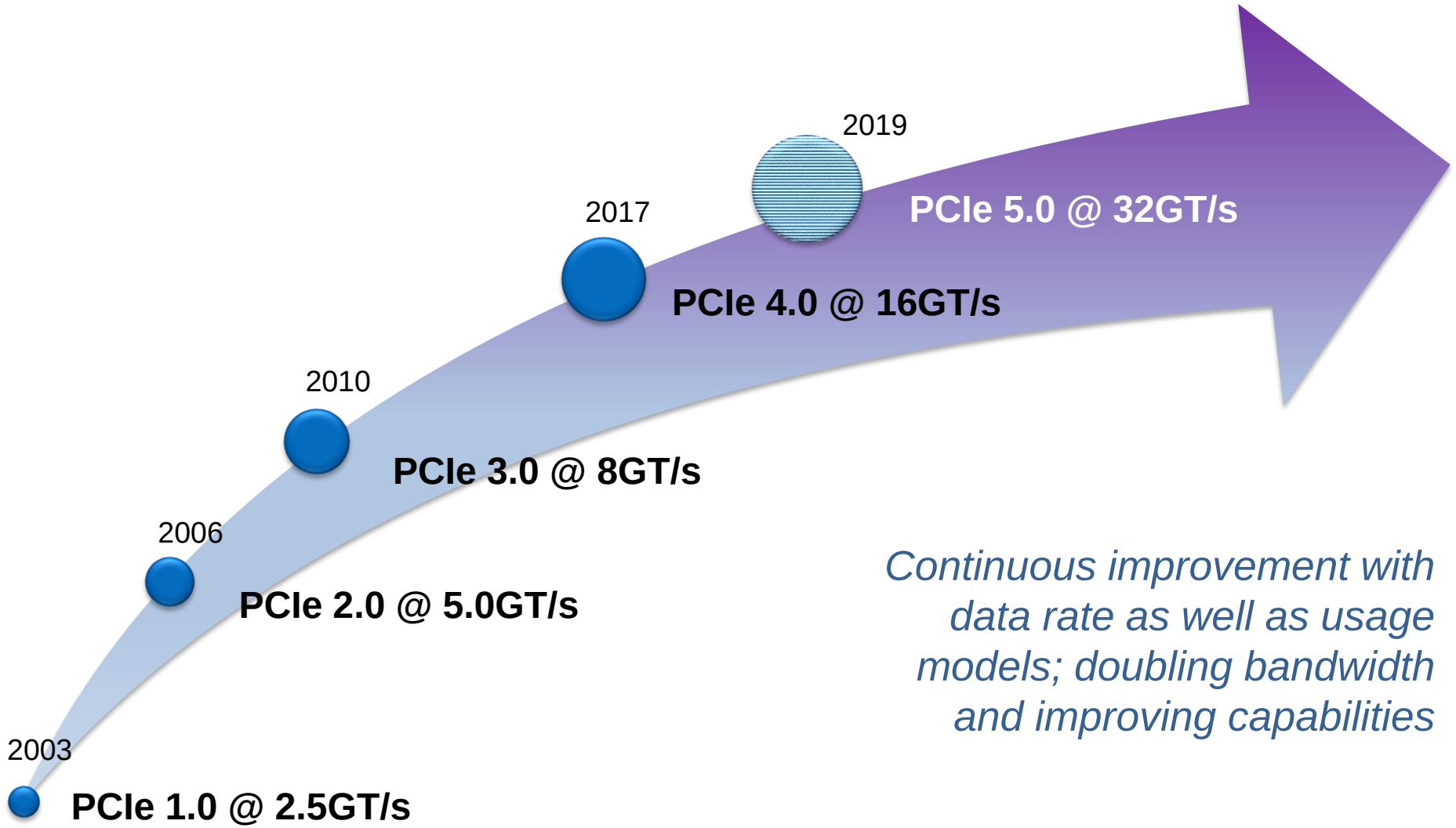
- Data explosion is driving SSD adoption
  - SSD market CAGR of 14.8% during 2016-2021 *Source*: IDC
  - PCIe SSD market to surpass a CAGR of 33% during 2016-2020 *Source*: Technavio
- PCIe adoption is accelerating





Source: SSD Insights Q1/18, Forward Insights

PCIe Roadmap: Specification Completion



Continuous improvement with data rate as well as usage models; doubling bandwidth and improving capabilities

PCI Express 4.0 Specification

PCI-SIG continues its solid reputation of delivering **low cost, high-performance, low-power specifications** for **multiple applications** and **markets.**

- **PCI Express 4.0 Specification – (16GT/S)**
  - Finalized and published October 2017
  - Includes new performance enhancements
  - Maintains position as the interconnect of choice for the expansive storage market and the backbone for the fast growing cloud ecosystem

PCI Express 5.0 Specification

- **PCI Express 5.0 Specification 32GT/S :**
  - PCIe 5.0 Revision 0.7 Specification published to membership in May 2018
  - Sets the standard for speed; backward compatible with prior generations of PCIe technology
  - Enables high-performance applications such as AI, machine learning, gaming, visual computing, storage, and high-end networking solutions (i.e. 400Gb Ethernet)
  - Delivers higher signaling rates that enable narrower links to be used, supporting multiple applications in a variety of form factors
  - Continues to meet requirements for low latency and power efficiency using L1 Sub-states to constrain power consumption during transmission idle periods

PCI Express 5.0 Roadmap

- Changes limited primarily to speed upgrade
  - Protocol already supports higher speed via extended tags and credits
  - Existing PHYs in the industry already run at 28GT/s / 56GT/s
  - Minimal electrical changes
  - Focus on connector studies
  - CEM connector targeted to be backwards compatible for add-in cards
- Specification process enhanced to accelerate development

PCIe 5.0 specification targeted for publication in Q1 2019

	RAW BIT RATE	LINK BW	BW/ LANE/WAY	TOTAL BW X16
PCIe 1.x	2.5GT/s	2Gb/s	250MB/s	8GB/s
PCIe 2.x	5.0GT/s	4Gb/s	500MB/s	16GB/s
PCIe 3.x	8.0GT/s	8Gb/s	~1GB/s	~32GB/s
PCIe 4.0	16GT/s	16Gb/s	~2GB/s	~64GB/s
PCIe 5.0	32GT/s	32Gb/s	~4GB/s	~128GB/s

Summary

- PCIe 4.0 adoption is accelerating, driven by servers, cloud, storage and PC/mobile/IoT
- PCIe 5.0 Revision 0.7 specification has been released to the members and the final Revision 1.0 specification is on track for completion in Q1 2019
- PCI-SIG continues to maintain its leadership position in delivering high-performance, low power I/O

2018 PCI-SIG® DevCon Sponsor Companies

Company Presenters

Platinum	PLDA	**Booth 4** – Stephane Hauradou, Chief Technology Officer
	SYNOPSYS® Silicon to Software™	**Booth 2** – Gary Ruggles, Product Marketing Manager, SG, Solutions Group
	TELEDYNE LECROY Everywhereyoulook™	**Booth 1** – John Wiedemeier, Sr. Product Marketing Manager
Gold	Anritsu	**Booth 9** – Hiroshi Goto, Business Development Manager
	Tektronix®	**Booth 10** – Jim Dunford, Sr. Product Manager
Exhibitor	DIODES INCORPORATED	**Booth 8** – Kay Annamalai, Senior Marketing Director

PLDA

Platinum Sponsor

- Just announced **XpressRICH5 PCIe® 5.0 Controller IP**
  - Supports PCIe 5.0 rev. 0.7 at 32 GT/s with 512-bit architecture
  - Configurable PIPE interface 8- to 64-bit
  - Endpoint, Root Port, Switch Port and Dual-Mode configurations
  - Target ASIC/SoC and FPGA interchangeably and seamlessly with same RTL code
  - Enterprise features including SR-IOV, advanced Low Power modes, RAS

- Showcasing **PCIe 4.0 multi-port Switch IP and Demo Platform**
  - Transparent design
  - PCIe 3.0 upstream, up to 32 PCIe 4.0 downstream ports
  - Demoed with 2 PCIe 4.0 endpoint devices and software applications running concurrently
  - DMA transfers include endpoints<-> host and endpoint<->endpoint via peer-to-peer comm.

Synopsys

Drive the Next Generation of Designs with DesignWare IP for PCI Express® Architecture

Industry Leadership

- Active contributor in PCI-SIG® for more than 20 years, helping to define PCIe® specification and drive adoption
- Complete solution: controllers, PHYs, verification IP, IP Prototyping Kits, IP Subsystems
- Multi-Port Switch IP including Embedded Endpoint
- Silicon-proven ASIL B Ready ISO 26262 certified IP

- Low-risk, silicon-proven solution in more than 1600 designs and billions of devices
- In over 100 designs for PCI Express 4.0 technology
- PCIe 5.0 specification delivered to early adopters
- Most interoperability testing & PCI-SIG certifications

Customers Achieving Silicon Success with DesignWare® IP for PCI Express Specification

AMD, STARBLAZE, KYOCERA Document Solutions, SOLARFLARE, GUC, Open-Silicon, ...

Visit our booth to see demos

1. PCIe 5.0 architecture at 32GT/s
2. Advanced Debug, Error Injection, and Statistics for PCIe 4.0
3. PHY IP for 16GT/s and Beyond
4. Verification Closure with PCIe® 5.0 architecture IP/VIP and Test Suites

SYNOPSYS®

Teledyne LeCroy

- Teledyne LeCroy Summit M5x Protocol Analyzer and Jammer
  - PCIe® 4.0 specification support
  - Speeds up to 16 GT/s
  - Link widths of x1, x2, x4, x8 and x16
  - Jammer for PCIe 4.0 technology up to x16 link widths
  - PCIe 5.0 technology capable platform
- MultiPort on all PCIe 4.0 technology protocol analyzer platforms
  - Bifurcated connector probing using one analyzer
  - Independent devices probing using one analyzer
- MidBus and MultiLead probing capability

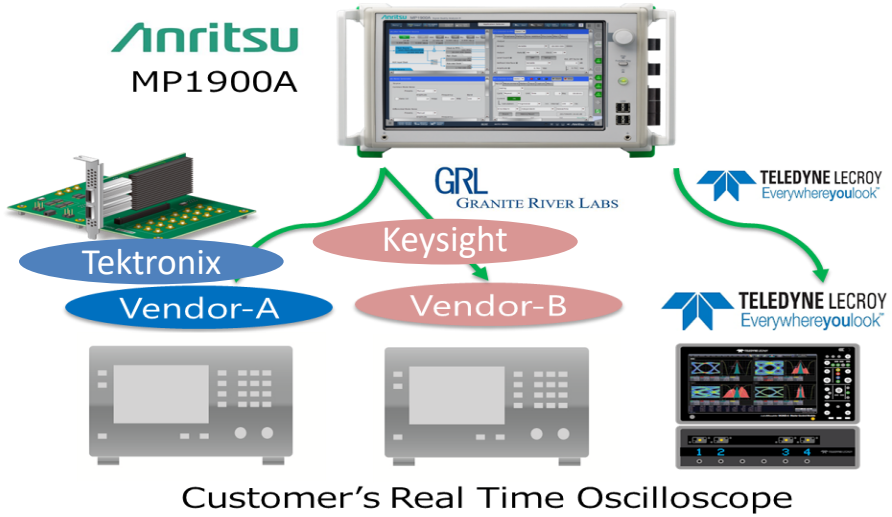
Anritsu

PCIe® Specification Rx Compliance Test

- Combination of best performance BERT MP1900A and your preference oscilloscope -

Shortening your test time and reducing your investment cost

- Supports combination with LeCroy/Tektronix/Keysight Real Time Oscilloscope
- Automated Rx CEM and Base tests : Calibration, Link EQ and Automated Tx test
- Protocol Aware : Link training/Equalization and LTSSM analysis
- Excellent expandable 32G multi-channel BERT for PCIe 1.0 architecture to PCIe 5.0 architecture



Customer's Real Time Oscilloscope

Best performance BERT

Fully automated SW and Analysis

Your preference Oscilloscope

For more information, please go to Anritsu WEB site.
https://www.anritsu.com/en-US/test-measurement/solutions/hssd/index?prod-page=mp1900a

Tektronix

Integrated PCIe 1.0 – 5.0 Receiver Test Solution

FROM COMPLEXITY TO CONFIDENCE

- **Simplified testing**
  - Full-rate output and built-in calibrated impairments up to **32Gb/s**
  - Reference clock multiplication and interference generation
  - Protocol Awareness with pattern sequencer
- **One instrument for PCIe 3.0 – 5.0 Rx testing needs**
  - Automated Compliance Solutions
    - PCIe 3.0 and PCIe 4.0
  - Single vendor solution with automated calibration wizard
- **Reduce debug uncertainty with sophisticated error analysis tools**
  - Pattern Sensitivity
  - Error Free Interval Tool
  - Forward error correction emulation

Tektronix®

Diodes

PCI Express® Solution

- Broad Portfolio of PCI Express (PCIe®) products in the industry including timing, switching, muxing and signal conditioning to support up to 16Gbps.
- Timing ICs (PCIe 2.0, PCIe 3.0 and PCIe 4.0 specifications) minimize clock jitter that degrades signal integrity at the source
- ReDrivers / Repeaters (PCIe 2.0, PCIe 3.0 and PCIe 4.0 specifications) compensate for known channel losses at the transmitter and restore signal integrity at the receiver
- Signal Switches / Multiplexers (PCIe 2.0, PCIe 3.0 and PCIe 4.0 specifications) provide the most efficient and clear signal routing
- Packet Switches (PCIe 2.0 specification) efficiently aggregate multiple I/O devices without compromising signal integrity
- Bridges (PCIe specification to UART/USB/PCI/PCI-X) enable reliable, turn-key connectivity between PCIe technology hosts and legacy peripherals

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DevCon Schedule

Lunch and Exhibit

11:30 a.m. – 1:00 p.m.

Conference Sessions

1:00 p.m. – 3:00 p.m.

Afternoon Break and Exhibit

3:00 p.m. – 3:30 p.m.

Conference Sessions

3:30 p.m. – 4:30 p.m.

PCI-SIG Evening Reception

5:30 p.m. – 7:00 p.m.

Conference Sessions

The following sessions are open for press attendance:

Tuesday, June 5

Track 2: PCI-SIG Architecture
- 1:00-2:00 p.m. – PCI Express Basics
- 3:30-4:30 p.m. – M.2 Updates

Track 3: Member Implementation
- 1:00-2:00 p.m. – Latency in PCIe Expansion Systems
- 2:00-3:00 p.m. – Implementing Lane Margining in a Heterogeneous System

Track 4: Member Implementation
- 1:00-2:00 p.m. – Be Prepared for PHY and PCIe Controller Integration
- 2:00-3:00 p.m. – Trials and Tribulations of Early PCIe 4.0 Adoption

Note: Wednesday, June 6 is closed to press