PCI-SIG® Snapshot

Organization that defines the PCI Express I/O bus specifications and related form factors.

- 730+ member companies located worldwide

Creating specifications and mechanisms to support compliance and interoperability.

BOARD OF DIRECTORS 2017-2018

- Australia
- Austria
- Belgium
- Brazil
- Bulgaria
- Canada
- China
- Czech Republic
- Denmark
- Finland
- France
- Germany
- Hong Kong
- Hungary
- India
- Ireland
- Israel
- Italy
- Japan
- Malaysia
- Norway
- Russia
- Singapore
- Slovak Republic
- South Korea
- Sri Lanka
- Sweden
- Switzerland
- Taiwan
- The Netherlands
- Turkey
- United Kingdom
- United States
PCI Express 4.0

PCI-SIG continues its solid reputation of delivering low cost, high-performance, low-power specifications for multiple applications and markets.

- **PCI Express 4.0 Specification – (16GT/s)**
  - Feature complete Revision 0.9 released for final IP review
  - Includes new performance enhancements
  - Maintains position as the interconnect of choice for the expansive storage market and the backbone for the fast growing cloud ecosystem
PCI Express 4.0

- **PCIe 4.0 Key Functional Enhancements**
  - Lane Margining at the Receiver
    - Allows the system to determine how close to “the edge” each lane is operating under real conditions
  - Expanded Tag and Credits
    - Allows both tags and credits to expand to service devices well into the foreseeable future

- **PCIe 4.0 Adoption**
  - Numerous vendors confirmed with 16GT/s PHYs in silicon
  - Major IP vendors offering 16GT/s controllers
  - Dozen 16GT/s solutions at a recent PCI-SIG Compliance Workshop
  - Several DevCon exhibitors with 16GT/s demos
Ethernet Evolution

Market Adoption of Ethernet Speeds

Ethernet's "success" in providing cost-effective and reliable solutions, soon expanded into new markets.

Service Provider applications started deploying Ethernet due to customer requests.

Service Provider applications started driving Ethernet's new higher speed rates.

Controller and Adapter Market Port Forecast

Source: Dell'Oro Research Q4'15

<table>
<thead>
<tr>
<th>Year</th>
<th>100 Gbps</th>
<th>50 Gbps</th>
<th>40 Gbps</th>
<th>25 Gbps</th>
<th>10 Gbps</th>
<th>1 Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>55</td>
<td>14</td>
<td>12</td>
<td>4</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2012</td>
<td>50</td>
<td>15</td>
<td>10</td>
<td>5</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2013</td>
<td>45</td>
<td>20</td>
<td>8</td>
<td>10</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2014</td>
<td>40</td>
<td>25</td>
<td>7</td>
<td>10</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2015</td>
<td>35</td>
<td>30</td>
<td>6</td>
<td>10</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>2016</td>
<td>30</td>
<td>35</td>
<td>5</td>
<td>10</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2017</td>
<td>25</td>
<td>40</td>
<td>4</td>
<td>10</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>2018</td>
<td>20</td>
<td>45</td>
<td>3</td>
<td>10</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>2019</td>
<td>15</td>
<td>50</td>
<td>2</td>
<td>10</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>2020</td>
<td>10</td>
<td>55</td>
<td>1</td>
<td>10</td>
<td>0</td>
<td>7</td>
</tr>
</tbody>
</table>

Total Ports

- 85 in 2011
- 114 in 2012
- 148 in 2013
- 191 in 2014
- 278 in 2015
- 442 in 2016
- 750 in 2017
- 906.05 in 2018
- 1,800 in 2019
- 3,000 in 2020

YER Ratio

- 1.7 in 2011
- 2.1 in 2012
- 3.0 in 2013
- 1.7 in 2014
- 1.5 in 2015
- 1.0 in 2016
- 0.5 in 2017
- 0.3 in 2018
- 0.2 in 2019
- 0.1 in 2020

3 Year Ratio

- 1.7 in 2011
- 2.1 in 2012
- 3.0 in 2013
- 1.7 in 2014
- 1.5 in 2015
- 1.0 in 2016
- 0.5 in 2017
- 0.3 in 2018
- 0.2 in 2019
- 0.1 in 2020
PCI Express – Future

- PCI Express 5.0 Specification with 32GT/s Bandwidth
  - Revision 0.3 has already been delivered to PCI-SIG members
  - Ideal for:
    - Applications such as artificial intelligence, machine learning, gaming, visual computing, storage and networking
    - High-end networking solutions (i.e. 400Gb Ethernet and dual 200Gb/s InfiniBand solutions)
    - Accelerator and GPU attachments for high-bandwidth solutions
    - Constricted form factor applications that cannot increase width and need higher frequency to achieve performance
PCIe 5.0 Delivering 32GT/s

- Supports 400Gb Ethernet Solutions
  - 400Gb = 50GB
  - 50GB in both directions

- Full Duplex
  - 128/130 bit encoding with 1.5% overhead
  - x16 ~64GB/s sufficient to support 400Gb Ethernet solutions (64GB > 50 GB)
  - Total Full Duplex = ~128GB

- CEM connector targeted to be backwards compatible for add-in cards
- Targeted Release in 2019

---

<table>
<thead>
<tr>
<th></th>
<th>RAW BIT RATE</th>
<th>LINK BW</th>
<th>BW/ LANE/WAY</th>
<th>TOTAL BW X16</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe 1.x</td>
<td>2.5GT/s</td>
<td>2Gb/s</td>
<td>250MB/s</td>
<td>8GB/s</td>
</tr>
<tr>
<td>PCIe 2.x</td>
<td>5.0GT/s</td>
<td>4Gb/s</td>
<td>500MB/s</td>
<td>16GB/s</td>
</tr>
<tr>
<td>PCIe 3.x</td>
<td>8.0GT/s</td>
<td>8Gb/s</td>
<td>~1GB/s</td>
<td>~32GB/s</td>
</tr>
<tr>
<td>PCIe 4.0</td>
<td>16GT/s</td>
<td>16Gb/s</td>
<td>~2GB/s</td>
<td>~64GB/s</td>
</tr>
<tr>
<td>PCIe 5.0</td>
<td>32GT/s</td>
<td>32Gb/s</td>
<td>~4GB/s</td>
<td>~128GB/s</td>
</tr>
</tbody>
</table>
## PCIe Bandwidth & Frequency

<table>
<thead>
<tr>
<th>Year</th>
<th>Bandwidth</th>
<th>Frequency/Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1992</td>
<td>133MB/s (32 bit simplex)</td>
<td>33 Mhz (PCI)</td>
</tr>
<tr>
<td>1993</td>
<td>533MB/s (64 bit simplex)</td>
<td>66 Mhz (PCI 2.0)</td>
</tr>
<tr>
<td>1999</td>
<td>1.06GB/s (64 bit simplex)</td>
<td>133 Mhz (PCI-X)</td>
</tr>
<tr>
<td>2002</td>
<td>2.13GB/s (64 bit simplex)</td>
<td>266 Mhz (PCI-X 2.0)</td>
</tr>
<tr>
<td>2002</td>
<td>8GB/s (x16 duplex)</td>
<td>2.5 GHz (PCIe 1.x)</td>
</tr>
<tr>
<td>2006</td>
<td>16GB/s (x16 duplex)</td>
<td>5.0 GHz (PCIe 2.x)</td>
</tr>
<tr>
<td>2010</td>
<td>32GB/s (x16 duplex)</td>
<td>8.0 GHz (PCIe 3.x)</td>
</tr>
<tr>
<td>2017</td>
<td>64GB/s (x16 duplex)</td>
<td>16.0 GHz (PCIe 4.0)</td>
</tr>
<tr>
<td>2019</td>
<td>128GB/s (x16 duplex)</td>
<td>32.0 GHz (PCIe 5.0)</td>
</tr>
</tbody>
</table>
PCIe® Roadmap

Continuous improvement with data rate as well as usage models; doubling bandwidth and improving capabilities.
PCI-SIG History

I/O BANDWIDTH DOUBLES
Every 3 Years

PCI-SIG BANDWIDTH 1992-2019

- Actual Bandwidth (GB/S)
- I/O Bandwidth Doubles Every Three Years
2017 PCI-SIG® DevCon Sponsor & Exhibiting Companies
## Company Presenters

<table>
<thead>
<tr>
<th>Platinum</th>
<th>Booth 3 – Sachin Dhingra, Senior Product Marketing Manager</th>
</tr>
</thead>
<tbody>
<tr>
<td>Platinum</td>
<td>Booth 2 – Scott Knowlton, Senior Product Marketing Manager</td>
</tr>
<tr>
<td>Platinum</td>
<td>Booth 4 – John Wiedemeier, Product Marketing Manager</td>
</tr>
<tr>
<td>Gold</td>
<td>Booth 8 – Rick Eads, Principal PCI Express Solutions Planner</td>
</tr>
<tr>
<td>Gold</td>
<td>Booth 9 – Jason Polychronopoulos, Mgr. Verification IP Solutions</td>
</tr>
<tr>
<td>Gold</td>
<td>Booth 12 – Stephane Hauradou, Co-founder</td>
</tr>
<tr>
<td>Gold</td>
<td>Booth 5 – Rob Venzina, Senior Application Engineer</td>
</tr>
<tr>
<td>Exhibitor</td>
<td>Booth 1 – Kay Annamalai, Senior Marketing Director</td>
</tr>
<tr>
<td>Exhibitor</td>
<td>Booth 7 – Gursimranjit Singh, Senior Systems Engineer</td>
</tr>
</tbody>
</table>
**Cadence IP Solution for PCI Express® 4.0 Architecture**

- **Complete, integrated, pre-verified Cadence® IP solution**
  - High-performance, low-latency controller
  - Multi-link, multi-protocol PHY
  - Verification IP with extensive test suite and debug utilities

- **Application-optimized solutions**
  - Enterprise
    - Multi-packet design allows >95% link utilization
    - Flexible PHY configurations to maximize utilization of bandwidth
  - Mobile
    - Lowest active power with L0 state power
    - Lowest area and flexible placement for smallest overall SoC
  - Automotive
    - First PCIe® 4.0 PHY audited by SGS-TÜV and deemed ASIL-B ready
    - Solution supports comprehensive automotive safety features

- **Technical presentation**
  - *Challenges and Techniques for Implementing Lane Margining* – Gopi K, Architect
Finish First with DesignWare IP Solutions for PCIe® Technology
Validated in Over 1500 Designs & Shipping Billions of Units

- **PCle® 4.0 Architecture Ready**
  - PHYs, controllers, verification IP & IP prototyping kits conforming to the 0.7 revision of the PCIe 4.0 specification
  - Validated PCIe 4.0 testing and interoperability with ecosystem partners: Mellanox, Teledyne LeCroy and more
    - Demos: Full system PCIe 4.0 interoperability @ 16GT/s with Mellanox; DesignWare® PHY IP; verification IP

- **Automotive Ready**
  - Certified PHY and controller IP solutions meet automotive functional safety, reliability and temperature requirements
  - Demo: Reliability, debug, error injection features
Teledyne LeCroy

PCIe® 4.0 Protocol Test Equipment

- Summit T416 Protocol Analyzer
- Summit Z416 Protocol Exerciser

makes Protocol Analysis Easy

Link Expert

- PCIe technology with SMBus Support
  - 90° Rack Mount
  - Standard Interposer
  - PCIe External Cable 3.0 Interposer
  - M.2 Interposer
  - U.2(SFF-8639) 5"

Booth #4
PCI Express® 4.0 Technology – Keysight Total Solution

**Physical layer – interconnect design**
- ADS design software
- 86100D DCA-X/TDR
- E5071C ENA option TDR

**Physical layer-transmitter test**
- V-Series, Z-Series Real-Time Oscilloscopes
- N5393F PCI Express 4.0 TX Electrical compliance software
- 86100CU-400 PLL and Jitter Spectrum Measurement SW

**Physical layer-receiver test**
- M8020A J-BERT High Performance, Protocol Aware BERT
- N5990A automated compliance and device characterization test software

**Verify PCIe 4.0 Compliant Channels**
- Verify Return Loss Compliance

**Automated RX Test software**
- Accurate, Efficient
- Comprehensive RX Testing
Mentor Graphics

- **Industry leading support for PCIe® Technology & NVMe®**
  - PCIe 4.0 specification, NVMe, AHCI, SRIOV, MRIOV, etc
- **Part of a complete Verification IP solution**
  - Protocols: AMBA®, Display, Ethernet, MIPI®, PCIe architecture, USB, etc.
  - Memory models: DDR, HBM, WideIO, SD, ONFI, etc
- **Architected for rapid productivity**
  - Standards based SV UVM support
  - New configuration GUI
  - New sequence library
- **Complete protocol assurance**
  - Comprehensive test suite, checking & coverage
- **High performance verification**
  - Optimized simulation models
  - Synthesizable transactors for testbench acceleration
  - Virtual models for Acceleration and ICE

Booth #9
PLDA launches PCIe Inspector, a Plug & Play PCIe 4.0 16GT/s host platform with built-in PCIe traffic monitoring, ideal for:

- Interoperability validation of PCIe endpoints (up to PCIe 4.0 architecture)
- Real-time benchmarking and performance monitoring
- Applications performance optimization
- Early PCIe 4.0 software development
- Performance validation of PCIe 4.0 PoCs
Viavi Solutions Storage Network Test Solutions

• Gold Sponsor

• Viavi provides storage network testing solutions for PCIe® technology, NVMe, Fibre Channel and ethernet

• Viavi announces Xgig 4K16 PCI Express 4.0 Protocol Analyzer/Jammer

• Single platform offers simultaneous protocol analysis and error injection for PCIe 4.0 technology traffic at all layers of the stack
PCI Express® Technology Solution

- Broad portfolio of PCI Express (PCIe) products in the industry including timing, switching, muxing and signal conditioning to support up to 16Gbps.
- **Timing ICs** (PCIe 2.0 and PCIe 3.0-based architectures) minimize clock jitter that can degrade signal integrity at the source.
- **ReDrivers / Repeaters** (PCIe 2.0 and PCIe 3.0-based architectures) compensate for known channel losses at the transmitter and restore signal integrity at the receiver.
- **Signal Switches / Multiplexers** (PCIe 2.0, PCIe 3.0 and PCIe 4.0-based solutions) provide efficient and clear signal routing.
- **Packet Switches** (PCIe 2.0-based architecture) efficiently aggregate multiple I/O devices without compromising signal integrity.
- **Bridges** (PCIe to UART/USB/PCI/PCI-X) enable reliable, turn-key connectivity between PCIe hosts and legacy peripherals.
**ExpEther – Expansion of PCIe® Switch over Ethernet**

ExpEther Engine is seen as PCIe Switch from CPU

- Ethernet region is invisible from the CPU

ExpEther is fully compatible with PCIe Specification

---

Click to edit Master title style

Copyright © 2017 PCI-SIG® - All Rights Reserved

DEVCON 2017 UPDATE

Booth #7
PCI-SIG® DevCon Schedule

Lunch and Exhibit
11:30 a.m. – 1:00 p.m.

Conference Sessions
1:00 p.m. – 3:00 p.m.

Afternoon Break and Exhibit
3:00 p.m. – 3:30 p.m.

Conference Sessions
3:30 p.m. – 4:30 p.m.

PCI-SIG 25th Anniversary Party
5:30 p.m. – 8:00 p.m.
The following sessions are open for press attendance:

Wednesday, June 7

**Track 2: PCI-SIG Architecture**
- 1:00-2:00 p.m. – PCI Express Basics
- 3:30-4:30 p.m. – M.2 Updates

**Track 3: Member Implementation**
- 2:00-3:00 p.m. – In-system Debugging of PCIe Devices
- 3:30-4:30 p.m. – Performance Tuning PCIe Systems

*Note: Thursday, June 8 is closed to press*