PCI Express® Specification
Frequently Asked Questions
PCI-SIG®

Q: What is PCI Express® (PCIe®) 4.0? What are the requirements for this evolution of the PCIe architecture?
A: PCIe 4.0 is the next evolution of the ubiquitous and general-purpose PCI Express I/O specification. At 16GT/s bit rate, the interconnect performance bandwidth will be doubled over the PCIe 3.0 specification, while preserving compatibility with software and mechanical interfaces. The key requirement for evolving the PCIe architecture is to continue to provide performance scaling consistent with bandwidth demand from a variety of applications with low cost, low power and minimal perturbations at the platform level. One of the main factors in the wide adoption of the PCIe architecture is its sensitivity to high-volume manufacturing capabilities and materials such as FR4 boards, low-cost connectors and so on.

Q: What is the release status of the PCIe 4.0 specification?
A: The PCIe 4.0 Revision 0.9 specification has been published to members. It is feature complete and going through final IP review.

Q: What is the bit rate for the PCIe 4.0 specification and how does it compare to prior generations of PCIe?
A: The bit rate for the PCIe 4.0 specification will be 16GT/s, while maintaining compatibility with previous generations of PCIe architecture. This bit rate represents the optimum tradeoff between performance, manufacturability, cost, power and compatibility.

Q: Will PCIe 4.0 products be compatible with existing PCIe 1.x, PCIe 2.x and PCIe 3.x products?
A: PCI-SIG is proud of its long heritage of developing compatible architectures and its members have consistently produced compatible and interoperable products. In keeping with this tradition, the PCIe 4.0 architecture is compatible with prior generations of this technology, from software to clocking architecture to mechanical interfaces. That is to say PCIe 1.x, 2.x and 3.x cards will seamlessly plug into PCIe 4.0-capable slots and operate at the highest performance levels possible. Similarly, all PCIe 4.0 cards will plug into PCIe 1.x-, PCIe 2.x- and PCIe 3.x-capable slots and operate at the highest performance levels supported by those configurations.

Q: What are the initial target applications for the PCIe 4.0 architecture?
A: The PCIe 4.0 specification will address the many applications pushing for increased bandwidth at a low cost including server, workstation, desktop PC, notebook PC, tablets, embedded systems, peripheral devices, high-performance computing markets and more. The target implementations are entirely at the discretion of the designer.

Q: Is PCIe 4.0 architecture more expensive to implement than PCIe 3.x?
A: PCI-SIG attempts to define and evolve the PCIe architecture in a manner consistent with low-cost and high-volume manufacturability considerations. While PCI-SIG cannot comment

on design choices and implementation costs, optimized silicon die size and power consumption continue to be important considerations that inform PCIe specification development and architecture evolution.

Q: Will there been a new compliance specification developed for the PCIe 4.0 specification?
A: For each revision of its specification, PCI-SIG develops compliance tests and related collateral consistent with the requirements of the new architecture. All of these compliance requirements are incremental in nature and build on the prior generation of the architecture. PCI-SIG anticipates releasing compliance specifications as they mature along with corresponding tests and measurement criteria. Each revision of the PCIe technology maintains its own criteria for product interoperability and admission into the PCI-SIG Integrators List. For the first time, PCI-SIG offered pre-publication compliance testing to its members leveraging the PCIe 4.0, Revision 0.9 specification.

Q: What is next for PCIe architecture?
A: PCI-SIG has announced 32GT/s as the next progression in speed for the PCIe 5.0 architecture, targeting high-performance applications such as artificial intelligence, machine learning, gaming, visual computing, storage and networking.

Q: When will the PCIe 5.0 specification be available?
A: This next iteration of the specification is slated for completion in 2019; however, development is well underway with Revision 0.3 already available to PCI-SIG member companies. The PCIe 4.0 specification was designed with key functional enhancements that future-proof the PCIe architecture design, thereby accelerating future specification development. This undertaking, along with improved silicon design processes, serves as the foundation for the PCIe 5.0 specification.