PCI-SIG® 2020 Update

Al Yanes, President and Board Chair

Richard Solomon, Vice President and Compliance Chair

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PCI-SIG® Snapshot

- Organization that **defines the PCI Express® (PCIe®) I/O bus specifications and related form factors**
- **830+** member companies located worldwide
  - Highest number of member companies in ten years
- Creating specifications and mechanisms to **support compliance** and **interoperability**

Board of Directors
2020 –2021

AMD
arm
DELL EMC
IBM
intel
KEYSIGHT TECHNOLOGIES
NVIDIA
Qualcomm
SYNOPSYS
Silicon to Software

PCI Express® 4.0 Specification & Status

Adoption is underway

Key Features:

- Delivers 16 GT/s
- Maintains backward compatibility with PCIe 3.x, 2.x, and 1.x specifications

Adoption:

- Numerous vendors with 16GT/s PHYs and controllers in silicon
- Test equipment from multiple vendors available
- Products are readily available in the marketplace

Compliance Program and Integrators List

- **PCI-SIG 5.0 Compliance Program**
  - PCIe 5.0 specification compliance testing is under development
- **PCI-SIG 4.0 Compliance Program**
  - PCI-SIG launched official testing for PCIe 4.0 specification in August 2019
  - 85 products have been added to the Integrators List in markets like Storage, Enterprise and Cloud

- PCI-SIG has held a total of **114** Compliance Workshops
- Compliance Workshops have been held in the **United States** and **Taipei**
- **1,153** total products are on the PCI-SIG Integrators List

PCI Express® 5.0 Specification & Status

Released in May 2019

Key Features:

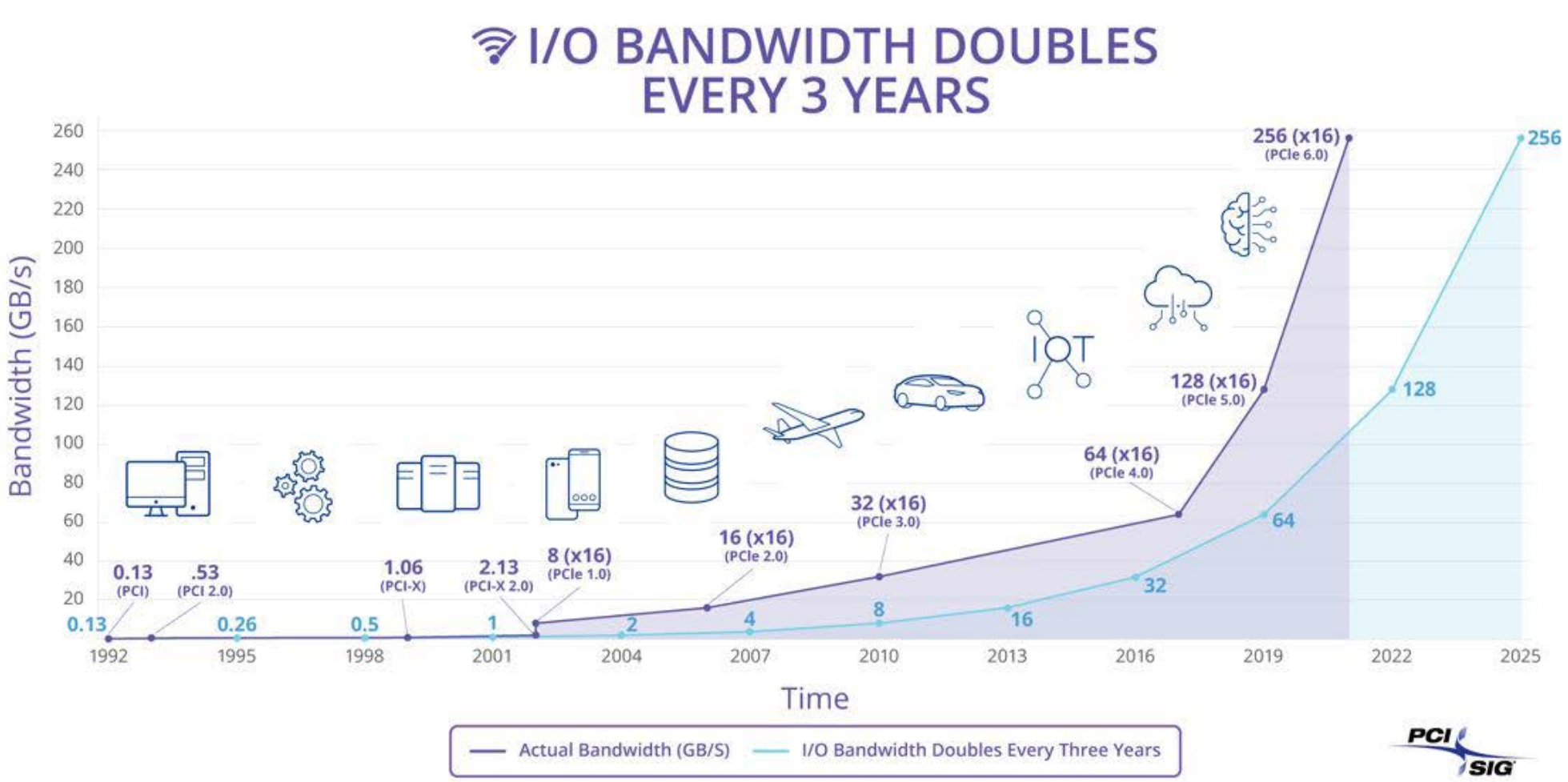
- Doubles bandwidth over PCIe 4.0 specification to deliver 32 GT/s
- Maintains backwards compatibility with PCIe 4.0, 3.x, 2.x and 1.x specifications

Adoption:

- Silicon ecosystem is available for product development
- Test equipment is available
- Several member companies have publicly announced and are showcasing PCIe 5.0 solutions in Storage, Enterprise, AI/ML and Cloud
- Adoption expected to grow in the next 18-24 months due to demand from high performance applications

PCIe® Rev	Total Channel Insertion Loss Budget	Root Package	CEM Connector	Add-in Card (AIC)	Remaining System Base Board Budget
3.0 (8 GT/s)	22 dB	3.5 dB	1.7 dB	6.5 dB	10.3 dB
4.0 (16 GT/s)	28 dB	5.0 dB	1.5 dB	8.0 dB	13.5 dB
5.0 (32 GT/s)	36 dB	9.0 dB	1.5 dB	9.5 dB	16.0 dB

PCI-SIG® Roadmap



PCI Express® 6.0 Specification Details

PCIe 6.0 version 0.5 specification released in Feb. 2020

Key Features:

- Doubles bandwidth to 64 GT/s from 32 GT/s (PCIe 5.0)
- Maintains backward compatibility with all previous generations of PCIe architecture
- Implements PAM4 signaling, allowing it to pack more bits into the same amount of time on a serial channel
- Includes low-latency Forward Error Correction (FEC) with additional mechanisms to improve bandwidth efficiency and improve reliability
  - FEC changes do not significantly affect protocol overhead and latency
- FLIT (flow control unit) based: FEC needs fixed set of bytes
- Targeting high-bandwidth applications like Cloud, AI/ML, edge and more
  - Single PCIe 6.0 x16 can support 800G Ethernet

PCIe Specification	Data Rate(GT/s) (Encoding)	Year
1.0	2.5 (8b/10b)	2003
2.0	5.0 (8b/10b)	2007
3.0	8.0 (128b/130b)	2010
4.0	16.0 (128b/130b)	2017
5.0	32.0 (128b/130b)	2019
6.0	64.0 (128b/130b, PAM4, FLIT)	2021*

Adoption:

- PCIe 6.0 version 0.7 specification targeted for later this year
- *PCIe 6.0 final specification on track for release in 2021

Upcoming PCIe 6.0 Specification Webinar

Visit https://pcisig.com/events/webinars to register

Questions

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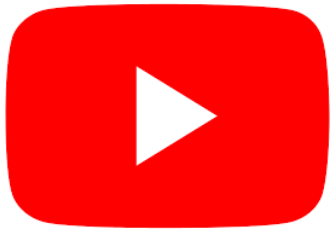

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https://pcisig.com/newsroom/blog