PCI-SIG® 2020 Update

Al Yanes, President and Board Chair
Richard Solomon, Vice President and Compliance Chair

June 3, 2020
PCI-SIG® Snapshot

- Organization that defines the PCI Express® (PCIe®) I/O bus specifications and related form factors
- 830+ member companies located worldwide
  - Highest number of member companies in ten years
- Creating specifications and mechanisms to support compliance and interoperability
PCI Express® 4.0 Specification & Status

Adoption is underway

Key Features:
• Delivers 16 GT/s
• Maintains backward compatibility with PCIe 3.x, 2.x, and 1.x specifications

Adoption:
• Numerous vendors with 16GT/s PHYs and controllers in silicon
• Test equipment from multiple vendors available
• Products are readily available in the marketplace
Compliance Program and Integrators List

• **PCI-SIG 5.0 Compliance Program**
  • PCIe 5.0 specification compliance testing is under development

• **PCI-SIG 4.0 Compliance Program**
  • PCI-SIG launched official testing for PCIe 4.0 specification in August 2019
  • 85 products have been added to the Integrators List in markets like Storage, Enterprise and Cloud

• PCI-SIG has held a total of **114** Compliance Workshops
• Compliance Workshops have been held in the **United States** and **Taipei**
• **1,153** total products are on the PCI-SIG Integrators List
PCI Express® 5.0 Specification & Status

Released in May 2019

Key Features:
- Doubles bandwidth over PCIe 4.0 specification to deliver 32 GT/s
- Maintains backwards compatibility with PCIe 4.0, 3.x, 2.x and 1.x specifications

Adoption:
- Silicon ecosystem is available for product development
- Test equipment is available
- Several member companies have publicly announced and are showcasing PCIe 5.0 solutions in Storage, Enterprise, AI/ML and Cloud
- Adoption expected to grow in the next 18-24 months due to demand from high performance applications

<table>
<thead>
<tr>
<th>PCle® Rev</th>
<th>Total Channel Insertion Loss Budget</th>
<th>Root Package</th>
<th>CEM Connector</th>
<th>Add-in Card (AIC)</th>
<th>Remaining System Base Board Budget</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0 (8 GT/s)</td>
<td>22 dB</td>
<td>3.5 dB</td>
<td>1.7 dB</td>
<td>6.5 dB</td>
<td>10.3 dB</td>
</tr>
<tr>
<td>4.0 (16 GT/s)</td>
<td>28 dB</td>
<td>5.0 dB</td>
<td>1.5 dB</td>
<td>8.0 dB</td>
<td>13.5 dB</td>
</tr>
<tr>
<td>5.0 (32 GT/s)</td>
<td>36 dB</td>
<td>9.0 dB</td>
<td>1.5 dB</td>
<td>9.5 dB</td>
<td>16.0 dB</td>
</tr>
</tbody>
</table>
PCI-SIG® Roadmap

I/O BANDWIDTH DOUBLES EVERY 3 YEARS

Time


Bandwidth (GB/s)

20 40 60 80 100 120 140 160 180 200 220 240 260

0.13 (PCI) 0.26 (PCI 2.0) 1.06 (PCI-X) 2.13 (PCI-X 2.0) 8 (x16) (PCIe 2.0) 16 (x16) (PCIe 3.0) 32 (x16) (PCIe 3.0) 64 (x16) (PCIe 4.0) 128 (x16) (PCIe 5.0) 256 (x16) (PCIe 6.0) 256

Actual Bandwidth (GB/S)  I/O Bandwidth Doubles Every Three Years
PCI Express® 6.0 Specification Details

PCle 6.0 version 0.5 specification released in Feb. 2020

Key Features:
- Doubles bandwidth to 64 GT/s from 32 GT/s (PCIe 5.0)
- Maintains backward compatibility with all previous generations of PCIe architecture
- Implements PAM4 signaling, allowing it to pack more bits into the same amount of time on a serial channel
- Includes low-latency Forward Error Correction (FEC) with additional mechanisms to improve bandwidth efficiency and improve reliability
  - FEC changes do not significantly affect protocol overhead and latency
- FLIT (flow control unit) based: FEC needs fixed set of bytes
- Targeting high-bandwidth applications like Cloud, AI/ML, edge and more
  - Single PCIe 6.0 x16 can support 800G Ethernet

Adoption:
- PCIe 6.0 version 0.7 specification targeted for later this year
- *PCIe 6.0 final specification on track for release in 2021

<table>
<thead>
<tr>
<th>PCIe Specification</th>
<th>Data Rate(GT/s) (Encoding)</th>
<th>Year</th>
</tr>
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<tbody>
<tr>
<td>1.0</td>
<td>2.5 (8b/10b)</td>
<td>2003</td>
</tr>
<tr>
<td>2.0</td>
<td>5.0 (8b/10b)</td>
<td>2007</td>
</tr>
<tr>
<td>3.0</td>
<td>8.0 (128b/130b)</td>
<td>2010</td>
</tr>
<tr>
<td>4.0</td>
<td>16.0 (128b/130b)</td>
<td>2017</td>
</tr>
<tr>
<td>5.0</td>
<td>32.0 (128b/130b)</td>
<td>2019</td>
</tr>
<tr>
<td>6.0</td>
<td>64.0 (128b/130b, PAM4, FLIT)</td>
<td>2021*</td>
</tr>
</tbody>
</table>
Upcoming PCIe 6.0 Specification Webinar

PCI-SIG Webinar Series

PCle® 6.0 Specification: The Interconnect for I/O Needs of the Future

June 4, 8:00 am - 9:00 am PT

REGISTRATION OPEN

Visit https://pcisig.com/events/webinars to register
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