M.2 Interoperability Warning

Executive Summary

The PCI-SIG® has released this document to make the industry and consumers aware of an incompatible use of the PCI Express® M.2 connector and form factor that could result in damage to a host system and / or Add-in-Card (AIC) when a non-M.2 compatible AIC is inserted into a M.2-compatible host or a M.2 AIC is inserted into a non-M.2 compatible host.

To ensure interoperability and to protect consumers, mechanical connectors are provisioned with a set of reserved pins—referred to as "No Connect" or NC pins—that can be used by future implementations to provide new functionality. To prevent problems and / or damage, M.2 compliant host and M.2 compliant AIC implementations are required to not connect these pins.

A third-party has developed a mechanical form factor called NGSFF or NF1 that does not comply with the M.2 specification as it connects a subset of NC pins for proprietary purposes. The use of these pins is in direct conflict with the latest M.2 specification which has allocated these pins to meet new, high-volume M.2 applications. To avoid interoperability and potential damage, a different mechanical key could be added to prevent an NGSFF AIC from being inserted into a M.2 host or a M.2 AIC from being inserted into an NGSFF host. By not adding such a mechanical key the industry and consumers could be placed at risk.

M.2 Evolution and High-volume Adoption

The M.2 version 1.0 specification was released in 2013, version 1.1 in 2015, and version 1.2 is scheduled to be released in late 2018. With each release, the PCI-SIG has expanded M.2 capabilities to meet new high-volume consumer requirements including: power loss notification, 1.8V I/O support, USB 2.0 (USB D- / USB D+) support, and on-board power disable capabilities to enable AICs to be reset to their power-on initialization state without requiring physical consumer intervention.

Since its initial release over 1 billion M.2 hosts and AICs have been shipped across multiple market segments including: enterprise and cloud data centers, PCs, embedded, and mobile solutions. Through it all, the PCI-SIG has conducted rigorous analysis to ensure forward and backward interoperability between all M.2 compliant host and AICs, and to reduce the probability of M.2 host or AIC damage.

NGSFF

Though it is common for industry bodies or third-parties to leverage or re-use mechanical connectors and form factors, most work with the mechanical specification's governing body to ensure interoperability and to prevent damage, or they incorporate mechanical keying to prevent mechanical mating between incompatible parts.

The following provides a high-level summary of the specific pin conflicts (see *Figure 1*) including interoperability concerns and the potential for host and / or AIC damage. This analysis is based on a public NGSFF presentation available at:
https://www.flashmemorysummit.com/English/Collaterals/Proceedings/2017/20170810_FC32_Wang.pdf.

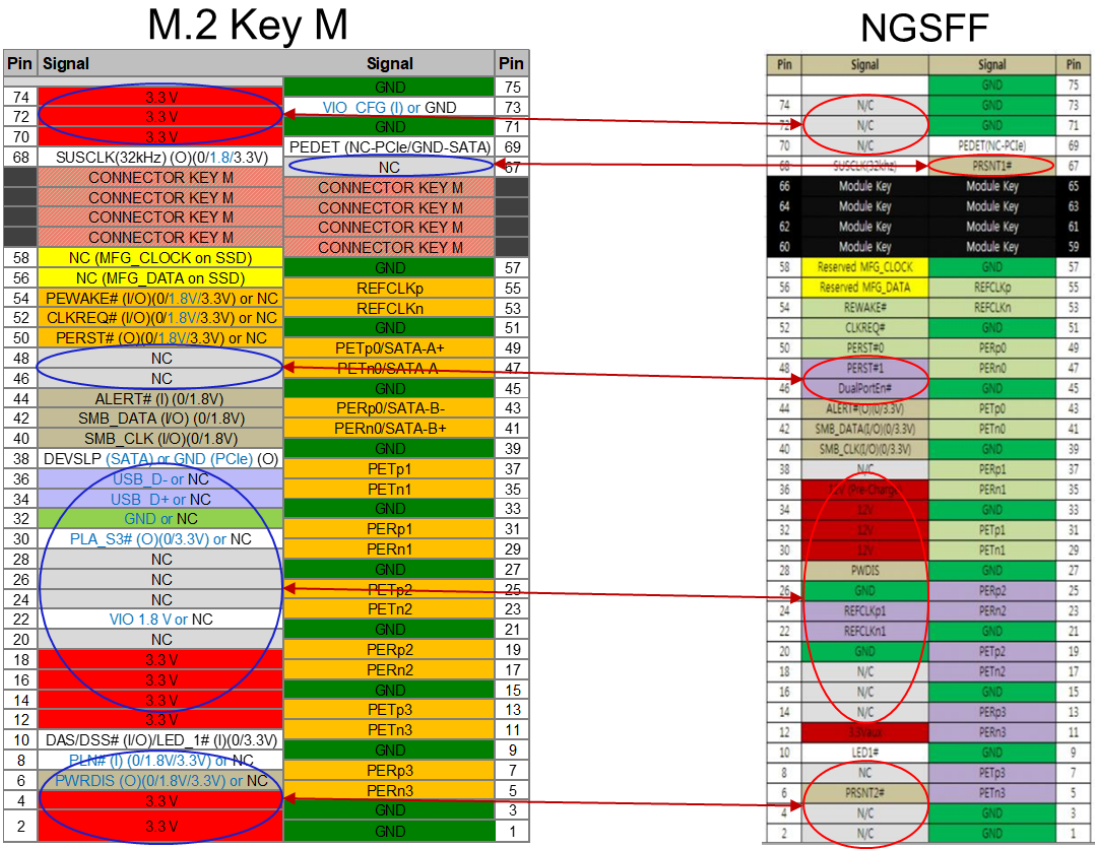

Figure 1: M.2 (Left) and NGSFF (Right) Pin Assignments with Differences Circled

M.2 and NGSFF Pin Conflict

Pin conflict summary:

- Potential M.2 host damage due to high current placed on M.2 host CMOS output - Pin 6 of M.2, PWRDIS, will connect to NGSFF PRSNT2#
- Potential M.2 host damage due to 3.3 V on M.2 host shorting to adjacent NGSFF Add-in Card Ground (pin 18 to pin 20).
- Potential M.2 Add-in Card and NGSFF host damage from shorting 12 V to Ground - Pin 32, M.2 Ground, will connect to NGSFF 12V.
- Potential end user impact/confusion from non-functioning devices - NGSFF Add-in Card not working in M.2 host system due to limited 3.3V on NGSFF.
- Potential NGSFF Add-in Card damage due to high current placed by M.2 host - pin 12, 3.3V power, will connect to NGSFF 3.3V Aux.
- Potential NGSFF Add-in Card damage due to out of spec voltage placed on one Add-in Card input signal - Pin 22, M.2 1.8V, connected to NGSFF REFCLKn1
- Unknown future issues due to NGSFF using 5 pins that M.2 may use in the future.

PRSNT2# on NGSFF and PWDIS vs. PWRDIS on M.2 (Pins 6, 28)

M.2 specifies pin 6 as PWRDIS (host output), and NGSFF specifies it as PRSNT2# (host input). If PRSNT2# is directly grounded on the NGSFF AIC, then the M.2 Host's PWRDIS pin will connect straight to ground. Though M.2 does not specify a maximum current, this atypical usage can result in I/O buffer electrical overstress, and potentially could cause permanent damage the M.2 host signal. Further, NGSFF specifies its PWRDIS functionality on a different pin 28, thus creating unnecessary duplication and complexity.

REFCLKp1/REFCLKn1 on NGSFF vs. VIO 1.8 V on M.2 (Pins 22, 24)

M.2 specifies pin 22 as a 1.8V power source (VIO 1.8 V), and NGSFF specifies it as REFCLKn1 (AIC input). If the NGSFF AIC supports PCI Express, then when an NGSFF AIC is inserted into an M.2 host, the M.2 host will drive 1.8V onto a pin that expects an absolute maximum input voltage (Vmax) of 1.15V. The increased voltage could damage the NGSFF AIC reference clock logic.

3.3V removal from NGSFF (pins 2, 4, 12, 14, 16, 18, 70, 72, 74)

M.2 specifies that a host provide 3.3V of power across the above pins, and NGSFF specifies only 3.3Vaux on one of these pins (NGSFF specifies that a host is to provide 12V of power across a different set of pins). If an NGSFF AIC is inserted into a M.2 host and the NGSFF AIC does not draw more than the maximum M.2 pin current limit, then due to insufficient power the AIC might not power up or function correctly. If the NGSFF AIC draws more than the maximum M.2 connector pin limit, then the M.2 connector pin could be overstressed which could result in damage to the M.2 host and/or the NGSFF AIC.

12V on NGSFF vs. USB D-/USB D+, GND, PLA_S3# on M.2 (Pins 30, 32, 34, 36)

M.2 specifies pin 30 as PLA-S3# (host input), pin 32 as GND, pin 34 as USB D+ (host output), and pin 36 as USB D- (host output). NGSFF specifies pins 30, 32, and 34 as 12V and pin 36 as 12V pre-charge. If an M.2 AIC is inserted into an NGSFF host, then 12V power would be connected to USB D+, USB D-, and GND. If an NGSFF host is unable to discern an M.2 AIC, then the NGSFF host and M.2 AIC could be damaged.

GND additions on NGSFF vs. NC on M.2 (Pins 20, 26)

M.2 specifies pin 20 and pin 26 as NC, and NGSFF specifies these as GND pins. If an NGSFF AIC is inserted into a M.2 host, then NGSFF AIC pin 20 would be located next to M.2 host pin 18 (3.3V power pin). If these pins were to make contact for any reason, then the M.2 host and NGSFF AIC could be damaged. To prevent such damage, M.2 and other industry standards do not locate power and ground pins where they could make contact. Further, since pin 20 and 26 are NC pins, future M.2 specifications will make use of these pins for other purposes.

PERST#1, DualPortEn#, and PRSNT1# on NGSFF vs. NC on M.2 (Pins 46, 48, 67)

M.2 specifies pins 46, 48, and 67 as NC, and NGSFF specifies these as DualPortEn#, PERST#1 and PRSNT1#. Future M.2 specifications will make use of these pins which could result in interoperability problems or damage.

Summary

The NGSFF or NF1 mechanical form factor is not-compatible with the M.2 specification as it connects a subset of NC pins for proprietary purposes. The use of these pins is in direct conflict with the latest M.2 specification, and could cause interoperability problems and host and/or AIC damage. All of these can be avoided by adding mechanical keying to ensure incompatible hosts and AICs do not mate. Given the industry has shipped over 1 billion M.2 host and AICs and 100s of millions more ship every year, the PCI-SIG believes it is critical for the industry and consumers to be aware of this situation to minimize impact to the industry and consumers.