PCI Express® Technology: Accelerating Automotive Connectivity, from Infotainment to ADAS

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PCI Express® Technology: Accelerating Automotive Connectivity, from Infotainment to ADAS

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Cadence
Topics

• Automotive Trends and Implications for SoC Design
• New Automotive SoC Segments
• PCIe® in Automotive Applications
• Use Cases
• Examples of Commercial Chips
• Summary
Automotive Trends and Implications
Major Forces Shaping the Automotive Industry

**Growth of Autonomous Driving**
- ADAS deployment
- Level 3 in 2019
- Level 4 by 2020~2025
- Security challenges

**Increased Connectivity**
- Multiple connectivity
  - Telematics services
  - V2X (4G/LTE → 5G)

**Vehicle Electrification**
- Some barriers
  - High battery costs
  - Proliferation of charging infrastructure
  - Wireless charging

**Shared Mobility**
- Uber
- Lyft
- Turo, etc.
Major Forces Shaping the Automotive Industry

Growth of Autonomous Driving
- ADAS deployment
- Level 3 in 2019
- Level 5 by 2025
- Improved driving ranges

Increased Connectivity
- Multiple connectivity options
- Telematics services
- V2X (5G)

Vehicle Electrification
- Some barriers:
  - High battery costs
  - Proliferation of charging infrastructure
  - Wireless charging

Shared Mobility
- Uber
- Lyft,
- Turo, etc.

Increased Connectivity
- ADAS deployment
- Level 3 in 2019
- Level 5 by 2025
- Improved driving ranges

Some clarity on DSRC vs C-V2X

Some barriers:
- Security challenges
- V2X (5G)

Long-term reliability

AUG 16-18, 2021
#DriveWorldESC
What Are These Trends Telling Us?

- New use cases
  - IVI, digital cockpit, DMS
  - ACC, AEB, ADAS, ADS
  - OTA, V2x . . .
- More chips, more integration, more custom
- Use of more advanced process nodes
  - 16nm, 7nm, 5nm . . .
- More compute intensive
  - Sensor fusion, DSP, AI
- More data
  - Collection, analysis, edge AI
- More software (a lot more)

- New architecture
  - Heterogeneous SoC
  - NoC (memory coherency)
  - MCU, domain and zonal transition (IVN)
- Higher speed memories
  - LPDDR5X, GDDR6, HBM2e
- Higher speed (connectivity) interfaces
  - PCIe® 3.0/4.0/5.0/6.0
- Larger storage
- More internet connectivity
  - Wi-Fi, 4G/5G, cellular v2x, DSRC
- More security
Automotive Market and Key Trends

- **Electrification**
- **Hybrid and EVs**

- **ADAS and Autonomous Driving**

- **Infotainment and Connectivity**
  - 4G → 5G, V2X

- **Zonal Architecture and ECU Consolidation**

**Auto Semiconductor Revenue by Domain ($M)**

- **CAGR: 4.6% (2021)** – Total semiconductor revenue
- **CAGR: 11.9% (2021)** – Auto semiconductor revenue!

**Key Trends**

- **16%** - ADAS: Part. Camera, Radar, Lidar Sensors
- **2%** - Body and Convenience
- **2%** - Chassis and Safety
- **25%** - HEV-EV
- **5%** - Infotainment: Connectivity and Telematics
- **-1%** - Powertrain

**Notes**

- **4G** → **5G**, V2X

**Source:** IHS

**Event:** Drive World ESC

**Date:** AUG 16-18, 2021

**Tag:** #DriveWorldESC
New SoCs Adopting Advanced Process Nodes

<table>
<thead>
<tr>
<th>Chassis, Powertrain, Body</th>
<th>Infotainment</th>
<th>ADAS</th>
<th>ADS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active suspension, ABS, Engine control</td>
<td>Digital cockpit and driver monitoring</td>
<td>Advanced driver-assistance system (L1~L3)</td>
<td>Autonomous driving system (L4~L5)</td>
</tr>
<tr>
<td>Mature foundry process (90nm, 65nm, and specialty process)</td>
<td>Mature foundry process (28nm, 16nm → 7nm)</td>
<td>Advanced foundry process (16nm → 7nm)</td>
<td>Advanced foundry process (7nm → 5nm)</td>
</tr>
</tbody>
</table>
New Automotive SoC Segments
New Automotive SoC Segments

- Infotainment and digital cockpit (including driver monitoring)
- ADAS (sensor fusion – camera, radar, lidar, ultrasound)
- Autonomous driving (L4/L5, ML/AI)
- Telematics (Wi-Fi, BT, C-V2X, GPS)
- Cloud connectivity (OTA, e-commerce)
Table-stake IP in infotainment SoC
• Multi-core CPU
• GPU
• Advanced memory
• MIPI®
• PCIe® 3.0/4.0
• Storage interface
• USB2/3
• GbE

An infotainment chip looks very much like a ruggedized applications processor for smartphones!
## From ADAS to Conditional Automation (Level 3)

<table>
<thead>
<tr>
<th>Level 0</th>
<th>Level 1</th>
<th>Level 2</th>
<th>Level 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Function</strong></td>
<td>Manual Cruise Ctrl</td>
<td>Traffic Sign Detection</td>
<td>Adaptive Cruise Control</td>
</tr>
<tr>
<td><strong>Features</strong></td>
<td>Manual set of fixed speed No detection of environment</td>
<td>Camera-based traffic sign detection Manual control of speed</td>
<td>Camera-based traffic sign detection Automatic control of speed and distance</td>
</tr>
<tr>
<td><strong>Sensor/ECU</strong></td>
<td>No sensors 1x ECU</td>
<td>1x front camera 1x ADAS ECU</td>
<td>1x front camera 1x front radar 1x ADAS ECU</td>
</tr>
</tbody>
</table>

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**We Are Here!**

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**Drive World ESC**

**AUG 16-18, 2021**
Autonomous Vehicles – Supercomputer on Wheels

UBER SELF-DRIVING VEHICLE SAFETY SENSOR SUITE

<table>
<thead>
<tr>
<th>Sensor Type</th>
<th>Volvo XC90</th>
<th>Ford Fusion</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIDAR</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>Radar</td>
<td>10</td>
<td>7</td>
</tr>
<tr>
<td>Camera</td>
<td>7</td>
<td>20</td>
</tr>
</tbody>
</table>

* Lidar uses laser light pulses to detect obstacles

Source: Uber
Images: Uber
W. Foe, 28/03/2018

Drive World ESC
AUG 16-18, 2021
## Evolution of Automated Driving Platforms

<table>
<thead>
<tr>
<th>TOPS / Watt</th>
<th>Mobileye</th>
<th>Audi</th>
<th>NVIDIA</th>
<th>Renesas</th>
<th>NVIDIA</th>
<th>Tesla</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25TOPS @ 2.5W</td>
<td>EyeQ3</td>
<td>zFAS</td>
<td>Drive PX2</td>
<td>R-Car V3U</td>
<td>Drive PX Pegasus</td>
<td>FSD Computer</td>
</tr>
<tr>
<td>&lt;1TOPS</td>
<td>Black box</td>
<td>Proprietary</td>
<td>Open system</td>
<td>Open system</td>
<td>Open system</td>
<td>Proprietary</td>
</tr>
<tr>
<td>20TOPS @ 250W</td>
<td>Standard components</td>
<td>Standard components</td>
<td>Standard components</td>
<td>Standard components</td>
<td>Standard components</td>
<td>Proprietary SoC</td>
</tr>
<tr>
<td>60TOPS</td>
<td>HW + SW</td>
<td>HW</td>
<td>HW + ML env.</td>
<td>HW</td>
<td>HW + ML env.</td>
<td>HW + SW + ML env.</td>
</tr>
<tr>
<td>320TOPS @ 500W</td>
<td>Air cooling</td>
<td>Air cooling</td>
<td>Water cooling</td>
<td>Air cooling</td>
<td>Water cooling</td>
<td>Air cooling</td>
</tr>
<tr>
<td>144TOPS @ 72W</td>
<td>We Are Here!</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Source: Audi, Mobileye, NVIDIA, Renesas, Tesla

**TOPS**

- 1TOPS = 1 Trillion Operations Per Second

**System Components**

- HW: Hardware
- SW: Software
- ML: Machine Learning
- Proprietary
- Open system

**Cooling Methods**

- Air cooling
- Water cooling
Perception from Vision, Radar, and Lidar Sensors Are Combined
AV Estimates Path of Surrounding Cars and Pedestrians
PCI Express® technology is mission critical in Domain and Zonal Network

- Already adopted in multiple generations of infotainment and ADAS SoC
- Key protocol in chip-to-chip communications, central processing and high-speed end point connections
PCI Express® Architecture in Automotive Applications
PCIe® Technology – A Ubiquitous Interface, Applied to Automotive

Empowering next generation of data intensive autonomous driving designs

Built on the state of the art 96-layer 3D NAND and leveraging the NVMe architecture to provide unmatched performance in automotive industry for years to come. The IX SN530 family is designed to support break through innovation development from the latest safety and driver assistance systems to autonomous driving.


 STORAGE

The Role of PCIe NVMe Industrial SSDs

At Electana Munich 2018, Micron officially launched the Micron 2100A/AT—an industrial- and automotive-grade PCIe NVMe Industrial SSD family based on 64-layer triple-level cell (TLC) 3D NAND technology. Available in 64GB-1TB BGA and 256GB-1TB M.2 form factors, the new 2100A/AT series is Micron’s first offering with a PCIe interface supporting the NVMe protocol that is designed to address the needs of the industrial segment: longevity, reliability, quality, ruggedness, and application-specific features such as namespace, autonomous power transitions, and boot emulation.

https://in.micron.com/about/blog/2018/deceber/the-role-of-pcie-nvme-industrial-ssds

PCIe®: One Base Specification – Multiple Form Factors

- BGA
  - 16x20 mm small and thin platforms
  - Smallest footprint of PCIe connector form factors, use for boot or for max storage density

- M.2
  - 42, 80, and 110mm

- U.2 2.5in (aka SFF-8639)
  - Majority of SSDs sold
  - Ease of deployment, hotplug, serviceability
  - Single-Port x4 or Dual-Port x2

- CEM Add-in-card
  - Add-in-card (AIC) has maximum system compatibility with existing servers and most reliable compliance program. Higher power envelope, and options for height and length

Multiple form factors from the same silicon to meet the needs of different segments

High B/W with PCIe 3.0 Prevalent in hand-held, IoT, automotive

AUG 16-18, 2021 #DriveWorldESC
Standard Has Headroom for I/O Bandwidth Needs

I/O Bandwidth Doubles Every 3 Years
(Data Source: PCI SIG)

Bandwidth GB/s

PCI 1.0 x16
PCIe 2.0 x16
PCIe 3.0 x16
PCIe 4.0 x16
PCIe 5.0 x16
PCIe 6.0 x16


Bandwidth GB/s

PCI 1.0 x16
PCIe 2.0 x16
PCIe 3.0 x16
PCIe 4.0 x16
PCIe 5.0 x16
PCIe 6.0 x16


(Aug 16-18, 2021 #DriveWorldESC)
Automotive Applications Meet PCIe® Technology

**Compute Performance**
High bandwidth, scalable applications

**System Performance**
Latency, virtualization, scalability, security reach, functional safety, storage

**Silicon Performance**
Power and thermal requirements
Silicon reliability in advanced process nodes
Compute Drivers

- ADAS Controllers
- Automotive SoC
- AI Accelerator
- Infotainment Controller
- AI Accelerator
- Automotive SoC
- Graphics Processing Unit

**Requirement** | **PCIe Support**
---|---
Bandwidth | Architecture version/Lane combination
Scalability | Configurable number of lanes
Low latency | Protocol timers and implementation dependencies
Virtualization | SR-IOV
Power management | ASPM, DPA, L1 substates, etc.
Security/trusted environments | IDE/DOE, ADISP
Functional Safety (FuSa) | Implementation specific
PCIe® Technology as the Data Backbone

ECU Processing Redundancy

2025+

- Bandwidth (5-40Gbps)
  - Architecture version/Lane combination

- Low latency
  - Protocol timers and implementation dependencies

- Long reach
  - Standard and implementation (EMC/EMI, reliability)

- Security/trusted environments
  - IDE/DOE, ADISP

- Functional Safety (FuSa)
  - Implementation

Sensor Fusion

Source: ON Semi webinar, 5/2021
## Storage Evolves Towards PCIe® SSDs

**Requirements**

<table>
<thead>
<tr>
<th>Feature</th>
<th>High Endurance</th>
<th>Very Low Latency</th>
<th>Very High Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lifetime &gt; 15 years</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High temp data retention</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Automotive Grade 1 and/or Grade 2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Guaranteed minimum performance for writes</td>
<td></td>
<td></td>
<td>Virtualization capabilities</td>
</tr>
<tr>
<td>Fast boot, fast startup</td>
<td></td>
<td></td>
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**PCIe®/NVMe SSDs Are Widely Used as Storage Solutions**

<table>
<thead>
<tr>
<th>Feature</th>
<th>PCIe RAS Features</th>
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<tr>
<td>Link CRC, ACK/NAK, Replay</td>
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<tr>
<td>ACK/NAK timeouts</td>
<td>ACK/NAK timeouts</td>
</tr>
<tr>
<td>End to End CRC</td>
<td>End to End CRC</td>
</tr>
<tr>
<td>Power</td>
<td>L1 substates</td>
</tr>
<tr>
<td>Clocking</td>
<td>SRIS</td>
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## Connectivity Applications with PCIe® Technology

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<th>PCIe Support</th>
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<td>Scalable bandwidth</td>
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<td>Implementation dependent</td>
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- **LTE/5G Modem**
- **Wi-Fi/BT**
- **GPS/GNSS**
- **V2X/V2V**
Stringent Automotive Requirements

• Standardization
  • Well-defined roadmap for protocol
  • Commercial (long-term) availability from diverse suppliers
  • Interoperability

• Certification and qualification for harsher environments and functional safety
  • AEC- Q100/ISO 26262 processes
  • EMC/EMI requirements
  • Temperature and mechanical

• Safety and security
  • End to end measures
  • Regulatory compliance

• Lifetime
  • Aging requirements
  • Long-term availability, migration, upgrades
  • Backwards/forward compatibility
Commercial Automotive SoC Examples
Infotainment SoC

PCIe® interfaces to WiFi/Bluetooth module

Source: Renesas website
ADAS SoC

Two 16G PCIe® 4.0 interfaces built-in

Source: Mobileye website
PCIe® Architecture Addresses Advanced Automotive SoC Needs

- Established standards body, vibrant ecosystem, strong technical leadership

- Protocol specification and implementation meet the segment needs
  - Bandwidth, scalability, latency, security, reach, reliability

- Compliance and certification

- Broad silicon, software, and IP provider base and ecosystem

- Automotive Working Group established in PCI-SIG® to continue work on this exciting new frontier!
Thank you!

QUESTIONS?