1. PCI Standard Hot-plug Engineering Change Notice – SHPC memory access granularity

TITLE:	SHPC memory access granularity
DATE:	March 25, 2003
AFFECTED DOCUMENT(S):	PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0
SPONSOR:	Alan Goodrum, Hewlett-Packard and Sridhar Muthrasanallur, Intel

1.1. Summary of the Functional Changes

Restrict PCI Standard Hot-Plug (SHPC) device drivers to a memory access granularity of maximum one DWORD (aligned) when reading or writing to the SHPC memory space.

1.2. Benefits

PCI Express to PCI(-X) bridges integrating an SHPC can be simplified to always handle single DWORD or smaller memory reads and writes from PCI Express to the SHPC memory space.

1.3. Assessment of the Impact

The change allows for a simplification of PCI Express to PCI-X bridges and has no impact on PCI-X bridges. It is believed that no SHPC device drivers have yet been shipped. And the new restriction imposed by this ECN on the SHPC device driver is a natural one, which most software writers would tend to follow even without the new requirement.

1.4. Analysis of the Hardware Implications

PCI Express to PCI(-X) bridge logic can be simplified to always handle only one DWORD memory reads and writes from PCI Express to the Standard Hot-Plug Controller memory space. There is no impact on an SHPC integrated with a conventional PCI or PCI-X bridge.

1.5. Analysis of the Software Implications

Standard Hot-Plug device drivers must not issue memory reads or writes greater than a DWORD (aligned) to the Standard Hotplug Controller memory space.

1.6. Additional Description and Rationale

Restricting the size of memory reads and writes that SHPC device drivers will issue to the SHPC provides an opportunity for simplifying the PCI-Express to PCI(-X) bridge hardware that integrates an SHPC. Simplification is achieved in that the bridge hardware has to only handle lengths for memory reads and writes to the SHPC memory space of maximum 1 DWORD. Allowing for PCI Express bridge hardware to only handle 1 DWORD memory writes to SHPC memory space is possible because PCI Express prohibits write combining and PCI Express bridges can be designed to handle this restricted length as long as the device driver does not issue any memory write greater than a DWORD to the SHPC memory space. Allowance for any bridge integrating an SHPC to restrict the size of memory reads to SHPC memory space to 1 DWORD maximum is already allowed by the SHPC 1.0 spec, provided the bridge clears the prefetchable bit in the SHPC's memory Base Address Register. This ECN makes the maximum memory read size requirement on the SHPC device driver independent of the prefetch bit in the SHPC's memory Base Address Register.

Details of Changes

Change Instruction: Change Section 4 on pg 97 as follows:

4. SHPC Programming Interface

This chapter defines the software-programming interface for the SHPC. The programming interface assumes the system design requirements defined in Section 4.1. This chapter also describes how software discovers SHPCs in a system (see Section 4.3).

The SHPC programming interface includes the SHPC Working Register set defined in Section 4.5. The SHPC Working Register set implements the command interface defined in Section 4.6. The command interface gives software the ability to control Hot-Plug slots and the bus segment that contains the Hot-Plug slots. The SHPC monitors the slots it controls for events. When the SHPC detects an event, it may optionally be programmed to generate a System Interrupt, assert the Wakeup Signal, or pulse **SERR#** (see Section 4.7).

All SHPCs must implement the programming interface defined in this section.

When reading or writing the registers identified in the programming interface via memory space, the SHPC device driver must use memory accesses that do not cross a naturally aligned DWORD boundary.