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PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Generic Capability Structure for SATA Host Bus Adapters
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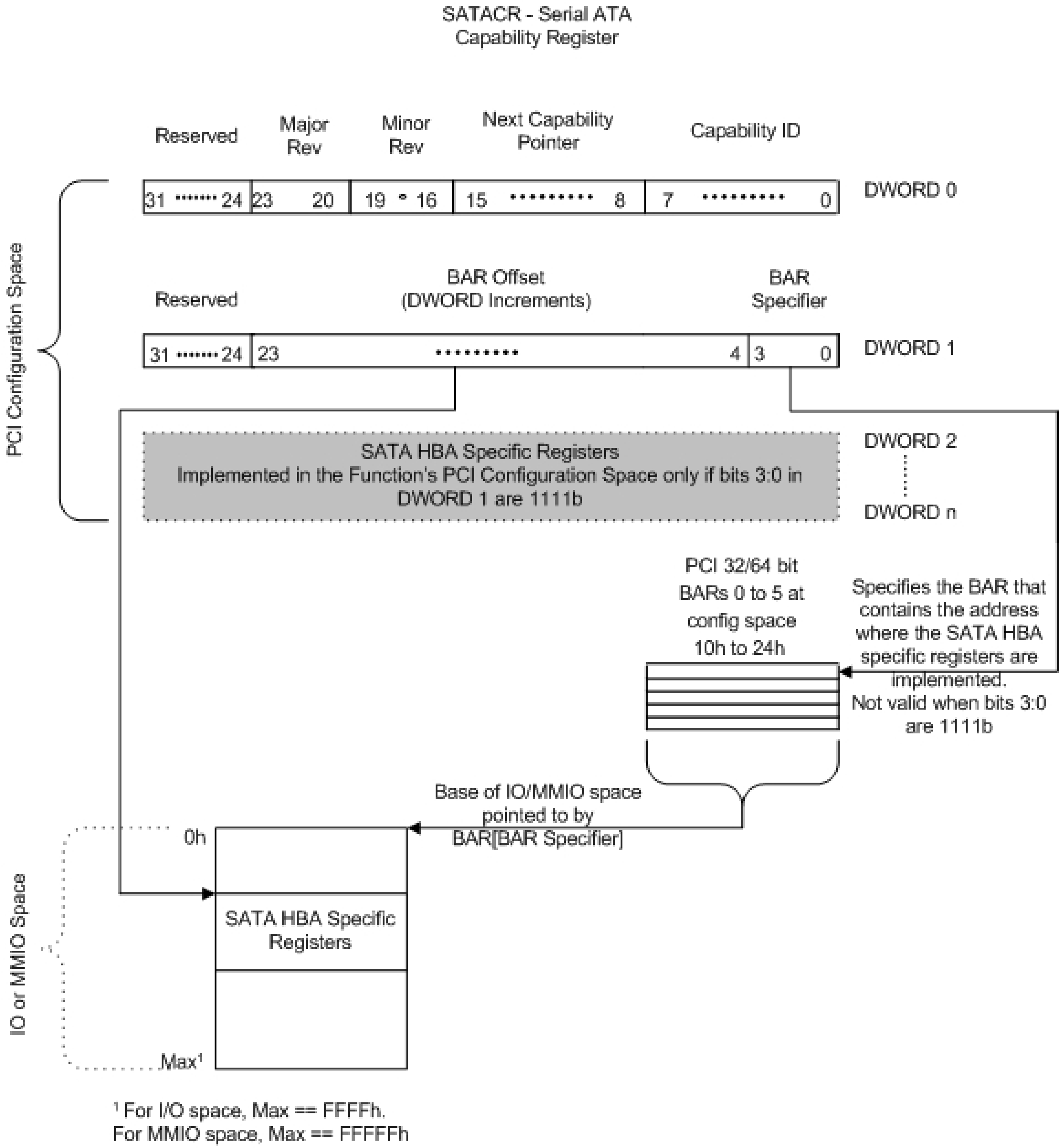
Part I

1. Summary of the Functional Changes

The functional changes proposed involve the definition of a new Capabilities List ID (and associated Capability register set). This new Capabilities ID will identify to system firmware (BIOS/OROM), a Serial ATA (SATA) host bus adapter's (HBA) support of optional features that may be defined in the particular SATA HBA specification (i.e. Advanced Host Controller Interface - AHCI). ***It is important to note that this capability register is intended for use by pre-boot software that may not have the ability to access SATA HBA specific MMIO registers that reside above 1MB. OS specific device drivers do not have this limitation and are expected to determine optional SATA HBA features through an examination of the HBA's specific capability register, which may be found in IO or MMIO space – this is SATA HBA specification dependent.***

The capabilities provided by the SATA HBA are HBA specification specific; it is the responsibility of the system firmware to comprehend the exact implementation. The following outlines the format of the new Capability register:


SATACR - Serial ATA
Capability Register
Reserved
Major Rev
Minor Rev
Next Capability Pointer
Capability ID
31 ••••••• 24
23 20
19 • 16
15 ••••••••• 8
7 ••••••••• 0
DWORD 0
Reserved
BAR Offset (DWORD Increments)
BAR Specifier
31 ••••••• 24
23 ••••••••• 4
3 0
DWORD 1
PCI Configuration Space
SATA HBA Specific Registers
Implemented in the Function's PCI Configuration Space only if bits 3:0 in DWORD 1 are 1111b
DWORD 2
DWORD n
PCI 32/64 bit BARs 0 to 5 at config space 10h to 24h
Specifies the BAR that contains the address where the SATA HBA specific registers are implemented.
Not valid when bits 3:0 are 1111b
Base of IO/MMIO space pointed to by BAR[BAR Specifier]
0h
SATA HBA Specific Registers
Max¹
IO or MMIO Space
¹ For I/O space, Max == FFFFh.
For MMIO space, Max == FFFFFh

Where:

DWORD 0

Bits [7:0] – **PCI SIG assigned Capability ID**. This SATA HBA feature has been assigned a Capability ID of **12h**.
Bits [15:8] – Pointer to Next Capability. Specifies the offset into PCI configuration space where the next Capability pointer resides.
Bits [19:16] – **Minor Revision.** Specifies the minor revision level to which the capability register is built. This may differ across SATA HBA implementations and is SATA HBA specification specific**.**
Bits [23:20] – **Major Revision**. Specifies the major revision level to which the capability register is built. This may differ across SATA HBA implementations and is SATA HBA specification specific.
Bits [31-24] – Reserved. Must return zero when read.

DWORD 1

Bits [3:0] – **BAR Specifier.** Specifies which IO/MMIO space BAR in the function's PCI configuration space contains the SATA HBA specific registers. These bits represent an absolute offset (DWORD increments) into the device's PCI configuration space. These bits are read-only and may be assigned one of the following values:

0100b = 10h (BAR 0)
0101b = 14h (BAR 1)
0110b = 18h (BAR 2)
0111b = 1Ch (BAR 3)
1000b = 20h (BAR 4)
1001b = 24h (BAR 5)
1111b = SATA HBA specific register (s) is implemented in the SATA HBA's PCI Configuration space
All other bit combinations are reserved.

Bits [23:4] – **BAR Offset.** Specifies the offset (DWORD increments) into the IO/MMIO space BAR where the SATA HBA specific registers are located. These bits are read-only and may be assigned (by hardware) the following range of values:

- For SATA HBA implementations that implement their specific registers in IO space, this value shall be in the range of 0000h – 3FFFh. This allows the SATA HBA specific registers to be located anythere in the 64K IO space (3FFFh * 4).
    - Example: Assume a SATA HBA implementation whose optional registers are located in a block of IO address space specified by the value contained in BAR 4 (with an assigned value of 1C00h). The absolute start location of the SATA HBA registers in IO space is determined by adding the BAR to the BAR Offset value * 4. Therefore, for a BAR value of 1C00h and a BAR Offset value of 2, the absolute start IO address of the SATA HBA registers will be: 1C00h + (2 << 2) or 1C08h.
- For SATA HBA implementations that implement their specific registers in MMIO space, this value shall be in the range of 00000h – 3FFFFh. This allows the SATA HBA specific registers to be located anywhere within the 1MB of memory space (3FFFFh * 4). Computing the absolute start address of the SATA HBA registers is similar to the mechanism used for IO addressing.

If the SATA HBA specific register are implemented in the SATA HBA's PCI Configuration space, then these bits are '0' (zero) and are ignored by the platform firmware.

Bits [31-24] – Reserved. Must return zero when read.

DWORD 2-n

SATA HBA Registers. Specifies the SATA HBA specific registers. Only valid if bits 3:0 of DWORD 1 are 1111b. *Implementing the SATA HBA specific registers in PCI configuration space is useful for those HBA implementations that do not wish to provide IO decoders or do not want to provide a MMIO decoder for <1MB accesses.*

2. Benefits as a Result of the Changes

Allows SATA HBA implementations to make easily discoverable to system firmware/pre-boot software, registers that are described in a particular SATA HBA specification (i.e. AHCI) but whose location in PCI Configuration space is IHV implementation specific. This feature also benefits OEMs who may have test suites that are sensitive to register movements; this feature does not necessitate rewriting of software.

3. Assessment of the Impact

No impact to the current specification and no impact to devices that currently conform to the PCI specification. This addition only applies to new SATA devices that require this feature.

4. Analysis of the Hardware Implications

The entire SATACR is implemented as read-only.

5. Analysis of the Software Implications

No SW implications. SW is free to ignore this feature. This feature is intended for pre-boot software, system test tools only and other software that cannot access MMIO space located above 1MB.

Part II

Detailed Description of the change

Table H-1: Capability IDs

This ECN reserves the Capability ID of 12h for use by Serial ATA host bus adapters:

Table H-1: Capability IDs

ID	Capability
00h – 11h	Reserved or currently assigned
12h	Serial ATA - Indicates a Serial ATA (SATA) host bus adapter's (HBA) support of optional features that are defined in the particular SATA HBA implementation's specification.
13h-FFh	Reserved