PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Enable PCIe and USB 3.1 Gen1 on M.2 Card Key B
DATE:	February 10, 2017
AFFECTED DOCUMENT:	PCI Express M.2 Specification, Revision 1.1
SPONSOR:	Jim Panian, Qualcomm Technologies Inc.

Part I

1. Summary of the Functional Changes

M.2 Key B (WWAN) is modified to enable PCIe and USB 3.1 Gen1 signals to be simultaneously present on the connector. This enables support for a single SKU M.2 card that supports both PCIe and USB 3.1 Gen1. There are two implementation options enabled:

1. State #14 in the "Socket 2 Add-in Card Configuration Table" is re-defined to indicate an Add-in Card built to the *PCI Express M.2 Specification, Revision 1.1* or later where both PCIe and USB 3.1 Gen1 are both present on the connector. The choice of Port Configuration is vendor defined. This enables the host to unambiguously determine that PCIe and USB 3.1 Gen1 are present on the connector.

2. States #4, 5, 6, 7 in the "Socket 2 Add-in Card Configuration Table" are re-defined to indicate that in addition to USB 3.1 Gen1, PCIe may be present on the connector. This definition was used by M.2 cards built to the *PCI Express M.2 Specification, Revision 1.0* (USB 3.1 Gen1 on connector; PCIe is "no connect"). This definition is now also permitted to be used by M.2 cards built to *PCI Express M.2 Specification, Revision 1.1* or later to indicate that PCIe and USB 3.1 Gen1 are both present on the connector. This allows GPIO port configurations to remain consistent with all other existing states.

2. Benefits as a Result of the Changes

An M.2 card as a single SKU may be designed for insertion into a:

- Host system that only supports PCIe
- Host system that only supports USB 3.1 Gen1
- Host system that supports PCIe and/or USB 3.1 Gen1

3. Assessment of the Impact

This feature is optional. It will have no impact on existing M.2 card implementations. Existing M.2 platforms may not support the PCIe interface on newer cards advertising States 4-7. Existing M.2 platforms may not support newer cards advertising State 14.

4. Analysis of the Hardware Implications

Hardware changes are required to take advantage of this new optional capability.

5. Analysis of the Software Implications

None.

6. Analysis of the C&I Test Implications

None.

Part II

Detailed Description of the changes

Change Table 29, page 143, as follows:

Table 29. Socket 2 Add-in Card Configuration

State #	Add-in Card Configuration Decodes				Add-in Card Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	NC	GND	GND	SSD – PCIe	N/A
2	GND	GND	NC	GND	WWAN – PCIe	0
3	GND	NC	NC	GND	WWAN – PCIe	1
4	GND	GND	GND	NC	WWAN – PCIe, USB3.1 Gen1	0[4, 5]
5	GND	NC	GND	NC	WWAN – PCIe, USB3.1 Gen1	1[4, 5]
6	GND	GND	NC	NC	WWAN – PCIe, USB3.1 Gen1	2[4, 5]
7	GND	NC	NC	NC	WWAN – PCIe, USB3.1 Gen1	3[4, 5]
8	NC	GND	GND	GND	WWAN – SSIC	0
9	NC	NC	GND	GND	WWAN – SSIC	1
10	NC	GND	NC	GND	WWAN – SSIC	2
11	NC	NC	NC	GND	WWAN – SSIC	3
12	NC	GND	GND	NC	WWAN – PCIe	2
13	NC	NC	GND	NC	WWAN – PCIe	3
~~14~~	~~NC~~	~~GND~~	~~NC~~	~~NC~~	~~RFU~~	~~N/A~~
14	N/C	GND	N/C	N/C	WWAN – PCIe, USB3.1 Gen1	Vendor Defined[3, 5]
15	NC	NC	NC	NC	No Add-in Card Present	N/A

Notes:

1 USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)

2 Applicable to WWAN only

3 Permitted for use by an Add-in Card built to the *PCI Express M.2 Specification, Revision 1.1* or later where PCIe and USB3.1 Gen1 are both present on the connector. Vendor defined choice of port configurations 0, 1, 2, 3. Refer to Table 32x.

4 Used by an Add-in Card where USB3.1 Gen1 is present on the connector and PCIe is no-connect. Refer to Table 31. Permitted for use by an Add-in Card built to the *PCI Express M.2 Specification, Revision 1.1* or later where PCIe and USB3.1 Gen1 are both present on the connector. Refer to Table 32x.

5 Only a single lane of PCIe is available in these configurations.

Change Section 3.2.15.1, page 144 as follows:

3.2.15.1 Socket 2 Key B Pinout Definitions

The following tables list the signal pinouts for the Adapter edge card connector:

- Table 30. Socket 2 Key B SSIC-based WWAN Adapter Pinouts
- Table 31. Socket 2 Key B USB3.1 Gen1-based WWAN Adapter Pinout
- Table 32. Socket 2 Key B PCIe-based WWAN Adapter Pinout
- Table 32x. Socket 2 Key B PCIe/USB3.1 Gen1-based WWAN Adapter Pinout

All ~~three~~ four of these WWAN pinouts also support legacy USB2.0-based WWAN solutions or optionally HSIC.

See Table 29 for a list of Socket 2 configuration bits on the Add-in Card used to identify the desired pinouts and Port Configuration.

Editorial Note: Adjust all subsequent table numbers due to the addition of the new table.

Add a new table after Table 32, page 147 as follows:

Table 32x. Socket 2 Key B PCIe/USB3.1 Gen1-based WWAN Adapter Pinout

Pin	Signal	Signal	Pin
		CONFIG_2 (States 4, 5, 6, 7 and 14)	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	CONFIG_1 (States 4, 5, 6, 7 and 14)	69
68	SUSCLK(32kHz) (I)(0/3.3V)	RESET# (I)(0/1.8V)	67
66	SIM_DETECT (I)	ANTCTL3 (O)(0/1.8V)	65
64	COEX_TXD (O)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
62	COEX_RXD (I)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (O)(0/1.8V)	59
58	N/C	GND	57
56	N/C	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V)	GND	51
50	PERST# (I)(0/3.3V)	PERp0	49
48	VENDOR DEFINED or GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	PERn0	47
46	VENDOR DEFINED or GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V*)	GND	45
44	VENDOR DEFINED or GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V*)	PETp0	43
42	VENDOR DEFINED or GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V*)	PETn0	41
40	VENDOR DEFINED or GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/IPC_0 (I/O)(0/1.8V*)	GND	39
38	N/C	USB3.1-Rx+	37
36	UIM-PWR (O)	USB3.1-Rx-	35
34	UIM-DATA (I/O)	GND	33
32	UIM-CLK (O)	USB3.1-Tx+	31
30	UIM-RESET (O)	USB3.1-Tx-	29
28	VENDOR DEFINED or GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	VENDOR DEFINED or GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8V)	25
24	VENDOR DEFINED or GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	VENDOR DEFINED or GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	VENDOR DEFINED or GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	CONFIG_0 (States 4, 5, 6, 7 and 14)	21
20	VENDOR DEFINED or GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
10	VENDOR DEFINED or GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	GND	11
8	W_DISABLE1# (I)(0/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (I)(0/1.8V)	USB_D+	7
4	3.3V	GND	5
2	3.3V	GND	3
		CONFIG_3 (States 4, 5, 6, 7 and 14)	1

Change Section 5.2.1, page 176, as follows:

5.2.1 Socket 2 Module Key B

5.2.1.1 Socket 2 Module Key B – Configuration Pin Definitions

The Socket 2 Key (Mechanical Key B) is unique in that it enables five major pinouts configurations and four variants for each of the three WWAN configurations. The five major configurations supported are:

- WWAN that is PCIe Based
- WWAN that is SSIC Based
- WWAN that is USB3.1 Gen1 or PCIe/USB3.1 Gen1 Based
- SSD that is PCIe (2 lane) Based
- SSD that is SATA Based

Change Table 51, page 177, as follows:

Table 51. Socket 2 Add-in Card Configuration Table

Add-in Card Configuration Decodes				Add-in Card Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN – PCIe	0
0	1	1	0	WWAN – PCIe	1
0	0	0	1	WWAN - PCIe, USB3.1 Gen1	0[4, 5]
0	1	0	1	WWAN - PCIe, USB3.1 Gen1	1[4, 5]
0	0	1	1	WWAN - PCIe, USB3.1 Gen1	2[4, 5]
0	1	1	1	WWAN - PCIe, USB3.1 Gen1	3[4, 5]
1	0	0	0	WWAN - SSIC	0
1	1	0	0	WWAN - SSIC	1
1	0	1	0	WWAN - SSIC	2
1	1	1	0	WWAN - SSIC	3
1	0	0	1	WWAN - PCIe	2
1	1	0	1	WWAN - PCIe	3
~~1~~	~~0~~	~~1~~	~~1~~	~~RFU~~	~~N/A~~
1	0	1	1	WWAN – PCIe, USB3.1 Gen1	Vendor Defined[3, 5]
1	1	1	1	No Add-in Card Present	N/A

Notes:

1. USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3).
2. Applicable to WWAN only.
3. Permitted for use by an Add-in Card built to the *PCI Express M.2 Specification, Revision 1.1* or later where PCIe and USB3.1 Gen1 are both present on the connector. Vendor defined choice of port configurations 0, 1, 2, 3. Refer to Table 32x.
4. Used by an Add-in Card where USB3.1 Gen1 is present on the connector and PCIe is no-connect. Refer to Table 31. Permitted for use by an Add-in Card built to *PCI Express M.2 Specification, Revision 1.1* or later where PCIe and USB3.1 Gen1 are both present on the connector. Refer to Table 32x.
5. Only a single lane of PCIe is available in these states.