Errata for the PCI Express® OCuLink Specification Revision 1.0

May 27, 2016

REVISION	REVISION HISTORY	DATE
1.0	First Release. Includes A100.	2016-05-27

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Note on Errata Numbering

Errata numbering is arbitrary and reflects numbers used during the development process.

A100 [OCuLink 1.0 Spec] Mating Sequence Table 3-2, Pin A11

In Section 3.2.2, page 10, make the following changes:

3.2.2 Pinout for x4 Fixed Internal Connector (end point)

- **See Table 6-9 for the Full Crossover Internal Cable wiring.**
- **The sideband signal assignment differs between the root and end point.**
- **The Fixed side must provide the 3.3 V to support the optional active cable.**

Table 3-2. Pinout for x4 Fixed Internal Connectors (end point)

Pin #	Description	Mating Sequence of cable to board		Pin #	Description
Row Offset – no pin this side			2nd	B1	RESERVED
A1	POWER 3.3 Vact RX	2nd	1st	B2	GROUND
A2	GROUND	1st	2nd	B3	PETp0
A3	PERp0	2nd	2nd	B4	PETn0
A4	PERn0	2nd	1st	B5	GROUND
A5	GROUND	1st	2nd	B6	PETp1
A6	PERp1	2nd	2nd	B7	PETn1
A7	PERn1	2nd	1st	B8	GROUND
A8	GROUND	1st	2nd	B9	BP TYPE
A9	2-WIRE CLOCK	2nd	2nd	B10	CWAKE#
A10	2-WIRE DATA	2nd	1st	B11	GROUND
A11	GROUND	1st~~2nd~~	2nd	B12	VSP
A12	PERST#	2nd	2nd	B13	VSP
A13	CPRSNT#	2nd	1st	B14	GROUND
A14	GROUND	1st	2nd	B15	PETp2
A15	PERp2	2nd	2nd	B16	PETn2
A16	PERn2	2nd	1st	B17	GROUND
A17	GROUND	1st	2nd	B18	PETp3
A18	PERp3	2nd	2nd	B19	PETn3
A19	PERn3	2nd	1st	B20	GROUND
A20	GROUND	1st	2nd	B21	POWER 3.3 Vact TX
A21	RESERVED	2nd	Row Offset – no pin this side		