Errata for the PCI Express® Base Specification Revision 2.0

February 27, 2009

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Contents

A1 Message Request Rules

In Section 2.2.8, page 69, line 19, add the following text:

- ❑ AT[1:0] must be 00b. Receivers are not required or encouraged to check this.

A2 Completion Rules

In Section 2.2.9, page 80, line 27, add the following text:

- Lower Address[6:0] – lower byte address for starting byte of Completion
  - ♦ For Memory Read Completions, the value in this field is the byte address for the first enabled byte of data returned with the Completion (see the rules in Section 2.3.1.1)
  - ♦ This field is set to all 0's for all types of Completions other than Memory Read Completions. Receivers may optionally check for violations of this rule. See Section 2.3.2, second bullet for details.

In Section 2.3.2, page 98, line 4, make the following edit:

- ❑ ~~If a received Completion is not malformed and matches the Transaction ID of an outstanding Request, but in some other way does not match the corresponding Request, it is permitted for the receiver to handle the Completion as an Unexpected Completion~~
- ❑ If a received Completion matches the Transaction ID of an outstanding Request, but in some other way does not match the corresponding Request (e.g., a problem with Attributes, Traffic Class, Byte Count, Lower Address, etc), it is strongly recommended for the Receiver to handle the Completion as a Malformed TLP. However, if the Completion is otherwise properly formed, it is permitted[footnote] for the Receiver to handle the Completion as an Unexpected Completion.

[footnote] For the case where only the Byte Count or Lower Address fields mismatch the expected values for a Memory Read Request, it is actually recommended for the Receiver to handle the Completion as an Unexpected Completion, since the mismatch might be caused by a previous Completion being misrouted.

A3 Completion Rules

In Section 2.2.9, page 82, line 10, add the following text:

- ❑ AT[1:0] must be 00b. Receivers are not required or encouraged to check this.

A4 Recovery.RcvrLock

In Section 4.2.6.4.1, page 216, line 27, make the following edit:

- Else the next state is Configuration and the directed_speed_change variable is reset to 0b if any of the configured Lanes that are receiving a TS1 or TS2 Ordered Set have received at least one TS1 or TS2 with Link and Lane numbers that match what is being transmitted on those same Lanes and the operating speed has not changed to a mutually negotiated data rate (i.e., changed_speed_recovery = 0b) since entering Recovery and at least one of the following conditions is true:…

A5 Recovery.RcvrCfg

In Section 4.2.6.4.3, page 220, line 13, make the following edit:

- 16 TS2 Ordered Sets are sent after receiving one TS2 Ordered Set without being interrupted by any intervening EIEOS. The changed_speed_recovery variable and the directed_speed_change variable are ~~is~~ reset to 0b on entry to Recovery.Idle.

In Section 4.2.6.4.3, page 220, line 27, make the following edit:

The changed_speed_recovery variable and the directed_speed_change variable are ~~is~~ reset to 0b if the LTSSM transitions to Configuration.

A6 Hardware Autonomous Speed Disable

In Section 7.8.19, page 489, Table 7-25, Bit 5, make the following edit:

Bit Location	Register Description	Attributes
5	**Hardware Autonomous Speed Disable** – When Set, this bit disables hardware from changing the Link speed for device-specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this bit. …	RWS/RsvdP (see description)

A7 ACS Violation Status

In Section 7.10.2, page 498, Table 7-29, Bit 21, add the following text:

Bit Location	Register Description	Attributes	Default
21	**ACS Violation Status** (Optional)	RW1CS	0b

A8 ACS Violation Mask

In Section 7.10.3, page 499, Table 7-30, Bit 21, add the following text:

Bit Location	Register Description	Attributes	Default
21	**ACS Violation Mask** (Optional)	RWS	0b

A9 ACS Violation Severity

In Section 7.10.4, page 500, Table 7-31, Bit 21, add the following text:

Bit Location	Register Description	Attributes	Default
21	**ACS Violation Severity** (Optional)	RWS	0b

A10 ECRC Check Capable

In Section 7.10.7, page 503, Table 7-34, Bit 7, make the following edit:

Bit Location	Register Description	Attributes
7	**ECRC Check Capable** – If Set, this bit indicates that the Function is capable of checking ECRC (see Section 2.7). ~~Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b.~~	RO

A11 ECRC Check Enable

In Section 7.10.7, page 503, Table 7-34, Bit 8, add the following text:

Bit Location	Register Description	Attributes
8	**ECRC Check Enable** – When Set, ECRC checking is enabled (see Section 2.7). Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	RWS

A12 VC Enable

In Section 7.18.7, page 562, Table 7-74, Bit 31, edit as follows:

Bit Location	Register Description	Attributes
31	**VC Enable** – When Set, this bit enables a Virtual Channel (see note 1 for exceptions). The Virtual Channel is disabled when this bit is cleared. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. ~~When the VC Negotiation Pending bit is cleared, a 1b read from the VC Enable bit indicates that the VC is enabled (Flow Control initialization is completed for the PCI Express Port); a 0b read from this bit indicates that the Virtual Channel is currently disabled.~~ Default value of this bit is 1b for the first VC resource and ~~is~~ 0b for other VC resource(s). …	RW

A13 Loopback.Entry

In Section 4.2.6.10.1, page 233, line 8, make the following edits:

- The loopback master must transmit 16 consecutive TS1 Ordered Sets with the Data Rate field and the Selectable De-emphasis bit (Symbol 4 bit 6) identical to the TS1 Ordered Sets it transmitted during the Configuration.LinkWidth.Start substate and with the Loopback bit (bit 2 of Symbol 5) asserted, followed by the EIOS (one EIOS if the current Link speed is 2.5 GT/s or two consecutive EIOSs if the current Link speed is greater than 2.5 GT/s), and then go to Electrical Idle. The loopback master must go to Electrical Idle, after sending the EIOS(s), for 1 ms. During this time the speed must be changed to the highest common transmitted and received Link speed advertised on two consecutive TS1 Ordered Sets. ~~The select_deemphasis variable must be set equal to the Selectable De-emphasis bit (Symbol 4 bit 6) in the two consecutive TS1 or TS2 Ordered Sets prior to entry to this substate. If speed is 5 GT/s, the de-emphasis level must be chosen to be -3.5 dB if select_demphasis is 1b else the de-emphasis level must be -6 dB.~~ If the speed is 5 GT/s, the loopback master can choose (in an implementation-specific manner) to transmit at a de-emphasis level of -3.5 dB or -6 dB regardless of the state of the Selectable De-emphasis bit that it transmitted in the 16 consecutive TS1 Ordered Sets.

A14 Recovery.Speed

In Section 4.2.6.4.2, page 217, line 34, make the following edits:

- The Transmitter enters Electrical Idle and stays there until the Receiver Lanes have entered Electrical Idle, and then additionally remains there for at least 800 ns on a successful speed negotiation (i.e., successful_speed_negotiation = 1b) or at least 6 µs on an unsuccessful speed negotiation (i.e., successful_speed_negotiation = 0b), but stays there no longer than an additional 1 ms. The frequency of operation is permitted to be changed to the new data rate only after the Receiver Lanes have entered Electrical Idle. If the ~~new frequency of operation~~negotiated data rate is ~~the~~ 5.0 GT/s ~~data rate~~, -6 dB de-emphasis level must be selected for operation if the select_deemphasis variable is 0b and -3.5 dB de-emphasis level must be selected for operation if the select_deemphasis variable is 1b. Note that if the link is already operating at the highest data rate supported by both components, Recovery.Speed is executed but the data rate is not changed.

A15 Recovery.RcvrCfg

In Section 4.2.6.4.3, page 219, line 40, make the following edit:

... The new speed to change to in Recovery.Speed is the highest data rate that can be supported by both components on the Link. The variable successful_speed_negotiation is set to 1b. Note that if the link is already operating at the highest data rate supported by both components, Recovery.Speed is executed but the data rate is not changed.

A16 Disabled

In Section 4.2.6.9, page 232, line 8, make the following edits:

- If an EIOS was transmitted (one if the current Link speed is 2.5 GT/s and two consecutive ones if the current Link speed is greater than 2.5 GT/s) and an EIOS was received on any Lane (even while transmitting TS1 with the Disable Link bit asserted), then:
  ...

A17 Polling.Compliance

In Section 4.2.6.2.2, page 198, lines 24 and 27, make the following edits:

- If the compliance pattern data rate is not 2.5 GT/s and any TS1 Ordered Sets were transmitted in Polling.Active prior to entering Polling.Compliance, the Transmitter sends either one EIOS or two consecutive EIOSs prior to entering Electrical Idle. If the compliance pattern data rate is not 2.5 GT/s and TS1 Ordered Sets were not transmitted in Polling.Active prior to entering Polling.Compliance, the Transmitter must enter Electrical Idle without transmitting ~~the EIOS~~any EIOSs. ...

A18 Loopback.Entry

In Section 4.2.6.10.1, page 233, line 13, make the following edits:

- The loopback slave must send ~~an~~ one EIOS if the current Link speed is 2.5 GT/s or two consecutive EIOSs if the current Link speed is greater than 2.5 GT/s and then immediately go to Electrical Idle for 2 ms. …

A19 Recovery.RcvrLock

In Section 4.2.6.4.1, page 215, line 8, edit as follows:

…A device is allowed to change the ~~data rates it supports only during entry to~~supported data rates that it advertises when it enters this substate ~~(from L0, L1, or Recovery.Speed) and~~ but must not change the values either in this substate or while in Recovery.RcvrCfg substate. …

A20 Configuration.Complete

In Section 4.2.6.3.5, page 210, line 27, edit as follows:

~~A device is allowed to change the data rates it supports only during entry to this substate, and must not change the values while in this substate. A device is also allowed to change its Link width upconfigure capability advertised in Link Upconfigure Capability (Symbol 4 bit 6) in the TS2 Ordered Set prior to entry to this substate and must not change the values while in this substate.~~A device is allowed to change the supported data rates and upconfigure capability that it advertises when it enters this substate, but it must not change those values while in this substate.

A21 Flow Control Initialization State Machine Rules

In Section 3.3.1, page 139, line 8, make the following edit:

- The three InitFC1 DLLPs must be transmitted at least once every 34 µs.
  - Time spent in the Recovery or Configuration LTSSM states does not contribute to this limit.

    ...

In Section 3.3.1, page 139, line 32, make the following edit:

- The three InitFC2 DLLPs must be transmitted at least once every 34 µs.
  - Time spent in the Recovery or Configuration LTSSM states does not contribute to this limit.

    ...

A22 Clock Tolerance Compensation Rules for Transmitters

In Section 4.2.7.1, page 238, line 5, make the following edits:

- ... If the Compliance SOS bit of the Link Control 2 register is 1b, two consecutive SKP Ordered Sets must be sent (instead of one) for every scheduled SKP Ordered Set time interval while the Compliance Pattern or the Modified Compliance Pattern is in progress.

A23 Transmitter Margining

In Section 4.3.3, page 246, line 12, make the following edits:

… All 5.0 GT/s capable Transmitters must implement full-swing margining, and those 5.0 GT/s capable Transmitters supporting half-swing signaling must additionally implement half swing margining. ...

A24 Recovery.RcvrCfg

In Section 4.2.6.4.3, page 220, line 25, make the following edit:

…

- current data rate is 2.5 GT/s and either no 5.0 GT/s, or higher, data rate identifiers are set in the received eight consecutive TS1 Ordered Sets, or no 5.0 GT/s, or higher, data rate identifiers are being transmitted~~, and the current data rate is 2.5 GT/s~~ in the TS2 Ordered Sets

A25 Compliance SOS Bit

In Section 7.8.19, page 491, Table 7-25, Bit 11, make the following edit:

Bit Location	Register Description	Attributes
11	**Compliance SOS** – When set to 1b, the LTSSM is required to send SKP Ordered Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern ~~periodically in between the (modified) compliance patterns~~. …	RWS/RsvdP (see description)

A26 Polling.Compliance

In Section 4.2.6.2.2, page 200, line 9, make the following edit:

(a) Transmitter sends out the compliance pattern on all Lanes that detected a Receiver during Detect at the data rate and de-emphasis level determined above.~~.~~

A27 Completion Status

In Section 6.2.3.1, page 342, line 17, make the following edit:

The Completion Status field (when status is not Successful Completion) in the Completion header indicates that the associated Request failed (see Section 2.2.9).

A28 Error Messages

In Section 6.2.3.2, page 343, lines 12 and 15, make the following edits:

When multiple errors of the same severity are detected, the corresponding error Messages with the same Requester ID may be merged for different errors of the same severity. At least one error Message must be sent for detected errors of each severity level. Note, however, that the detection of a given error in some cases will preclude the reporting of certain errors. Refer to Section 6.2.3.2.3. Also note special rules in Section 6.2.4. regarding non-Function-specific errors in multi-Function devices.

A29 Error Pollution

In Section 6.2.3.2.3, page 345, line 28, make the following edit:

- Malformed TLP
- ACS Violation
- Unsupported Request (UR), Completer Abort (CA), or Unexpected Completion

A30 PME Pending Bit

In Section 7.8.14, page 483, Table 7-22, make the following edit:

Bit Location	Register Description	Attributes
17	**PME Pending** – This bit indicates that another PME is pending when the PME Status bit is Set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the PME Requester ID field appropriately. …	RO

A31 Transaction Layer Behavior in DL_Down States

In Section 2.9.1, page 131, line 15, make the following edit:

- (for Switch and Bridge) propagating hot reset to all ~~other~~ associated Downstream Ports

A32 Link Capabilities Register

In Section 7.8.6, pages 458, 459, 460 and 461, Table 7-14, make the following edits:

Bit Location	Register Description	Attributes
3:0	**Supported Link Speeds** … Multi-Function devices associated with an Upstream Port must report the same value in this field for all Functions.	RO
9:4	**Maximum Link Width** … Multi-Function devices associated with an Upstream Port must report the same value in this field for all Functions.	RO
11:10	**Active State Power Management (ASPM) Support** … Multi-Function devices associated with an Upstream Port must report the same value in this field for all Functions.	RO
14:12	**L0s Exit Latency** … Multi-Function devices associated with an Upstream Port must report the same value in this field for all Functions.	RO
17:15	**L1 Exit Latency** … Multi-Function devices associated with an Upstream Port must report the same value in this field for all Functions.	RO
18	**Clock Power Management** … For a multi-Function device associated with an Upstream Port, each Function indicates its capability independently. ….	RO
…	**…**	…
31:24	**Port Number** … Multi-Function devices associated with an Upstream Port must report the same value in this field for all Functions.	HwInit

A33 Virtual Channel Mechanism

In Section 2.5, page 106, line 22, make the following edit:

~~A PCI Express Endpoint or Root Complex that intends to be a Requester that can issue requests with TC label other than TC0 must implement the Virtual Channel Capability structure, even if it only supports the default VC.~~ A Device containing Functions capable of generating Requests with TC labels other than TC0 must implement suitable VC or MFVC Capability structures (as applicable), even if it only supports the default VC. Example Function types are Endpoints and Root Ports. …

A34 LCRC and Sequence Number Rules (TLP Transmitter)

In Section 3.5.2.1, page 152, line 18, make the following edit:

- Increment REPLAY_NUM. When the replay is initiated by the reception of a Nak which acknowledged some TLPs in the retry buffer, REPLAY_NUM is reset. It is then permitted (but not required) to be incremented.
  - …

A35 UpdateFC FCP

In Section 2.6.1.2, page 119, line 27, make the following edit:

- For non-infinite NPH, NPD, PH, and CPLH types, an UpdateFC FCP must be scheduled for Transmission each time the following sequence of events occurs:
  - ~~all advertised FC units for a particular type of credit are consumed by TLPs received~~when the number of available FC credits of a particular type is zero
  - one or more units of that type are made available by TLPs processed

A36 Configuration.Linkwidth.Start

In Section 4.2.6.3.1.1, page 202, line 17, edit as follows:

- The Transmitter sends TS1 Ordered Sets with selected Link numbers and sets Lane numbers to PAD (K23.7) on all the active Downstream Lanes if LinkUp is 0b or if the LTSSM is not initiating upconfiguration of the Link width. ...

In Section 4.2.6.3.1.1, page 203, line 1, edit as follows:

- If LinkUp is 1b and the LTSSM is initiating upconfiguration of the Link width, initially it transmits TS1 Ordered Sets with both the Link and Lane numbers set to PAD (K23.7) on the current set of active Lanes; the inactive Lanes it intends to activate; and those Lanes where it detected an exit from Electrical Idle since entering Recovery and has received two consecutive TS1 Ordered Sets with the Link and Lane numbers each set to PAD (K23.7). ...

In Section 4.2.6.3.1.1, page 203, line 27, edit as follows:

- Else: Optionally, if LinkUp is 0b and if crosslinks are supported, then all Downstream Lanes that detected a Receiver during Detect must first transmit 16-32 TS1s with a non PAD Link number and PAD Lane number and after this occurs if any Downstream Lanes receive two consecutive TS1 Ordered Sets with a Link number different than PAD (K23.7) and a Lane Number set to PAD, the Downstream Lanes are now designated as Upstream Lanes and a new random cross Link timeout is chosen (see $T_{crosslink}$ in Table 4-9). ...

In Section 4.2.6.3.1.2, page 205, line 25, edit as follows:

- Optionally, if LinkUp is 0b and if crosslinks are supported, then all Upstream Lanes that detected a Receiver during Detect must first transmit 16–32 TS1s with a PAD Link number and PAD Lane number and after this occurs and if any Upstream Lanes first receive two consecutive TS1 Ordered Sets with Link and Lane numbers set to PAD (K23.7), then: ...

A37 Loopback.Entry

In Section 4.2.6.10.1, page 232, line 19, add the following text:

- LinkUp = 0b (False)
- Note: The Link and Lane numbers are ignored by the Receiver.

A38 Link Error Recovery

In Section 4.2.4.6, page 185, line 28, make the following edit:

- 8b/10b decode errors must be checked and trigger a Receiver Error in specified LTSSM states (see ~~Table 4-4~~Table 4-7), which is a reported error associated with the Port (see Section 6.2). …

A39 Receiver Loopback

In Section 4.3.4.9, page 272, line 14, make the following edits:

- Error codes are defined in Section ~~4.2~~4.2.9.

A40 Ordering Rules Summary

In Section 2.4.1, page 101, make the following edits:

Replace Table 2-24: Ordering Rules Summary Table with the following table:

Table 2-24: Ordering Rules Summary Table

Row Pass Column?		Posted Request (Col 2)	Non-Posted Request		Completion (Col 5)
			Read Request (Col 3)	NPR with Data (Col 4)	
Posted Request (Row A)		a) No b) Y/N	Yes	Yes	a) Y/N b) Yes
Non-Posted Request	Read Request (Row B)	No	Y/N	Y/N	Y/N
	NPR with Data (Row C)	No	Y/N	Y/N	Y/N
Completion (Row D)		a) No b) Y/N	Yes	Yes	a) Y/N b) No

After Table 2-24, add the following text:

Explanation of the row and column headers in Table 2-24:

A **Posted Request** is a Memory Write Request or a Message Request.

A **Read Request** is a Configuration Read Request, an I/O Read Request, or a Memory Read Request.

An **NPR** (Non-Posted Request) **with Data** is a Configuration Write Request or an I/O Write Request.

A **Non-Posted Request** is a Read Request or an NPR with Data.

Make the following edits starting at page 101, line 1:

Explanation of the entries in Table 2-24:

~~A2 a~~	~~A Memory Write or Message Request with the Relaxed Ordering Attribute bit clear (0b) must not pass any other Memory Write or Message Request.~~
A2a	A Posted Request must not pass another Posted Request unless A2b applies.
~~A2 b~~	~~A Memory Write or Message Request with the Relaxed Ordering Attribute bit set (1b) is permitted to pass any other Memory Write or Message Request.~~
A2b	A Posted Request with RO[footnote] Set is permitted to pass another Posted Request.
[footnote]	In this section, "RO" is an abbreviation for the Relaxed Ordering Attribute field.
~~A3, A4~~	~~A Memory Write or Message Request must be allowed to pass Read Requests and I/O or Configuration Write Requests to avoid deadlocks.~~
A3, A4	A Posted Request must be able to pass Non-Posted Requests to avoid deadlocks.
~~A5, A6 a~~	~~Endpoints, Switches, and Root Complex may allow Memory Write and Message Requests to pass Completions or be blocked by Completions.~~
A5a	A Posted Request is permitted to pass a Completion, but is not required to be able to pass Completions unless A5b applies.
~~A5, A6 b~~	~~PCI Express to PCI Bridges and PCI Express to PCI-X Bridges, when operating the PCI/PCI-X bus segment in conventional mode, must allow Memory Write and Message Requests to pass Completions traveling in the PCI Express to PCI direction (Primary side of Bridge to Secondary side of Bridge) to avoid deadlock.~~
A5b	Inside a PCI Express to PCI/PCI-X Bridge whose PCI/PCI-X bus segment is operating in conventional PCI mode, for transactions traveling in the PCI Express to PCI direction, a Posted Request must be able to pass Completions to avoid deadlock.
~~B2, C2~~	~~These Requests cannot pass a Memory Write or Message Request. This preserves strong write ordering required to support Producer/Consumer usage model.~~
B2	A Read Request must not pass a Posted Request.
C2	An NPR with Data must not pass a Posted Request.
~~B3, B4, C3, C4~~	~~Read Requests and I/O or Configuration Write Requests are permitted to be blocked by or to pass other Read Requests and I/O or Configuration Write Requests.~~
B3, B4, C3, C4	A Non-Posted Request is permitted to pass another Non-Posted Request.
~~B5, B6, C5, C6~~	~~These Requests are permitted to be blocked by or to pass Completions.~~
B5, C5	A Non-Posted Request is permitted to pass a Completion.
~~D2 a~~	~~If the Relaxed Ordering attribute bit is not set, then a Read Completion cannot pass a previously enqueued Memory Write or Message Request.~~
D2a	A Completion must not pass a Posted Request unless D2b applies.
~~D2 b~~	~~If the Relaxed Ordering attribute bit is set, then a Read Completion is permitted to pass a previously enqueued Memory Write or Message Request.~~

D2b An I/O or Configuration Write Completion[footnote] is permitted to pass a Posted Request. A Completion with RO Set is permitted to pass a Posted Request.

[footnote] Note: Not all components can distinguish I/O and Configuration Write Completions from other Completions. In particular, routing elements not serving as the associated Requester or Completer generally cannot make this distinction. A component must not apply this rule for I/O and Configuration Write Completions unless it is certain of the associated Request type.

~~D3, D4, E3, E4 Completions must be allowed to pass Read and I/O or Configuration Write Requests to avoid deadlocks.~~

D3, D4 A Completion must be able to pass Non-Posted Requests to avoid deadlocks.

~~D5 a Read Completions associated with different Read Requests are allowed to be blocked by or to pass each other.~~

D5a Completions with different Transaction IDs are permitted to pass each other.

~~D5 b Read Completions for one Request (will have the same Transaction ID) must return in address order.~~

D5b Completions with the same Transaction ID must not pass each other. This ensures that multiple Completions associated with a single Memory Read Request will remain in ascending address order.

~~D6 Read Completions are permitted to be blocked by or to pass I/O or Configuration Write Completions.~~

~~E2 I/O or Configuration Write Completions are permitted to be blocked by or to pass Memory Write and Message Requests. Such Transactions are actually moving in the opposite direction and, therefore, have no ordering relationship.~~

~~E5, E6 I/O or Configuration Write Completions are permitted to be blocked by or to pass Read Completions and other I/O or Configuration Write Completions.~~

A41 Configuration.Lanenum.Accept Substate

In Section 4.2.6.3.3.1, page 208, line 20, make the following edits:

- If two consecutive TS1 Ordered Sets are received with non-PAD Link and non-PAD Lane numbers that match all the non-PAD Link and non-PAD Lane numbers (or reversed Lane numbers if Lane reversal is optionally supported) that are being transmitted in Downstream Lane TS1 Ordered Sets, the next state is Configuration.Complete.
  - The Link Bandwidth Management Status and Link Autonomous Bandwidth Status bits of the Link Status register must be updated as follows on a Link bandwidth change if the current transition to Configuration state was from the Recovery state:

    ~~(a) If the Link bandwidth was reduced and either the Autonomous Change bit (Symbol 4 bit 6) in two consecutive received TS1 Ordered Sets is 0b or the bandwidth change was initiated by the Upstream component due to reliability issues, the Link Bandwidth Management Status bit is set to 1b~~

    (a) If the bandwidth change was initiated by the Upstream component due to reliability issues, the Link Bandwidth Management Status bit is set to 1b.

(b) Else if the bandwidth change was not initiated by the Upstream component and the Autonomous Change bit (Symbol 4 bit 6) in two consecutive received TS1 Ordered Sets is 0b, the Link Bandwidth Management Status bit is set to 1b.

(~~b~~c) e~~E~~lse the Link Autonomous Bandwidth Status bit is set to 1b.

A42 Polling.Active Substate

In Section 4.2.6.2.1, page 196, lines 12-25, make the following edits:

- Next state is Polling.Configuration after at least 1024 TS1 Ordered Sets were transmitted, and all Lanes that detected a Receiver during Detect receive eight consecutive ~~TS1 or TS2 Ordered Sets~~ training sequences (or their complement) ~~with both of~~ satisfying any of the following conditions:
  - ~~Lane and Link numbers set to PAD (K23.7)~~
  - ~~Compliance Receive bit (bit 4 of Symbol 5) is 0b in the received TS1's, if any, or Loopback bit (bit 2 of Symbol 5) is 1b in the received TS1 or TS2 Ordered Sets.~~
  - TS1 with Lane and Link numbers set to PAD (K23.7) and the Compliance Receive bit (bit 4 of Symbol 5) is 0b.
  - TS1 with Lane and Link numbers set to PAD (K23.7) and the Loopback bit (bit 2 of Symbol 5) is 1b.
  - TS2 with Lane and Link numbers set to PAD (K23.7).
- Otherwise, after a 24 ms timeout the next state is:
  - Polling.Configuration if,
    i. Any Lane, which detected a Receiver during Detect, received eight consecutive ~~TS1 or TS2 Ordered Sets~~ training sequences (or their complement) satisfying any of the following conditions:

       ~~1. the Lane and Link numbers set to PAD (K23.7),~~

       ~~2. the Compliance Receive bit (bit 4 of Symbol 5) is 0b or Loopback bit (bit 2 of Symbol 5) is 1b.~~

       1. TS1 with Lane and Link numbers set to PAD (K23.7) and the Compliance Receive bit (bit 4 of Symbol 5) is 0b.
       2. TS1 with Lane and Link numbers set to PAD (K23.7) and the Loopback bit (bit 2 of Symbol 5) is 1b.
       3. TS2 with Lane and Link numbers set to PAD (K23.7).

       and a minimum of 1024 TS1s are transmitted after receiving one TS1.

A43 Recovery from L1

In Section 4.2.6.4.1, page 216, lines 12-26, make the following edits:

- Else the next state is Recovery.Speed if the speed of operation has not changed to a mutually negotiated data rate since entering Recovery from L0 or L1 (i.e., changed_speed_recovery = 0b) and the current speed of operation is greater than 2.5 GT/s. The new data rate to operate after leaving Recovery.Speed will be at 2.5 GT/s.
  Note: This indicates that the Link was unable to operate at the current data rate (greater than 2.5 GT/s) and the Link will operate at the 2.5 GT/s data rate.

- Else the next state is Recovery.Speed if the operating speed has been changed to a mutually negotiated data rate since entering Recovery from L0 or L1 (changed_speed_recovery = 1b; i.e., the arc to this substate has been taken from Recovery.Speed). The new data rate to operate after leaving Recovery.Speed is reverted back to the speed it was when Recovery was entered from L0 or L1.

  Note: This indicates that the Link was unable to operate at the new negotiated data rate and will revert back to the old data rate with which it entered Recovery from L0 or L1.

In Section 4.2.6.4.2, page 218, line 26, make the following edit:

- Else if this substate is being entered for a second time since entering Recovery from L0 or L1 (i.e., changed_speed_recovery = 1b), the new data rate will be the data rate at which the LTSSM entered Recovery from L0 or L1. The changed_speed_recovery variable will be reset to 0b.

In Section 4.2.6.4.3, page 220, lines 34 and 38, make the following edits:

- ❑ Next state is Recovery.Speed if the speed of operation has changed to a mutually negotiated data rate since entering Recovery from L0 or L1 (i.e., changed_speed_recovery = 1b) and an EIOS has been detected or an Electrical Idle condition has been inferred/detected on any of the configured Lanes and no configured Lane received a TS2 Ordered Set since entering this substate (Recovery.RcvrCfg). The new data rate to operate after leaving Recovery.Speed will be reverted back to the speed of operation during entry to Recovery from L0 or L1.

  Note: As described in Section 4.2.4.3, an Electrical Idle condition may be inferred if a TS1 or TS2 Ordered Set has not been received in a 1280 UI time interval.

- ❑ Next state is Recovery.Speed if the speed of operation has not changed to a mutually negotiated data rate since entering Recovery from L0 or L1 (i.e., changed_speed_recovery = 0b) and the current speed of operation is greater than 2.5 GT/s and an EIOS has been detected or an Electrical Idle condition has been detected/inferred on any of the configured Lanes and no configured Lane received a TS2 Ordered Set since entering this substate (Recovery.RcvrCfg). The new data rate to operate after leaving Recovery.Speed will be 2.5 GT/s.

  Note: As described in Section 4.2.4.3, an Electrical Idle condition may be inferred if a TS1 or TS2 Ordered Set has not been received in a 1280 UI time interval.

A44 Compliance Pattern

In Section 4.2.8, page 239, line 10, make the following edits:

After the eight Symbols are sent, the delay Symbols are advanced to the next Lane, until the delay Symbols have been sent on all eight lanes. Then the delay Symbols cycle back to Lane 0, and the process is repeated. It is permitted to advance the delay sequence across all eight lanes, regardless of the number of lanes detected or supported. An illustration of this process is shown below:

In Section 4.2.9, page 240, line 8, make the following edits:

After the 16 Symbols are sent, the delay Symbols are advanced to the next Lane, until the delay Symbols have been sent on all eight lanes. Then the delay Symbols cycle back to Lane 0, and the process is repeated. It is permitted to advance the delay sequence across all eight lanes, regardless of the number of lanes detected or supported. Note: A x1 device, or a xN device operating a Link in x1 mode, in permitted to include the Delay symbols with the Modified Compliance Pattern.

A45 Refclk Compliance Parameters for Common Refclk Rx Architecture

In Section 4.3.7.2.3, page 288, Table 4-16, make the following edits to the notes:

Notes:

1. $T_{REFCLK\text{-}HF\text{-}RMS}$ is measured at the far end of the test circuit illustrated in Figure 4-52 after the ~~following filter functions have been applied.~~filter function defined in Table 4-14 for Common Refclk Rx for >1.5 MHz jitter components has been applied.
2. $T_{REFCLK\text{-}SSC\text{-}RES}$ and $T_{REFCLK\text{-}LF\text{-}RMS}$ are measured after ~~applying~~ the ~~following filter functions.~~filter function defined in Table 4-14 for Common Refclk Rx for >1.5 MHz jitter components has been applied.
3. Defined for a worst case SSC modulation profile such as Lexmark.

A46 Refclk Compliance Parameters for Data Clocked Rx Architecture

In Section 4.3.7.2.5, page 290, Table 4-18, make the following edits to the notes:

Notes:

1. $T_{REFCLK\text{-}HF\text{-}RMS}$ is measured at the far end of the test circuit illustrated in Figure 4-52 after the ~~following filter functions have been applied.~~filter function defined in Table 4-14 for Data Clocked Rx for >1.5 MHz jitter components has been applied.
2. $T_{REFCLK\text{-}SSC\text{-}FULL}$ and $T_{REFCLK\text{-}LF\text{-}RMS}$ are measured after ~~applying the following filter functions.~~the filter function defined in Table 4-14 for Data Clocked Rx for <1.5 MHz jitter components has been applied.
3. Defined for a worst case SSC modulation profile such as Lexmark.

A47 Transmitter Specification

In Section 4.3.3.5, page 249, Table 4-9, make the following edits:

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak Output Voltage	0 (min) 20 (max)	0 (min) 20 (max)	mV	$V_{TX-IDLE-DIFFp}$ = $\|V_{TX-Idle-D+} - V_{Tx-Idle-D-}\| \leq 20$ mV. Voltage must be ~~high~~ band pass filtered to remove any DC component and HF noise.~~– Filter characteristics TBD.~~ The bandpass is constructed from two first-order filters, the high pass and low pass 3 dB bandwidths are 10 kHz and 1.25 GHz, respectively.

A48 Transmitter Specification

In Section 4.3.3.5, page 249, Table 4-9, make the following edits:

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	Not specified	0 (min) 5 (max)	mV	$V_{TX-IDLE-DIFF-DC}$ = $\|V_{TX-Idle-D+} - V_{Tx-Idle-D-}\| \leq 5$ mV. Voltage must be low pass filtered to remove any AC component.~~ Filter characteristics complementary to above.~~ The low pass filter is first-order with a 3 dB bandwidth of 10 kHz.

A49 Component Interfaces

In Section 4.3.1.2, page 242, line 10, make the following edit:

PCI express components from different ~~sources~~manufacturers must interoperate reliably together. At the electrical level, this is achieved by specifying a set of parameters and the interfaces at which those parameters must be met.

A50 ACS Translation Blocking

In Section 7.16.3, page 549, Table 7-65, make the following edit:

Bit Location	Register Description	Attributes
6	**ACS Direct Translated P2P Enable (T)** – When Set, overrides the ACS P2P Request Redirect and ACS P2P Egress Control mechanisms with peer-to-peer Memory Requests whose Address Translation (AT) field indicates a Translated address (see Section 6.12.3). This bit is ignored if ACS Translation Blocking (B) is 1b. Default value of this bit is 0b. Must be hardwired to 0b if the ACS Direct Translated P2P functionality is not implemented.	RW

In Section 6.12.1.1, page 404, line 27, make the following edit:

- ACS Translation Blocking: must be implemented.

  When enabled, the Downstream Port checks the Address Translation (AT) field of each Upstream Memory Request received by the Port. If the AT field is not the default value, this is a reported error (ACS Violation) associated with the Receiving Port (see Section 6.12.4). This error must take precedence over ACS Upstream Forwarding and any applicable ACS P2P control mechanisms.

  Completions are never affected by ACS Translation Blocking.

A51 Completion Handling Rules

In Section 2.3.2, page 98, line 6 add the following text:

- If a received Completion is not malformed and matches the Transaction ID of an outstanding Request, but in some other way does not match the corresponding Request, it is permitted for the receiver to handle the Completion as an Unexpected Completion
- When an Ingress Port of a Switch receives a Completion which cannot be forwarded, that Ingress Port must handle the Completion as an "Unexpected Completion." This includes Completions that target:
  - a non-existent Function in the Device associated with the Upstream Port,
  - a non-existent Device on the Bus associated with the Upstream Port,
  - a non-existent Device or Function on the internal switching fabric, or
  - a Bus Number within the Upstream Port's Bus Number aperture but not claimed by any Downstream Port.
- Receipt of an Unexpected Completion is an error and must be handled according to the following rules:
  - The agent receiving an Unexpected Completion must discard the Completion.
  - An Unexpected Completion is a reported error associated with the Receiving Port (see Section 6.2)

    Note: Unexpected Completions are assumed to occur mainly due to Switch misrouting of the Completion. The Requester of the Request may not receive a Completion for its Request in this case, and the Requester's Completion Timeout mechanism (see Section 2.8) will terminate the Request.

In Section 6.2.4, page 350, line 10, add the following text:

- These Transaction Layer errors:
  - ECRC Fail
  - UR, when caused by no Function claiming a TLP
  - Receiver Overflow
  - Flow Control Protocol Error
  - Malformed TLP
  - Unexpected Completion, when caused by no Function claiming a Completion
  - Unexpected Completion, when caused by a Completion that cannot be forwarded by a Switch, and the Ingress Port is a Switch Upstream Port associated with a multi-Function device

A52 ID Based Routing Rules

In Section 2.2.4.2, page 58, line 4, make the following edits:

ID routing is used with Configuration Requests, ~~optionally~~ with ID Routed Messages~~Vendor_Defined Messages (see Section 2.2.8.6)~~, and with Completions. This specification defines Vendor_Defined Messages that are ID Routed (Section 2.2.8.6). Other specifications define additional ID Routed Messages.[footnote]

[footnote] Currently, this includes the *ATS Specification*.

A53 PCI Express Capability Structure

In Section 7.8, page 440, line 26, make the following edit:

For Functions that do not implement the Slot Capabilities, Slot Status, and Slot Control registers, these spaces must be hardwired to 0b, with the exception of the Presence Detect State bit in the Slot Status register of Downstream Ports, which must be hardwired to 1b (see Section 7.8.11). Slot Capabilities 2, Slot Status 2, and Slot Control 2 registers are required for Switch Downstream and Root Ports if a slot is implemented on the Port and the Function implements capabilities requiring those registers.

A54 ACS Peer-to-Peer Control Interactions

In Section 6.12.3, page 409, line 5, add the following text:

Specifically, the applicable Egress Control Vector bit, along with the ACS P2P Egress Control Enable bit (E) and the ACS P2P Request Redirect Enable bit (R), determine how the Request is handled. It must be noted that atomicity of accesses cannot be guaranteed if ACS peer-to-peer Request Redirect targets a legacy device location that can be the target of a locked access. Refer to Section 7.16 for descriptions of these control bits. Table 6-8 specifies the interactions.

A55 Enhanced Capability Header

In various sections (96 occurrences):

Replace Enhanced Capability Header with Extended Capability Header.

A56 $D3_{hot}$ State

In Section 5.3.1.4.1, page 302, add the following implementation note after line 14:

IMPLEMENTATION NOTE

Multi-Function Device Issues with Soft Reset

With multi-Function devices (MFDs), certain control settings affecting overall device behavior are determined either by the collective settings in all Functions or strictly off the settings in Function 0. Here are some key examples:

- With non-ARI MFDs, certain controls in the Device Control register and Link Control register operate off the collective settings of all Functions. See Section 7.8.4 and Section 7.8.7.
- With ARI Devices, certain controls in the Device Control register and Link Control register operate strictly off the settings in Function 0. See Section 7.8.4 and Section 7.8.7.
- With all MFDs, certain controls in the Link Control 2 register operate strictly off the settings in Function 0. See Section 7.8.19.

Performing a soft reset on any Function (especially Function 0) may disrupt the proper operation of other active Functions in the MFD. Since some Operating Systems transition a given Function between $D3_{hot}$ and D0 with the expectation that other Functions will not be impacted, it is strongly recommended that every Function in an MFD be implemented with the No_Soft_Reset bit Set in the Power Management Status/Control register. This way, transitioning a given Function from $D3_{hot}$ to D0 will not disrupt the proper operation of other active Functions.

It is also strongly recommended that every Endpoint Function in an MFD implement Function Level Reset (FLR). FLR can be used to reset an individual Endpoint Function without impacting the settings that might affect other Functions, particularly if those Functions are active. Because of FLR's quiescing, error recovery, and cleansing for reuse properties, FLR is also recommended for single-Function Endpoint devices.

A57 Data Scrambling

In Section 4.2.3, page 175, line 9, make the following changes:

- All data Symbols (D codes) except those within a Training Sequence Ordered Sets (e.g., TS1, TS2), ~~and~~ the Compliance Pattern (see Section 4.2.8) and the Modified Compliance Pattern (see Section 4.2.9) are scrambled.

A58 Multicast ECN

In the *Multicast ECN*, page 7, line 30 make following edit:

If (MC_Overlay_Size ≤ 6 ~~== 0~~)

A59 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 9, Section 7.8.16, bit 10, make the following edit:

~~Components~~ Functions that do not implement LTR are permitted to hardwire this bit to 0b.

A60 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 4, line 11, make the following edit:

When the LTR Mechanism Enable bit is cleared, if a device's ~~had previously~~ most recently sent LTR Message (since the last DL_Down to DL_UP transition) reported Latency Tolerance values with any ~~one or both latency fields with the~~ Requirement bit set, then it must send a new LTR Message with ~~both~~ all the Requirement bits clear.

A61 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 4, line 26, make the following edit:

It is recommended that Endpoints transmit an LTR Message Upstream shortly after the LTR capability is enabled~~, and ideally before issuing any other Request TLPs~~.

A62 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 5, line 12, make the following edit:

- When any Downstream Port reports a field with the Requirement bit set to 1 and a LatencyValue of all 0's (regardless of the LatencyScale value), the Message sent Upstream must report a LatencyScale of 000b and a LatencyValue of all 0's.

A63 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 9, Section 7.8.16, bit 10, make the following edit:

Components that do not implement the LTR mechanism are permitted to hardwire this bit to 0b.

In the *Latency Tolerance Reporting ECN*, page 10, Line 3, make the following edit:

… and is required if the component supports the LTR mechanism. It is not applicable to Root Ports or Downstream Ports in a Switch.

In the *Latency Tolerance Reporting ECN*, page 10, Line 6, make the following edit:

… component that implements the LTR mechanism, this Capability structure must be implemented only in Function 0, and must control the component's Link behavior on behalf of all the Functions of the device.

B1 Polling

In Section 4.2.5.2, page 189, line 12, make the following edit:

… This portion of the Polling.Compliance state is logically entered by at least one component asserting the Compliance Receive bit (bit 4 in Symbol 5 of TS1) while not asserting the Loopback bit (bit 2 in Symbol 5 of TS1) upon entering Polling.Active. The ability to set the Compliance Receive bit is implementation specific. A provision for changing speeds to the highest common transmitted and received Link speed (Symbol 4 of TS1) is also included to make this behavior scalable to various Link speeds.

B2 Loopback.Entry

In Section 4.2.6.10.1, page 234, line 10, make the following edits:

- The next state for the loopback slave is Loopback.Active.
  - Note: The loopback master is permitted to set the ~~The~~ Compliance Receive bit (bit 4 of Symbol 5) in the TS1 Ordered Set ~~is set~~ to help force a transition in to Loopback.Active for both the loopback master and the loopback slave in the case that successful Symbol lock cannot occur. Once the loopback master asserts this bit in the TS1 Ordered Sets it transmits, it must not deassert that bit while in the Loopback state. This usage model is useful for test and validation purposes. The ability to set the Compliance Receive bit is implementation specific.

B3 Configuration

In Section 4.2.6.3.1.1, page 202, line 26, make the following edit:

- Note: On transition to this substate from Polling, any Lane that detected a Receiver during Detect is considered an active Lane.
- Note: On transition to this substate from Recovery, any Lane that is part of the configured Link the previous time through Configuration.Complete is considered an active Lane.

In Section 4.2.6.3.1.2, page 204, line 30, make the following edit:

- Note: On transition to this substate from Polling, any Lane that detected a Receiver during Detect is considered an active Lane.
- Note: On transition to this substate from Recovery, any Lane that is part of the configured Link the previous time through Configuration.Complete is considered an active Lane.

B4 Selectable De-emphasis

In Section 7.8.19, page 489, Table 7-25, bit 6, edit as follows:

Bit Location	Register Description	Attributes
6	**Selectable De-emphasis** – When the Link is operating at 5.0 GT/s speed, this bit ~~selects the level of de-emphasis for an Upstream component~~is used to control the transmit de-emphasis of the link in specific situations. See Section 4.2.6 for detailed usage information. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is not applicable and reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches.	HwInit

B5 Recovery.RcvrLock

In Section 4.2.6.4.1, page 215, line 19, edit as follows:

…~~An Upstream component must record the Selectable De-emphasis bit (Symbol 4 bit 6) in the Received TS1 Ordered Set in a Downstream_de-emphasis_setting variable on exit from this state.~~ If the upstream component intends to use the downstream component's de-emphasis information in Recovery.RcvrCfg, then it must record the value of the Selectable De-emphasis bit received in this state.

B6 Configuration.Linkwidth.Accept

In Section 4.2.6.3.2.1, page 206, line 14, make the following edit:

- The assigned non-PAD Lane numbers must range from 0 to n-1, be assigned sequentially to the same grouping of Lanes that are receiving the same Link number~~ Lane numbers~~, and Downstream Lanes which are not receiving TS1 Ordered Sets must not disrupt the initial sequential numbering of the widest possible Link. …

B7 Completion Status

In Section 6.2.3.1, page 342, line 23, edit as follows:

The Completion Status field in the Completion header indicates that the associated Request failed (see Section 2.2.9). This is one method of error reporting which enables the Requester to associate an error with a specific Request. In other words, since Non-Posted Requests are not considered complete until after the Completion returns, the Completion Status field gives the Requester an opportunity to "fix" the problem at some higher level protocol (outside the scope of this specification). For example, if a Read is issued to prefetchable Memory Space and the Completion returns with an Unsupported Request Completion Status, ~~perhaps due to a temporary condition, the Requester may choose to reissue the Read Request without side effects~~the Requester would not be in violation of this specification if it chose to reissue the Read Request. Note that from a PCI Express point of view, the reissued Read Request is a distinct Request, and there is no relationship (on PCI Express) between the initial Request and the reissued Request.

B8 Transmitter De-emphasis

In Section 4.3.3.9, page 255, Figure 4-30, make the following edit:

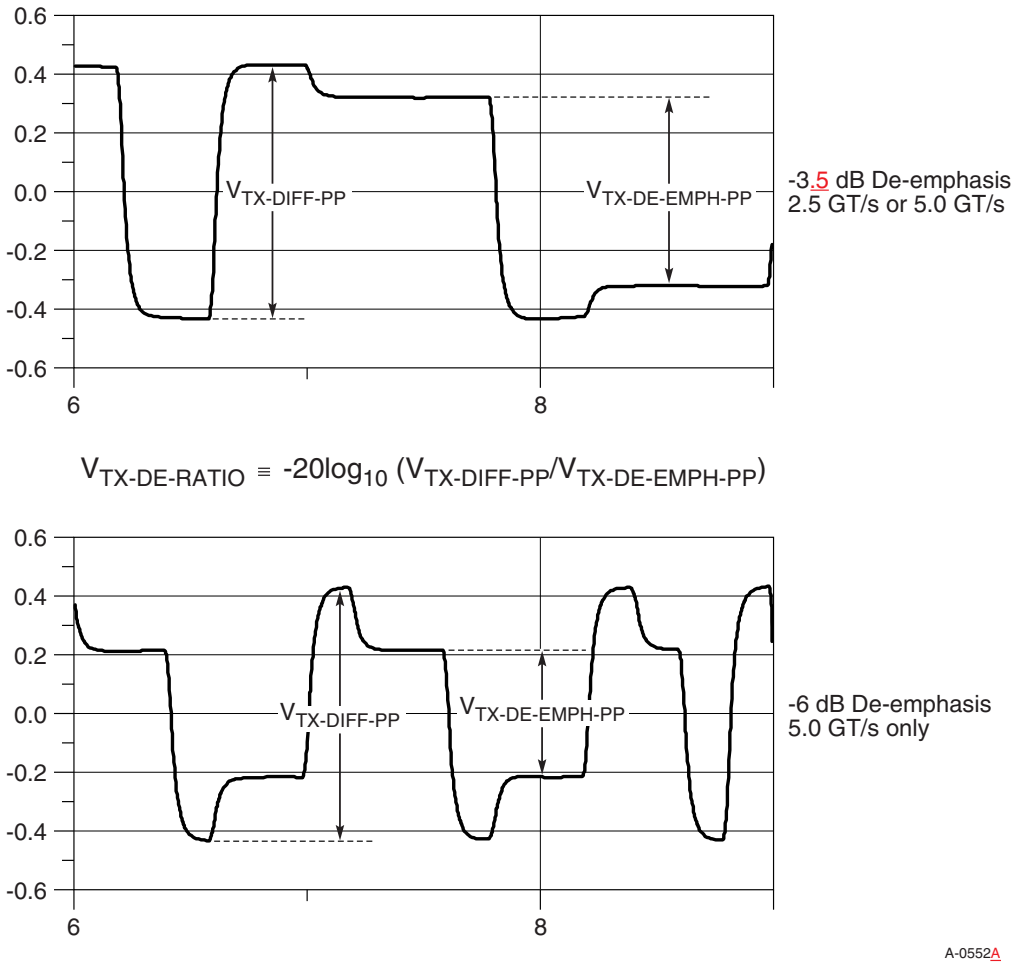

Figure 4-30: Full Swing Tx Parameters Showing De-emphasis

B9 Virtual Channel Mechanism

In Section 2.5, page 106, line 13, make the following edit:

Support for TCs and VCs beyond default TC0/VC0 pair is optional. The association of TC0 with VC0 is fixed, i.e., "hardwired," and must be supported by all components. Therefore the baseline TC/VC setup does not require any VC-specific hardware or software configuration. In order to ensure interoperability, components that do not implement the optional Virtual Channel Capability structure or Multi-Function Virtual Capability structure must obey the following rules:

…

B10 VC Arbitration

In Section 6.3.3.2, page 366, line 21, make the following edit:

This specification defines a default VC prioritization via the VC Identification (VC ID) assignment, i.e., the VC IDs are arranged in ascending order of relative priority in the Virtual Channel Capability structure or Multi-Function Virtual Channel Capability structure.

B11 Active State Link PM

In Section 5.4.1, page 315, line 18, make the edits indicated below:

All ~~components other than Root Complex Integrated Endpoints~~ ports not associated with an Internal Root Complex Link or system Egress Port are required to support the minimum requirements defined herein for Active State Link PM.

B12 Configuration Request Routing Rules

In Section 7.3.3, page 423, line 1, make the following edit:

- ❑ If Configuration Request Type is 1, apply the following tests, in sequence, to the Bus Number and Device Number fields: ...

B13 Non-Pad Link Numbers

In Section 4.2.6.3.1.2, page 205, lines 13 and 15, make the following edits:

- Note: If the LTTSM is initiating upconfiguration of the Link width, it waits until it receives two consecutive TS1 Ordered Sets with a non-PAD ~~(K23.7)~~ Link Number and a PAD (K23.7) Lane number on all the inactive Lanes it wants to activate, or, 1 ms after entry to this substate, it receives two consecutive TS1 Ordered Sets on any Lane with a non-PAD ~~(K23.7)~~ Link number and PAD (K23.7) Lane number, whichever occurs earlier, before transmitting TS1 Ordered Sets with selected Link number and Lane number set to PAD (K23.7).

B14 Recovery.Speed

In Section 4.2.6.4.2, page 218, line 41, make the following edit:

- On a Link bandwidth change, if successful_speed_negotiation is set to 1b and the Autonomous Change bit (bit 6 of Symbol 4) in the eight consecutive TS2 Ordered Sets in Recovery.RcvrCfg is set to 1b or the speed change was initiated by the Upstream component for autonomous reasons (non-reliability and not due to the setting of the Link Retrain bit), the Link Autonomous Bandwidth Status bit of the Link Status register is set to 1b for an Upstream component.

B15 Receiver Tolerancing at 5.0 GT/s

In Section 4.3.4.2, page 262, Table 4-10, make the following edits:

Table 4-10: 5.0 GT/s Tolerancing Limits for Common Refclk Rx Architecture

Parameter	Description	Min	Max	Units	Notes
UI	Unit interval without including of SSC	200.06	199.94	ps	Over 10^6 UI
$T_{RX-HF-RMS}$	1.5 – 100 MHz RMS jitter		3.4	ps RMS	Spectrally flat
$T_{RX-HF-DJ-DD}$	Max Dj impinging on Rx under test		88	ps	2,4
$T_{RX-SSC-RES}$	33 kHz Refclk residual	--	75	ps	
$T_{RX-LF-RMS}$	< 1.5 MHz RMS jitter	--	4.2	ps RMS	Spectrally flat
$T_{RX-MIN-PULSE}$	Minimum single pulse applied at Rx	120		ps	2
$V_{RX-MIN-MAX-RATIO}$	Min/max pulse voltage ratio seen over an time interval of 2 UI.	--	5		2
V_{RX-EYE}	Receive eye voltage opening	120		mVPP diff	1,3
$V_{RX-CM-CH-SRC}$	Common mode noise from Rx	--	300	mVPP	2

B16 Receiver Loopback

In Section 4.3.4.9, page 272, line 2, make the following edits:

Receivers, whether operating at 2.5 GT/s or 5.0 GT/s, must implement a loopback error count (described in Section 4.2.6.2.2) when placed in the appropriate ~~test~~compliance mode. …

B17 Receiver Loopback

In Section 4.3.4.9, page 272, line 7, make the following edits:

Some ~~D~~details of the error check and loopback circuits are implementation dependent and are not covered in this specification. However, the basic requirements are listed below:

B18 Electrical Idle

In Section 4.3.5.5, page 274, line 5, make the following edits:

Before a Transmitter enters Electrical Idle, is must always send the required number of EIOSs defined in Section 4.2.4.1 except for the LTSSM substates explicitly exempted from ~~being a~~this requirement. …

B19 Active State Power Management (ASPM)

In Section 5.4.1, page 316, line 23, make the following edit:

An Upstream Port ~~with~~of a multi-Function device may be programmed with different values in their respective Active_PM_En registers of each Function. …

In Section 5.4.1.1.1, page 317, line 28, make the following edit:

Definition of Idle

… An Upstream Port ~~with~~of a multi-Function device is considered idle only when all of its Functions are idle.

B20 Root Control Register

In Section 7.8.12, page 481, Table 7-20, make the following edit:

Bit Location	Register Description	Attributes
3	**PME Interrupt Enable** – When Set, this bit enables PME interrupt generation upon receipt of a PME Message as reflected in the PME Status bit (see Table 7-22). A PME interrupt is also generated if the PME Status ~~register~~ bit is Set when this bit is changed from Clear to Set (see Section 6.1.5). …	RW

B21 Function Arbitration Table

In Section 7.18.10, page 564, line 18, make the following edit:

The Function Arbitration Table Entry Size field in the Port VC Capability ~~register~~Register 1 determines the table entry size. The length of the table is determined by the Function Arbitration Select field as shown in Table 7-76.

B22 Electrical Idle

In Section 4.3.5.5, page 274, lines 5 and 9, make the following edits:

Before a Transmitter enters Electrical Idle, is must always send the required number of EIOSs defined in ~~Section 4.2.4.1~~Section 4.2.4.2 except for the LTSSM substates explicitly exempted from being a requirement. After sending the last Symbol of the last of the required number of EIOSs, the Transmitter must be in a valid Electrical Idle state within the time as specified by $T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$ in Table 4-9.

The successful reception of an EIOS (see ~~Section 4.2.4.1~~Section 4.2.4.2) occurs upon the receipt of two out of the three K28.3 (IDL) Symbols in the transmitted EIOS, irrespective of the current Link speed. It must be noted that in substates (e.g., Loopback.Active for a loopback slave) where multiple consecutive EIOSs are expected, the Receiver must receive the appropriate number of EIOS sequences comprising of COM, IDL, IDL, IDL.

B23 VC Arbitration Select

In Section 7.11.4, page 516, Table 7-42, Bits 3:1, edit as follows:

Bit Location	Register Description	Attributes
3:1	**VC Arbitration Select** – Used for software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the Port VC Capability Register 2. This field is valid for all Functions. The permissible value of this field is the number corresponding to one of the asserted bits in the VC Arbitration Capability field. …	RW

In Section 7.18.4, page 557, Table 7-71, Bits 3:1, edit as follows:

Bit Location	Register Description	Attributes
3:1	**VC Arbitration Select** – Used for software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the Port VC Capability Register 2. The permissible value of this field is the number corresponding to one of the asserted bits in the VC Arbitration Capability field. …	RW

B24 Device Control Register

In Section 7.8.4, page 449, Figure 7-13, make the following edit:

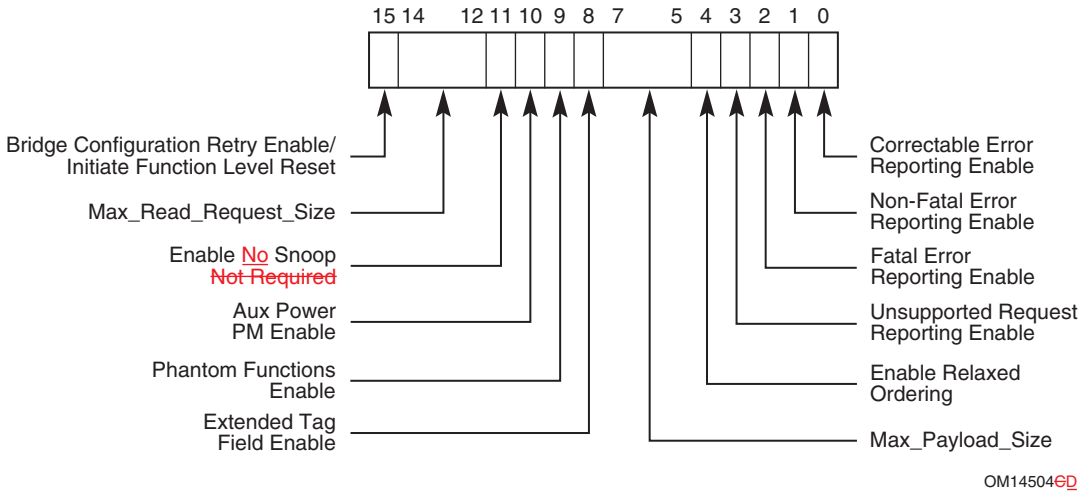

Figure 7-13: Device Control Register

B25 Link Control 2 Register

In Section 7.8.19, page 490, Table 7-25, make the following edits:

Bit Location	Register Description	Attributes
9:7	**Transmit Margin** – This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b-111b As defined in Section 4.3.3.3, not all encodings are required to be implemented. ~~001b 800-1200 mV for full swing and 400-700 mV for half-swing~~ ~~010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full swing and 100-200 mV for half swing~~ ~~n - 111b reserved~~ For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of	RWS/RsvdP (see description)

Bit Location	Register Description	Attributes
	that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.	

B26 Power Management Statement of Requirements

In Section 5.1.1, page 294, line 16, make the following edit:

All PCI Express Functions, with the exception of Functions in a Root Complex, are required to meet or exceed the minimum requirements defined by the PCI-PM software compatible PCI Express-PM features. Root Complexes are required to participate in Link power management DLLP protocols initiated by a Downstream device. For further details, refer to Section 5.3.2.

ASPM is a required feature ~~(L0s entry at minimum) for Root Ports, Upstream Ports, and Switch Downstream Ports~~. Refer to Section 5.4.1 for more information on ASPM.

B27 Receiver Specifications

In Section 4.3.4.4, page 266, Table 4-12, make the following edit:

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
Z_{RX-DC}	Receiver DC ~~common mode~~single ended impedance	40 (min) 60 (max)	40 (min) 60 (max)	Ω	DC impedance limits are needed to guarantee Receiver detect. See Note 5.

B28 Receiver Specifications

In Section 4.3.4.4, page 267, Table 4-12, make the following edit to the Notes:

Notes:

5. The Rx DC ~~Common Mode Impedance~~single ended impedence must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the Rx Common Mode Impedance (constrained by RL_{RX-CM} to 50 Ω ±20%) must be within the specified range by the time Detect is entered.
6. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V_{-CMDC}|}.

B29 Evaluation Delay

In Section 4.2.6.3.1.2, page 205, lines 21 and 40, make the following edits:

- Note: It is recommended that any possible multi-Lane Link that received an error in a TS1 Ordered Set on a subset of the received Lanes; delay the evaluation listed above by an additional two, or more, TS1 Ordered Sets, but must not exceed 1 ms, so as not to prematurely configure a smaller Link than possible.
  - ♦ After activating any inactive Lane, the Transmitter must wait for its TX common mode to settle before exiting Electrical Idle and transmitting the TS1 Ordered Sets.

❑ Optionally, if crosslinks are supported, then all Upstream Lanes that detected a Receiver during Detect must first transmit 16–32 TS1s with a PAD Link number and PAD Lane number and after this occurs and if any Upstream Lanes first receive two consecutive TS1 Ordered Sets with Link and Lane numbers set to PAD (K23.7), then:

- The Transmitter continues to send out TS1 Ordered Sets with Link numbers and Lane numbers set to PAD (K23.7).
- If any Lanes receive two consecutive TS1 Ordered Sets with Link numbers that are different than PAD (K23.7) and Lane number set to PAD (K23.7), a single Link number is selected and Lane number set to PAD are transmitted on all Lanes that both detected a Receiver and also received two consecutive TS1 Ordered Sets with Link numbers that are different than PAD (K23.7) and Lane number set to PAD (K23.7). Any left over Lanes that detected a Receiver during Detect must transmit TS1 Ordered Sets with the Link and Lane number set to PAD (K23.7). The next state is Configuration.Linkwidth.Accept.
  - ♦ Note: It is recommended that any possible multi-Lane Link that received an error in a TS1 Ordered Set on a subset of the received Lanes; delay the evaluation listed above by an additional two, or more, TS1 Ordered Sets, but must not exceed 1 ms, so as not to prematurely configure a smaller Link than possible.

In Section 4.2.6.3.2.1, page 206, line 20, make the following edit:

- Note: It is recommended that any possible multi-Lane Link that received an error in a TS1 Ordered Set on a subset of the received Lanes delay the evaluation listed above by an additional two, or more, TS1 Ordered Sets, but must not exceed 1 ms, so as not to prematurely configure a smaller Link than possible.

In Section 4.2.6.3.2.2, page 207, line 5, make the following edit:

- Note: It is recommended that any possible multi-Lane Link that received an error in a TS1 Ordered Sets on a subset of the received Lanes delay the evaluation listed above by an additional two, or more, TS1 Ordered Sets, but must not exceed 1 ms, so as not to prematurely configure a smaller Link than possible.

In Section 4.2.6.3.3.1, page 208, line 30, make the following edit:

- Note: It is recommended that any possible multi-Lane Link that received an error in a TS1 Ordered Sets on a subset of the received Lanes delay the evaluation listed above by an additional two, or more, TS1 Ordered Sets, but must not exceed 1 ms, so as not to prematurely configure a smaller Link than possible.

In Section 4.2.6.3.3.1, page 209, line 10, make the following edit:

- Note: It is recommended that any possible multi-Lane Link that received an error in a TS1 Ordered Set on a subset of the received Lanes delay the evaluation listed above by an additional two, or more, TS1 Ordered Sets, but must not exceed 1 ms, so as not to prematurely configure a smaller Link than possible.

In Section 4.2.6.3.3.2, page 209, line 30, make the following edit:

- Note: It is recommended that any possible multi-Lane Link that received an error in a TS1 Ordered Sets on a subset of the received Lanes delay the evaluation listed above by an additional two, or more, TS1 Ordered Sets, but must not exceed 1 ms, so as not to prematurely configure a smaller Link than possible.

B30 Multi-Function Virtual Channel Capability

In Section 7.18, page 552, line 5, make the following edit:

The Multi-Function Virtual Channel (MFVC) Capability is an optional Extended Capability ~~required for multi-Function devices that have individual Functions that support functionality beyond the default Traffic Class (TC0) over the default Virtual Channel (VC0).~~that permits enhanced QoS management in a multi-Function device, including TC/VC mapping, optional VC arbitration, and optional Function arbitration for Upstream Requests. When implemented, the MFVC Capability structure must be present in the Extended Configuration Space of Function 0 of the multi-Function device's Upstream Port. Figure 7-79 provides a high level view of the MFVC Capability structure. This MFVC Capability structure controls Virtual Channel assignment at the PCI Express Upstream Port of the multi-Function device, while a VC Capability structure, if present in a Function, controls the Virtual Channel assignment for that individual Function.

B31 Configuration Request Routing Rules

In Section 7.3.3, page 422, lines 15 and 23, make the following edits:

- ❑ If Configuration Request Type is 0,
  - Determine if the Request addresses a valid local Configuration Space of an implemented Function
    - ♦ If so, process the Request
    - ♦ If not, follow rules for handling Unsupported Requests

For Root Ports, Switches, and PCI Express-PCI Bridges, the following rules apply:

- ❑ Propagation of Configuration Requests from Downstream to Upstream as well as peer-to-peer are not supported
  - Configuration Requests are initiated only by the Host Bridge
- ❑ If Configuration Request Type is 0,
  - Determine if the Request addresses a valid local Configuration Space of an implemented Function
    - ♦ If so, process the Request
    - ♦ If not, follow rules for handling Unsupported Requests

B32 Physical Layer Error List

In Section 6.2.7, page 355, Table 6-2, make the following edit:

Error Name	Error Type (Default Severity)	Detecting Agent Action[1]	References
Receiver Error	Correctable	*Receiver:* Send ERR_COR to Root Complex.	Section 4.2.1.3 Section 4.2.2 Section 4.2.4.6 Section 4.2.6

[1] For these tables, detecting agent action is given as if all enable bits are set to "enable" and, for Advanced Error Handling, mask bits are disabled and severity bits are set to their default values. Actions must be modified according to the actual settings of these bits.

B33 Address Field Mapping

In Section 2.2.4.1, page 57, Table 2-6, make the following edit:

Address Bits	32-bit Addressing	64-bit Addressing
63:56	Not Applicable	Bits 7:0 of Byte 8
55:~~47~~48	Not Applicable	Bits 7:0 of Byte 9
47:40	Not Applicable	Bits 7:0 of Byte 10
39:32	Not Applicable	Bits 7:0 of Byte 11
31:24	Bits 7:0 of Byte 8	Bits 7:0 of Byte 12
23:16	Bits 7:0 of Byte 9	Bits 7:0 of Byte 13
15:8	Bits 7:0 of Byte 10	Bits 7:0 of Byte 14
7:2	Bits 7:2 of Byte 11	Bits 7:2 of Byte 15

B34 MSI and MSI-X Capability Structures

In Section 7.7, page 439, line 2, make the following edit:

MSI, MSI-X, and their ~~and the MSI~~ Capability structures are defined in the *PCI Local Bus Specification, Revision 3.0*. ~~MSI-X, the MSI-X Capability structure, and new optional MSI features are defined in the MSI-X ECN for the *PCI Local Bus Specification, Revision 3.0*.~~

B35 Header Log Register

In Section 7.10.8, page 504, line 5, make the following edit:

The header is captured such that, when read using DW accesses, the fields of the header are laid out ~~read by software~~ in the same way the headers are presented in this document~~, when the register is read using DW accesses~~. Therefore, byte 0 of the header is located in byte 3 of the Header Log register, byte 1 of the header is in byte 2 of the Header Log register and so forth. For 12-byte headers, only bytes 0 through 11 of the Header Log register are used and values in bytes 12 through 15 are undefined.

B36 L0

In Section 4.2.6.5, page 223, line 9, make the following edit:

- For a Downstream component, the directed_speed_change variable must not be set to 1b if it has never recorded greater than 2.5 GT/s data rate identifier(s) advertised in Configuration.Complete or Recovery.RcvrCfg~~Complete~~ substates by the Upstream component since exiting the Detect state.

B37 LCRC and Sequence Number Rules (TLP Transmitter)

In Section 3.5.2.1, page 154, line 17, make the following edit:

When measuring replay timing to the point when TLP retransmission begins, compliance tests must allow for any other TLP or DLLP transmission already in progress in that direction (thus preventing the TLP retransmission). Also, compliance tests must allow for implementations that statically adjust the REPLAY_TIMER by the L0s exit latency of the Ack's Link.~~if either~~ Finally, if the retransmitted TLP's Link is enabled for L0s, compliance tests must allow for its L0s exit latency[19]~~, either with the Link over which the Ack is transmitted, or with the Link over which the TLP is retransmitted~~.

B38 Error Message Forwarding and PCI Mapping for Bridge -- Rules

In Section 6.2.8.1, page 359, line 21, make the following edit:

- Poisoned TLPs are forwarded according to the same rules as non-Poisoned TLPs
  - When forwarding a Poisoned ~~TLP from Primary to Secondary~~Request Downstream:
    - ~~the Receiving side must s~~Set the Detected Parity Error bit in the Status register
    - ~~the Transmitting side must s~~Set the Master Data Parity Error bit in the Secondary Status register if the Parity Error Response Enable bit in the Bridge Control register is set
  - When forwarding a Poisoned Completion Downstream:
    - Set the Detected Parity Error bit in the Status register
    - Set the Master Data Parity Error bit in the Status register if the Parity Error Response bit in the Command register is set
  - When forwarding a Poisoned ~~TLP from Secondary to Primary~~Request Upstream:
    - ~~the Receiving side must s~~Set the Detected Parity Error bit in the Secondary Status register
    - ~~the Transmitting side must s~~Set the Master Data Parity Error bit in the Status register if the Parity Error Response bit in the Command register is set
  - When forwarding a Poisoned Completion Upstream:
    - Set the Detected Parity Error bit in the Secondary Status register
    - Set the Master Data Parity Error bit in the Secondary Status register if the Parity Error Response Enable bit in the Bridge Control register is set

In Section 7.5.1.2, Table 7-4, page 430, bit 8, make the following edit:

Bit Location	Register Description	Attributes
8	**Master Data Parity Error** – See Section 7.5.1.7. This bit is Set by ~~a Requester (Primary Side for Type 1 Configuration Space header Function)~~an Endpoint Function if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs: • ~~Requester~~Endpoint receives a Poisoned Completion~~ marked poisoned~~ • ~~Requester~~Endpoint transmits a Poisoned~~ poisons a write~~ Request This bit is Set by a Root Port, Switch Upstream Port, or Switch Downstream Port if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs: • Port receives a Poisoned Completion going Downstream • Port transmits a Poisoned Request Upstream If the Parity Error Response bit is 0b, this bit is never Set. Default value of this bit is 0b.	RW1C

In Section 7.5.3.4, Table 7-5, page 435, bit 8, make the following edit:

Bit Location	Register Description	Attributes
8	**Master Data Parity Error** – See Section 7.5.1.7. This bit is Set by a Root Port, Switch Upstream Port, or Switch Downstream Port, ~~the Secondary side Requester~~ if the Parity Error Response Enable bit in the Bridge Control register is Set and either of the following two conditions occurs: • Port ~~Requester~~ receives a Poisoned Completion coming Upstream~~marked poisoned~~ • Port~~Requester~~ transmits a ~~poisons a write~~ Poisoned Request Downstream If the Parity Error Response Enable bit is Clear, this bit is never Set. Default value of this bit is 0b.	RW1C

B39 Multicast ECN

In the *Multicast ECN*, page 6, make following edit to Implementation Note:

IMPLEMENTATION NOTE

Multicast, ATS, and Redirection

…When either type of sender targets these ranges with Memory Writes, each TLP that satisfies the access control checks will be reflected back down by the RC with a Translated Address targeting a protected Multicast Window[footnote]. ATS-capable senders can request and cache Translated Addresses using the RC Memory Space range, and then later use those Translated Addresses for Memory Writes that target protected Multicast Windows directly and can be Multicast without a taking a trip through the RC.…

[footnote] If the original sender belongs to the MCG associated with this Window, the original sender will also receive a copy of the reflected TLP.

In the *Multicast ECN*, page 6, make following edit:

If the TLP is not blocked in a Switch or Root Complex it is forwarded out all of the Ports, except its Ingress Port, whose MC_Receive bit corresponding to the extracted MCG is set. In an Endpoint, it is consumed by all Functions whose MC_Receive bit corresponding to the extracted MCG is set. If no Ports forward the TLP or no Functions consume it, the TLP is silently dropped.

~~Note that t~~ To prevent loops, it is prohibited for a Root Port or a Switch Port to forward a TLP back out its Ingress Port, even if so specified by the MC_Receive register associated with the Port. An exception is the case described in the preceding Implementation Note, where an RC reflects a unicast TLP that came in on an Ingress Root Port to a Multicast Window. In that case, when specified by the MC_Receive register associated with that Ingress Root Port, the RC is required to send the reflected TLP out the same Root Port that it originally came in.

In the *Multicast ECN*, page 5, add the following Implementation Note as indicated:

…

Components next check the MC_Block_All and the MC_Block_Untranslated bits corresponding to the extracted MCG. Switches and Root Ports check Multicast TLPs in their Ingress Ports using the MC_Block_All and MC_Block_Untranslated registers associated with the Ingress Port. Endpoint Functions check Multicast TLPs they are preparing to send, using their MC_Block_All and MC_Block_Untranslated registers. If the MC_Block_All bit corresponding to the extracted MCG is set, the TLP is handled as an MC Blocked TLP. If the MC_Block_Untranslated bit corresponding to the extracted MCG is set and the TLP contains an Untranslated Address, the TLP, is also handled as an MC Blocked TLP.

IMPLEMENTATION NOTE

MC_Block_Untranslated and PIO Writes

Programmed I/O (PIO) Writes to Memory Space generally have Untranslated addresses since there is no architected mechanism for software to control the Address Type (AT) field for PIO Requests. Thus, if it's necessary for a given Switch to Multicast any PIO Writes, software should ensure that the appropriate MC_Block_Untranslated bits in the Upstream Port of that Switch are Clear. Otherwise, the Switch Upstream Port may block PIO Writes that legitimately target Multicast Windows.

Since it may be necessary for software to clear MC_Block_Untranslated bits in a Switch Upstream Port for the sake of PIO Writes, the following are strongly recommended for a Root Complex capable of Address translation:

- All Integrated Endpoints each implement a Multicast Capability structure to provide access control for sending Untranslated Multicast TLPs.
- All peer-to-peer capable Root Ports each implement a Multicast Capability structure to provide access control for Untranslated Multicast TLPs that are forwarded peer-to-peer.

For similar reasons, with Multicast-capable Switch components where the Upstream Port is a Function in a multi-Function device, it is strongly recommended that any Endpoints in that multi-Function device each implement a Multicast Capability structure.

B40 Message Code Usage

Add the following new Appendix as indicated:

X Message Code Usage

This appendix contains a list of currently defined PCI Express Message Codes. Message codes are defined in this specification and in other specifications. This table will be updated as Messages are defined in other specifications but due to document release schedules, this table may not contain recently defined Messages.

Table X-1: Message Code Usage

Message Code	Routing r[2:0]	Type	Description
0000 0000	011	Msg	Unlock, see Section 2.2.8.4
0000 0001	010	MsgD	Invalidate Request Message, see the *Address Translation Services Specification*
0000 0010	010	Msg	Invalidate Completion Message, see *Address Translation Services Specification*
0000 0100	000	Msg	Page Request Message, see *Address Translation Services Specification*
0000 0101	010	Msg	PRG Response Message, see *Address Translation Services Specification*
0001 0000	100	Msg	Latency Tolerance Reporting (LTR) Message, see Section 2.2.8.x
0001 0100	100	Msg	PM_Active_State_Nak, see Section 2.2.8.2
0001 1000	000	Msg	PM_PME, see Section 2.2.8.2
0001 1001	011	Msg	PME_Turn_Off, see Section 2.2.8.2
0001 1011	101	Msg	PME_TO_Ack, see Section 2.2.8.2
0010 0000	100	Msg	Assert_INTA, see Section 2.2.8.1
0010 0001	100	Msg	Assert_INTB, see Section 2.2.8.1
0010 0010	100	Msg	Assert_INTC, see Section 2.2.8.1
0010 0011	100	Msg	Assert_INTD, see Section 2.2.8.1
0010 0100	100	Msg	Deassert_INTA, see Section 2.2.8.1
0010 0101	100	Msg	Deassert_INTB, see Section 2.2.8.1
0010 0110	100	Msg	Deassert_INTC, see Section 2.2.8.1
0010 0111	100	Msg	Deassert_INTD, see Section 2.2.8.1
0011 0000	000	Msg	ERR_COR, see Section 2.2.8.3
0011 0001	000	Msg	ERR_NONFATAL, see Section 2.2.8.3
0011 0011	000	Msg	ERR_FATAL, see Section 2.2.8.3
0100 0000	100	Msg	Ignored Message, see Section 2.2.8.7

Message Code	Routing r[2:0]	Type	Description
0100 0001	100	Msg	Ignored Message, see Section 2.2.8.7
0100 0011	100	Msg	Ignored Message, see Section 2.2.8.7
0100 0100	100	Msg	Ignored Message, see Section 2.2.8.7
0100 0101	100	Msg	Ignored Message, see Section 2.2.8.7
0100 0111	100	Msg	Ignored Message, see Section 2.2.8.7
0100 1000	100	Msg	Ignored Message, see Section 2.2.8.7
0101 0000	100	MsgD	Set_Slot_Power_Limit, see Section 2.2.8.5
0111 1110	000, 010, 011, or 100	Msg/MsgD	Vendor_Defined Type 0, see Section 2.2.8.6
0111 1111	000, 010, 011, or 100	Msg/MsgD	Vendor_Defined Type 1, see Section 2.2.8.6

B41 Resizable BAR ECN

In the *Resizable BAR ECN*, page 8, Table 7-x3, bit location 12:8 make following edit:

Table 7-x3 Resizable BAR Control Register

Bit Location	Register Description	Attributes
12:8	**...** When this register field is programmed, the value is immediately reflected in the size of the resource, as encoded in the number of read-only bits in the BAR. Software must only write supported values that correspond to those reported in the Resizable BAR Capability register. Writing an unsupported value will produce undefined results.	R/W

B42 Internal Error Reporting ECN

In the *Internal Error Reporting ECN*, page 8, line 18, make following edits:

If the Advisory Non-Fatal Error Mask bit is clear, logging proceeds by setting the "corresponding" bit in the Uncorrectable Error Status register, based upon the specific uncorrectable error that's being reported as an advisory error ~~and recording the header~~. If the "corresponding" uncorrectable error bit in the Uncorrectable Error Mask register is clear~~, the First Error Pointer and Header Log registers are updated to log the error, assuming they are not still "occupied" by a previous unserviced error.~~ and the error is one that requires header logging, then the header is recorded, subject to the availability of resources. See Section 6.2.4.2.

B43 Dynamic Power Allocation ECN

In the *Dynamic Power Allocation ECN*, page 5, make following edits to Figure 7-xx:

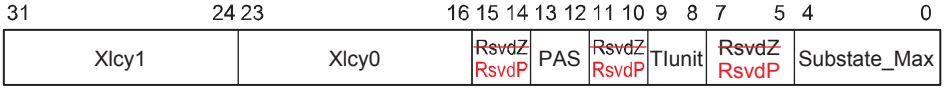

Figure 7-xx DPA Capability Register

B44 Multicast ECN

In the *Multicast ECN*, page 4, line 18, make following edits:

In this step, each Switch Ingress Port and other components use values of MC_Enable, MC_Base_Address, MC_Index_Position, and MC_Num_Group from any one of their Functions. Software is required to configure all Functions to have the same values in each of these fields ~~identically~~ and results are indeterminate if this is not the case.

B45 Multicast ECN

In the *Multicast ECN*, page 15, Table 7-xx, bit location 15, make following edits:

Table 7-xx Multicast Capability Register

Bit Location	Register Description	Attributes
15	**MC_ECRC_Regeneration_Supported** – If S~~s~~et, indicates that ECRC regeneration is supported. This bit must not be Set unless the Function supports Advanced Error Reporting, and the ECRC Check Capable bit in the Advanced Error Capabilities and Control register is also Set. However, if ECRC regeneration is supported, its operation is not contingent upon the setting of the ECRC Check Enable bit in the Advanced Error Capabilities and Control register.	RO

B46 Multicast ECN

In the *Multicast ECN*, page 16, Table 7-xx, bit location 15, make following edits:

Table 7-xx Multicast Control Register

Bit Location	Register Description	Attributes
15	MC_Enable – When Sset, the Multicast mechanism~~Capability~~ is enabled for the component. Default is 0.	RW

B47 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 4, line 28 make following edit:

It is strongly recommended that Endpoints send no more than two LTR Messages within any 500 µs time period, except where required to by the specification.

B48 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 4, line 29 make following edit:

Downstream Ports must not generate an error if more than two LTR Messages are received within a 500 µs time period, and must properly handle all LTR Messages regardless of the time interval between them.

B49 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 5, line 1 make following edit:

- The MFD must transmit a~~n~~ new LTR Message Upstream when any Function of the MFD changes the values it has reported internally in such a way as to change the conglomerated value earlier reported by the MFD.

B50 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 5, line 8 make following edit:

- A Switch ~~must only~~Upstream Port is permitted to transmit LTR Messages only when its~~the~~ LTR Mechanism Enable bit is Sset, ~~at the Upstream Port~~ or shortly after software clears its LTR Mechanism Enable bit, as described earlier in this section.

B51 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 8, bit 11 make following edit:

Bit Location	Register Description	Attributes
11	**LTR Mechanism Supported** – A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. Root Ports, Switches and Endpoints are permitted to implement this capability. For a multi-Function device associated with an Upstream Port, each Function must report the same value for this bit. For Bridges~~, Downstream Ports,~~ and ~~components~~ other Functions that do not implement this capability, this bit must be hardwired to 0b.	RO

B52 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 10, line 4, make following edit:

The PCI Express Latency Tolerance Reporting (LTR) Capability is an optional Extended Capability that allows software to provide platform latency information to components with Upstream Ports (Endpoints and Switches), and is required if the component supports LTR. It is not applicable to Root Ports, Bridges, or Downstream Ports in a Switch.

B53 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 11, Table LTR4, bit location 9:0, make following edit:

Table <LTR4>: Max Snoop Latency Register

Bit Location	Register Description	Attributes
9:0	**Max Snoop LatencyValue —**Along with the Max Snoop LatencyScale field, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. The default value for this field is 0. Hardware operation is undefined if software writes a Not Permitted value to this field.	RW

In the *Latency Tolerance Reporting ECN*, page 11, Table LTR3, bit location 9:0, make following edit:

Table <LTR3>: Max No-Snoop Latency Register

Bit Location	Register Description	Attributes
9:0	**Max No-Snoop LatencyValue —** Along with the Max No-Snoop LatencyScale field, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. The default value for this field is 0. Hardware operation is undefined if software writes a Not Permitted value to this field.	RW

B54 ID-Based Ordering ECN

After Figure 2-6 on page 3 of the *ID-Based Ordering ECN*, add the following:

Modify Figure 2-10 Transaction Descriptor as shown:

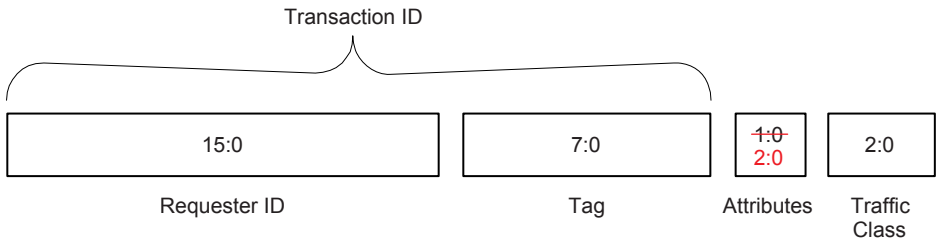

Figure 2-10: Transaction Descriptor

B55 Flow Control Update DLLPs

In Section 4.2.4.3, Table 4-6, page 183, make the following edit:

Table 4-6: Electrical Idle Inference Conditions

State	2.5 GT/s	5.0 GT/s
L0	Absence of ~~Update_FC~~ Flow Control Update DLLP[footnote] or alternatively a SKP Ordered Set in 128 µs window	Absence of ~~Update_FC~~ Flow Control Update DLLP[footnote] or alternatively a SKP Ordered Set in 128 µs window

[footnote] A Flow Control Update DLLP is either an Update_FC as defined in this specification or an MRUpdateFC as defined in the Multi-Root I/O Virtualization and Sharing Specification (MR-IOV).

In Section 4.2.4.3, page 184, line 1, make the following edit:

In L0 state, some number of ~~Update_FC's~~Flow Control Update DLLPs are expected to be received in a 128 µs window.

In Section 4.2.4.3, page 184, line 4, make the following edit:

…Hence, the absence of either a~~n Update_FC~~Flow Control Update DLLP or alternatively a SKP Ordered Set in any 128 µs window can be inferred as Electrical Idle

B56 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 11, Table LTR4, bit location 9:0, make following edit:

Table <LTR4>: Max Snoop Latency Register

Bit Location	Register Description	Attributes
9:0	**Max Snoop LatencyValue —**Along with the Max Snoop LatencyScale field, this register specifies the maximum ~~no-snoop~~snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. The default value for this field is 0.	RW

B57 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 8, bit 11 make following edit:

Bit Location	Register Description	Attributes
11	**LTR Mechanism Supported** – A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism ~~capability~~. Root Ports, Switches and Endpoints are permitted to implement this capability. …	RO

B58 Message Request Rules

In Section 2.2.8, page 69, line 7, make the following edit:

This document defines the following groups of Messages:

- INTx Interrupt Signaling
- Power Management
- Error Signaling
- Locked Transaction Support
- Slot Power Limit Support
- Vendor-Defined Messages
- LTR Messages

B59 Receiver Tolerancing Clarification

In Section 4.3.4.2, page 262, Table 4-10, make the following edits:

Table 4-10: 5.0 GT/s Limits for Common Refclk Rx Architecture

Parameter	Description	Min	Max	Units	Notes
UI	Unit interval without including of SSC	~~200.06~~1 99.94	~~199.94~~2 00.06	ps	Over 10^6 UI
$T_{RX-HF-RMS}$	1.5 – 100 MHz RMS jitter		3.4	ps RMS	Spectrally flat, 3
$T_{RX-HF-DJ-DD}$	Max Dj impinging on Rx under test		88	ps	2,4
$T_{RX-SSC-RES}$	33 kHz Refclk residual	--	75	ps	
$T_{RX-LF-RMS}$	< 1.5 MHz RMS jitter	--	4.2	ps RMS	Spectrally flat
$T_{RX-MIN-PULSE}$	Minimum single pulse applied at Rx	120		ps	2
$V_{RX-MIN-MAX-RATIO}$	Min/max pulse voltage ratio seen over an time interval of 2 UI.	--	5		2
V_{RX-EYE}	Receive eye voltage opening	120		mVPP diff	1,3
$V_{RX-CM-CH-SRC}$	Common mode noise from Rx	--	300	mVPP	2

Notes:

1. Refer to Figure 4-41 for a description of how the Rx eye voltage is defined.
2. Accumulated over 10^6 UI.

3. Minimum eye is obtained by first injecting maximum Dj and then adjusting Rj until a minimum eye (defined by T_{RX-EYE}) is reached. Rj is spectrally flat before being filtered with a BPF having 3 dB cut-offs f_{C-LOW} and f_{C-HIGH} of 1.5 MHz and 100 MHz, respectively with step rolloff at 1.5 MHz and a 20 dB/decade rolloff on the high side. Minimum eye width is defined for a sample size equivalent to a BER of 10^{-12}.
4. Different combinations of $T_{RX-HF-DJ-DD}$ and $T_{RX-HF-RMS}$ are needed to measure $T_{RX-TJ-CC}$ and $T_{RX-DJ-DD-CC}$.

In Section 4.3.4.3, page 263, Table 4-11, make the following edits:

Table 4-11: 5.0 GT/s Tolerancing Limits for Data Clocked Rx Architecture

Parameter	Description	Min	Max	Units	Notes
UI	Unit interval without including of SSC	~~200.06 ppm~~199.94	~~199.94 ppm~~200.06	ps	Over 10^6 UI
$T_{RX-HF-RMS}$	1.5 – 100 MHz RMS jitter		4.2	ps RMS	Spectrally flat, ~~Note 2~~3
$T_{RX-HF-DJ-DD}$	Max Dj impinging on Rx under tolerancing		88	ps	2,4
$T_{RX-LF-SSC-FULL}$	Full 33 kHz SSC	--	20	ns	2
$T_{RX-LF-RMS}$	10 kHz to 1.5 MHz RMS jitter	--	8.0	ps RMS	Spectrally flat
$T_{RX-MIN-PULSE}$	Minimum single pulse applied at Rx	120		ps	2
$V_{RX-MIN-MAX-RATIO}$	Min/max pulse voltage ratio seen over an time interval of 2 UI.	--	5		2
V_{RX-EYE}	Receive eye voltage opening	100		mVPP diff	1,3
$V_{RX-CM-CH-SRC}$	Common mode noise from Rx	--	300	mVPP	2

Notes:

1. Refer to Error! Reference source not found. for a description of how the Rx eye voltage is defined.
2. Accumulated for 10^6 UI.
3. Minimum eye is obtained by first injecting maximum Dj and then adjusting Rj until a minimum eye (defined by T_{RX-EYE}) is reached. Rj is spectrally flat before being filtered with a BPF having 3 dB cut-offs f_{C-LOW} and f_{C-HIGH} of 1.5 MHz and 100 MHz, respectively with step rolloff at 1.5 MHz and a 20 dB/decade rolloff on the high side. Minimum eye width is defined for a sample size equivalent to a BER of 10^{-12}.
4. Different combinations of $T_{RX-HF-DJ-DD}$ and $T_{RX-HF-RMS}$ are needed to measure $T_{RX-TJ-DC}$ and $T_{RX-DJ-DD-DC}$.

C1 LCRC and Sequence Number Rules (TLP Receiver)

In Section 3.5.3.1, page 159, line 10, make the following edit:

- ❑ The following 12-bit counter is used:
  - NEXT_RCV_SEQ – Stores the expected Sequence Number for the next TLP
    - ♦ Set to ~~all~~ 000h in DL_Inactive state

C2 ARI Control Register

In the *Alternative Routing-ID Interpretation (ARI) ECN*, page 32, ARI Control Register Table make the following edit:

Bit Location	Register Description	Attributes
6:4	**Function Group –** Assigns a Function Group Number to this Function. Default value of this field is 000b. Must be hardwired to 000b if in Function 0, the MFVC Function Groups Capability bit and ACS Function Groups Capability bit are both 0b.	RW

C3 TS1 and TS2

In Section 4.2.4.4, page 184, line 17, make the following edit:

During the training sequence, the Receiver looks at Symbols 6-15 of the TS1 and TS2 Ordered Sets as the indicator of Lane polarity inversion (D+ and D- are swapped). …

In Section 4.2.6.1.1, page 194, line 7, make the following edit:

- Note: This does not affect the advertised data rate in the TS1 and TS2 Ordered Sets.

C4 TS1s

In Section 4.2.6.2.1, page 196, line 25, make the following edit:

...

1. the Lane and Link numbers set to PAD (K23.7),
2. the Compliance Receive bit (bit 4 of Symbol 5) is 0b or Loopback bit (bit 2 of Symbol 5) is 1b.

and a minimum of 1024 ~~TS1s~~ TS1 Ordered Sets are transmitted after receiving one TS1.

In Section 4.2.6.3.1.1, page 203, line 28, make the following edit:

- ❑ Else: Optionally, if crosslinks are supported, then all Downstream Lanes that detected a Receiver during Detect must first transmit 16-32 ~~TS1s~~ TS1 Ordered Sets with a non PAD Link number and PAD Lane number and after this occurs if any Downstream Lanes receive two consecutive TS1 Ordered Sets with a Link number different than PAD (K23.7) and a Lane Number set to PAD, the Downstream Lanes are now designated as Upstream Lanes and a new random cross Link timeout is chosen (see $T_{crosslink}$ in Table 4-9). ...

In Section 4.2.6.3.1.2, page 205, line 26, make the following edit:

- ❑ Optionally, if crosslinks are supported, then all Upstream Lanes that detected a Receiver during Detect must first transmit 16–32 ~~TS1s~~ TS1 Ordered Sets with a PAD Link number and PAD Lane number and after this occurs and if any Upstream Lanes first receive two consecutive TS1 Ordered Sets with Link and Lane numbers set to PAD (K23.7), then: ...

In Section 4.2.6.3.2.2, page 207, line 21, make the following edit:

3. A x8 Downstream Port where only seven Lanes are receiving ~~TS1s~~ TS1 Ordered Sets with the same received Link number (non-PAD and matching one that was transmitted by the Downstream Lanes) and an eighth Lane, which is in the middle or adjacent to those same Lanes, is not receiving a TS1 Ordered Set. …

In Section 4.2.6.3.4.2, page 210, line 20, make the following edit:

...

a. If any of the Lanes receive two consecutive ~~TS1s~~ TS1 Ordered Sets that have a Lane number different from when the Lane first entered Configuration.Lanenum.Wait, and not all the Lanes' Link numbers are set to PAD (K23.7)

or...

C5 TS1

In Section 4.2.6.2.1, page 196, line 25, make the following edit:

1. the Lane and Link numbers set to PAD (K23.7),
2. the Compliance Receive bit (bit 4 of Symbol 5) is 0b or Loopback bit (bit 2 of Symbol 5) is 1b.

and a minimum of 1024 TS1s are transmitted after receiving one TS1 Ordered Set.

In Section 4.2.6.3.5.1, page 211, line 1, make the following edit:

- ❑ TS2 Ordered Sets are transmitted using Link and Lane numbers that match the received TS1 Ordered Set Link and Lane numbers.

C6 TS1

In Section 4.2.6.3.2.2, page 207, line 1, make the following edit:

- ❑ … Remaining Lanes must transmit TS1 Ordered Sets with Link and Lane numbers set to PAD (K23.7).

In Section 4.2.6.3.2.2, page 208, line 3, make the following edit:

a. … The Upstream Port will assign a Lane 0 to only the received Lane 7 (received Lane number n-1) and the remaining seven Lanes must transmit TS1 Ordered Sets with Link and Lane numbers set to PAD (K23.7)

C7 TS1 ordered sets

In Section 4.2.6.4.1, page 215, line 17, make the following edit:

- ❑ ... It must also be noted that since the Downstream component's request may not reach the Upstream component due to bit errors in the TS1 ~~ordered sets~~Ordered Sets, the Downstream component may attempt to re-request the desired de-emphasis level in subsequent entries to Recovery state when speed change is requested. ...

C8 TS1 or TS2

In Section 4.2.6.4.1, page 216, line 28, make the following edit:

- Else the next state is Configuration if any of the configured Lanes that are receiving a TS1 or TS2 Ordered Set have received at least one TS1 or TS2 Ordered Set with Link and Lane numbers that match what is being transmitted on those same Lanes and the operating speed has not changed to a mutually negotiated data rate (i.e., changed_speed_recovery = 0b) since entering Recovery and at least one of the following conditions is true:…

C9 Port VC Capability Register 2

In Section 7.11.3, page 515, Table 7-41, make the following edit:

Bit Location	Register Description	Attributes
7:0	**VC Arbitration Capability** – Indicates the types of VC Arbitration supported by the Function for the LPVC group. This field is valid for all Functions that report a Low Priority Extended VC Count field greater than 0. For all other Functions, this field must be hardwired to 00h. …	RO

C10 Configuration Register Types

In Section 7.4, page 424, line 2, make the following edit:

Configuration register fields are assigned one of the attributes described in Table 7-2. All PCI Express components, with the exception of the Root Complex and system-integrated devices, initialize register fields to specified default values.

C11 Port VC Control Register

In Section 7.11.4, page 516, Table 7-42, make the following edit:

Bit Location	Register Description	Attributes
3:1	**VC Arbitration Select** – Used ~~for~~by software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the Port VC Capability Register 2. This field is valid for all Functions. …	RW

C12 Port VC Control Register

In Section 7.18.4, page 557, Table 7-71, make the following edit:

Bit Location	Register Description	Attributes
0	**Load VC Arbitration Table** – Used ~~for~~by software to update the VC Arbitration Table. This bit is valid when the selected VC Arbitration uses the VC Arbitration Table. …	RW

C13 Port VC Control Register

In Section 7.18.4, page 557, Table 7-71, make the following edit:

Bit Location	Register Description	Attributes
3:1	**VC Arbitration Select** – Used ~~for~~by software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the Port VC Capability Register 2. …	RW

C14 Recovery.RcvrCfg

In Section 4.2.6.4.3, page 219, line 21, make the following edit:

- Note: For devices that support Link width upconfigure, it is recommended that the Electrical Idle detection circuitry should be activated in the set of currently inactive Lanes in this substate, the Recovery.Idle substate, and Configuration.Linkwidth.Start substates, if the directed_speed_change variable is reset to 0b. …

C15 Multi-Function Devices and Function Arbitration

In Section 6.3.3.4, page 369, line 16, make the following edit:

…However, ~~in contrast to~~unlike a complete Switch with devices on its Downstream Ports, the multi-Function device model does not support full QoS management for peer-to-peer requests between Functions or for Downstream requests.

C16 Link Control Register

In Section 7.8.7, page 462, Figure 7-16, make the following edit:

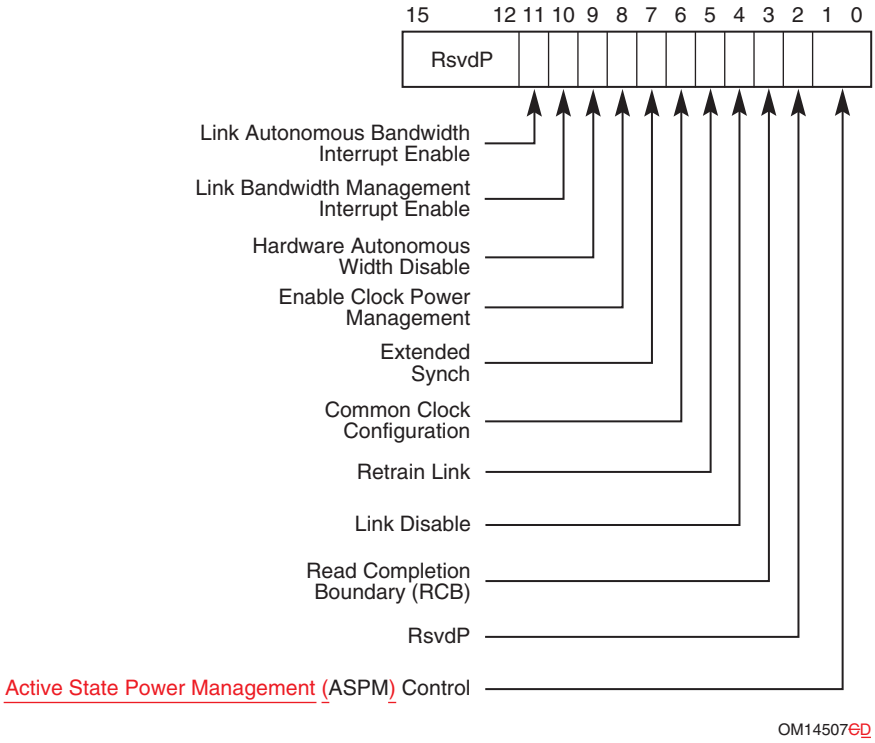

Figure7-16: Link Control Register

C17 Root Complex Link Control Register

In Section 7.14.3, page 538, Figure 7-66, make the following edit:

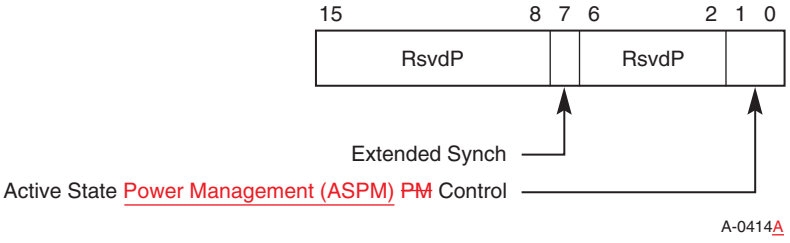

Figure 7-66: Root Complex Link Control Register

C18 Configuration.Linkwidth.Accept

In Section 4.2.6.3.1.2, page 205, line 12, make the following edit:

- Note: If the ~~LTTSM~~LTSSM is initiating upconfiguration of the Link width, it waits until it receives two consecutive TS1 Ordered Sets with a non-PAD (K23.7) Link Number and a PAD (K23.7) Lane number on all the inactive Lanes it wants to activate, or, 1 ms after entry to this substate, it receives two consecutive TS1 Ordered Sets on any Lane with a non-PAD (K23.7) Link number and PAD (K23.7) Lane number, whichever occurs earlier, before transmitting TS1 Ordered Sets with selected Link number and Lane number set to PAD (K23.7).

C19 Slot Power Limit Control

In Section 6.9, page 397, line 25, make the following edit:

- ❑ Captured Slot Power Limit Value and Scale fields of the Device ~~Capability~~Capabilities register implemented in Endpoint, Switch, or PCI Express-PCI Bridge Functions present in an Upstream Port

C20 Slot Power Limit Control

In Section 6.9, page 397, line 28, make the following edit:

- ❑ Set_Slot_Power_Limit Message that conveys the content of the Slot Power Limit Value and Scale fields of the Slot ~~Capability~~Capabilities register of the Downstream Port (of a Root Complex or a Switch) to the corresponding Captured Slot Power Limit Value and Scale fields of the Device Capabilities register in the Upstream Port of the component connected to the same Link

C21 Slot Power Limit Control

In Section 6.9, page 398, line 7, make the following edit:

- ❑ Thermal capabilities

  This software is responsible for correctly programming the Slot Power Limit Value and Scale fields of the Slot ~~Capability~~Capabilities registers of the Downstream Ports connected to slots.

  …

C22 Requestor

In Section 1.3.2.2, page 37, line 11, make the following edit:

- A PCI Express Endpoint must not support Locked Requests as a Completer or generate them as a ~~Requestor~~Requester. PCI Express-compliant software drivers and applications must be written to prevent the use of lock semantics when accessing a PCI Express Endpoint.

In Section 1.3.2.3, page 38, line 2, make the following edit:

- A Root Complex Integrated Endpoint must not support Locked Requests as a Completer or generate them as a ~~Requestor~~Requester. PCI Express-compliant software drivers and applications must be written to prevent the use of lock semantics when accessing a Root Complex Integrated Endpoint.

In Section 2.2.6.2, page 62, line 3, make the following edit:

- Tag[7:0] is a 8-bit field generated by each ~~Requestor~~Requester, and it must be unique for all outstanding Requests that require a Completion for that Requester

In Section 6.5.5, page 378, line 1, make the following edit:

A Root Complex is permitted to support locked transactions as a ~~Requestor~~Requester. If locked transactions are supported, a Root Complex must follow the sequence described in Section 6.5.2 to perform a locked access. ...

C23 Loopback.Entry

In Section 4.2.6.10.1, page 233, line 16, make the following edit:

- …The select_deemphasis variable must be set equal to the Selectable De-emphasis bit (bit 6~~)~~ of Symbol 4) in the two consecutive TS1 or TS2 Ordered Sets prior to entry to this substate. ...

C24 Modified Compliance Pattern

In Section 4.2.9, page 240, lines 4 and 5, make the following edits:

…Two identical error status Symbols followed by two K28.5 are appended to the basic Compliance sequence of 8b/10b Symbols (K28.5, D21.5, K28.5, and D10.2) to form the Modified Compliance Sequence of (K28.5, D21.5, K28.5, D10.2, ~~E~~error ~~S~~status Symbol, ~~E~~error ~~S~~status Symbol, K28.5, K28.5). …

In Section 4.2.9, page 240, in the Key for the Modified Compliance Pattern illustration, make the following edits:

Key:

K28.5-	COM when disparity is negative, specifically: "0011111010"
K28.5+	COM when disparity is positive, specifically: "1100000101"
D21.5	Out of phase data Symbol specifically: "1010101010"
D10.2	Out of phase data Symbol, specifically: "0101010101"
D	Delay Symbol K28.5 (with appropriate disparity)
ERR	~~E~~error ~~S~~status Symbol (with appropriate disparity)
K28.7-	EIE when disparity is negative, specifically "0011111000"

C25 Software Notification of Hot-Plug Events

In Section 6.7.3.4, page 395, line 28, make the following edit:

- ❑ At least one hot-plug event status bit in the Slot Status register and its associated ~~E~~enable bit in the Slot Control register are both set to 1b.

In Section 6.7.3.4, page 396, line 1, make the following edit:

- ❑ At least one hot-plug event status bit in the Slot Status register and its associated ~~E~~enable bit in the Slot Control register are both set to 1b.

C26 Ignored Messages

In Section 2.2.8.7, page 79, line 14, make the following edit:

- ❑ The Transaction ~~l~~Layer must account for flow control credit but take no other action in response to these messages

C27 Multi-Function Devices and Function Arbitration

In Section 6.3.3.4, page 369, line 13, make the following edit:

…Note that each Function optionally contains a VC Capability structure, which if present manages TC/VC mapping, optional Port Arbitration, and optional VC ~~a~~Arbitration, all within the Function. …

C28 Software Notification of Hot-Plug Events

In Section 6.7.3.4, page 395, lines 27 and 36, make the following edits:

…

- ❑ The Interrupt Disable bit in the Command register is set to 0b.
- ❑ The Hot-Plug Interrupt Enable bit in the Slot Control register is set to 1b.

...

- ❑ The associated vector is unmasked (not applicable if MSI does not support PVM).
- ❑ The Hot-Plug Interrupt Enable bit in the Slot Control register is set to 1b.

C29 Legacy Endpoint Rules

In Section 1.3.2.1, page 36, line 21, make the following edit:

- ❑ A Legacy Endpoint must support Configuration Requests as a Completer.

C30 Electrical Idle Sequences

In Section 4.2.4.2, page 181, line 6, make the following edit:

… After sending the last Symbol of the last Electrical Idle Ordered Set, the Transmitter must be in a valid Electrical Idle state as specified by $T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$ (see Table 4-9).

C31 PCI Express Reset - Rules

In Section 6.6, page 378, line 22, make the following edit:

This section specifies the PCI Express Reset mechanisms. This section covers the relationship between the architectural mechanisms defined in this document and the reset mechanisms defined in this document. Any relationship between the PCI Express Conventional Reset and component or platform reset is component or platform specific (except as explicitly noted).

C32 PCI Power Management Capability Structure

In Section 7.6, page 438, line 4, make the following edit:

… The functionality associated with this structure is the same for PCI Express as it is for conventional PCI, and only the added requirements associated with PCI Express are included here.

C33 Recovery.Speed

In Section 4.2.6.4.2, page 218, line 39, make the following edit:

- On a Link bandwidth change, if successful_speed_negotiation is set to 1b and the Autonomous Change bit (-bit 6 of Symbol 4) in the eight consecutive TS2 Ordered Sets in Recovery.RcvrCfg is set to 1b or the speed change was initiated by the Upstream component for autonomous (non-reliability and not due to the setting of the Link Retrain bit), the Link

C34 Link State Power Management

In Section 5.2, page 295, line 3, make the following edit:

- L0 – Active state.

  L0 support is required for both ASPM and PCI-PM compatible power management.

  …

C35 L0

In Section 4.2.6.5, page 223, line 3, make the following edit:

- LinkUp = 1b (status is set true).
  - On receipt of an STP or SDP Symbol, the idle_to_rlock_transitioned variable is reset to 0b.

C36 Acknowledgements

In the Acknowledgements section, page 606, make the following edit:

Mike Osborn	Advanced Micro Devices, Inc.
~~Johathan~~Jonathan Owen	Advanced Micro Devices, Inc.
Ali Oztaskin	Intel Corporation

C37 Refclk Architectures

In Section 4.3.7.2, page 285, line 17, make the following edit:

Three distinct Refclk architectures are possible: common Refclk, separate Refclks, and data driving PLL. Each has an associated filter function that comprehends the worst case combination of PLL bandwidth/peaking and equivalent jitter. The effective jitter seen at the Rx's clock-data recovery inputs is a function of the difference in Rx ~~and.~~and Tx PLL bandwidth and peaking convolved with the jitter spectrum of the Refclk. It is also dependent on the Refclk architecture.

C38 Captialization of "Message(s)"

In Section 5.3.1.2, page 300, lines 15 and 16, make the following edits:

D1 support is optional. While in the D1 state, a Function must not initiate any Request TLPs on the Link with the exception of a PME Message as defined in Section 5.3.3. Configuration and Message Requests are the only TLPs accepted by a Function in the D1 state. All other received Requests must be handled as Unsupported Requests, and all received Completions may optionally be handled as Unexpected Completions. If an error caused by a received TLP (e.g., an Unsupported Request) is detected while in D1, and reporting is enabled, the Link must be returned to L0 if it is not already in L0 and an error ~~message~~Message must be sent. If an error caused by an event other than a received TLP (e.g.,. a Completion Timeout) is detected while in D1, an error ~~message~~Message must be sent when the Function is programmed back to the D0 state.

In Section 5.3.1.3, page 300, lines 30 and 31, make the following edits:

D2 support is optional. While in the D2 state, a Function must not initiate any Request TLPs on the Link with the exception of a PME Message as defined in Section 5.3.3. Configuration and Message requests are the only TLPs accepted by a Function in the D2 state. All other received Requests must be handled as Unsupported Requests, and all received Completions may optionally be handled as Unexpected Completions. If an error caused by a received TLP (e.g., an Unsupported Request) is detected while in D2, and reporting is enabled, the Link must be returned to L0 if it is not already in L0 and an error ~~message~~Message must be sent. If an error caused by an event other than a received TLP (e.g., a Completion Timeout) is detected while in D2, an error ~~message~~Message must be sent when the Function is programmed back to the D0 state. Note that a Function's software driver participates in the process of transitioning the Function from D0 to D2. It contributes to the process by saving any functional state (if necessary), and otherwise preparing the Function for the transition to D2. As part of this quiescence process the Function's software driver must ensure that any mid-transaction TLPs (i.e., Requests with outstanding Completions), are terminated prior to handing control to the system configuration software that would then complete the transition to D2.

In Section 5.3.1.4.1, page 301, lines 30 and 31, make the following edits:

Configuration and Message requests are the only TLPs accepted by a Function in the D3hot state. All other received Requests must be handled as Unsupported Requests, and all received Completions may optionally be handled as Unexpected Completions. If an error caused by a received TLP (e.g., an Unsupported Request) is detected while in D3hot, and reporting is enabled, the Link must be returned to L0 if it is not already in L0 and an error ~~message~~Message must be sent. If an error caused by an event other than a received TLP (e.g., a Completion Timeout) is detected while in D3hot, an error ~~message~~Message may optionally be sent when the Function is programmed back to the D0 state.

In Section 7.5.1.1, page 428, Table 7-3, make the following edit:

Bit Location	Register Description	Attributes
8	**SERR# Enable** – See Section 7.5.1.7. When Set, this bit enables reporting of Non-fatal and Fatal errors detected by the Function to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI Express specific bits in the Device Control register (see Section 7.8.4). In addition, for Functions with Type 1 Configuration Space headers, this bit controls transmission by the primary interface of ERR_NONFATAL and ERR_FATAL error ~~messages~~Messages forwarded from the secondary interface. This bit does not affect the transmission of forwarded ERR_COR messages. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.	RW

In the Terms and Acronyms section, page 25, make the following edits:

error reporting	In a broad context, the general notification of errors. In the context of the Device Control register, sending an ~~Error~~error Message. In the context of the Root Error Command register, signaling an interrupt as a result of receiving an ~~Error~~error Message.

In Section 6.2.3.2.4, page 346, line 14, make the following edit:

"Advisory Non-Fatal Error" cases are predominantly determined by the role of the detecting agent (Requester, Completer, or Receiver) and the specific error. In such cases, an agent with AER signals the non-fatal error (if enabled) by sending an ERR_COR Message as an advisory to software, instead of sending ERR_NONFATAL. An agent without AER sends no ~~Error~~error Message for these cases, since software receiving ERR_COR would be unable to distinguish Advisory Non-Fatal Error cases from the correctable error cases used to assess Link integrity.

In Section 6.2.3.2.4.1, page 346, line 30, make the following edit:

A Completer generally sends a Completion with an Unsupported Request or Completer Abort (UR/CA) Status to signal a uncorrectable error for a Non-Posted Request. If the severity of the UR/CA error is non-fatal, the Completer must handle this case as an Advisory Non-Fatal Error. A Completer with AER signals the non-fatal error (if enabled) by sending an ERR_COR Message. A Completer without AER sends no ~~Error~~error Message for this case.

In Section 6.2.3.2.4.2, page 347, line 8, make the following edit:

When a Receiver that's not serving as the ultimate PCI Express destination for a TLP detects a non-fatal error with the TLP, this "intermediate" Receiver must handle this case as an Advisory Non-Fatal Error. A Receiver with AER signals the error (if enabled) by sending an ERR_COR Message. A Receiver without AER sends no ~~Error~~error Message for this case. An exception to the intermediate Receiver case for Root Complexes (RCs) is noted below.

In Section 6.2.3.2.4.3, page 347, line 27, make the following edit:

When a poisoned TLP is received by its ultimate PCI Express destination, if the severity is non-fatal and the Receiver deals with the poisoned data in a manner that permits continued operation, the Receiver must handle this case as an Advisory Non-Fatal Error. A Receiver with AER signals the error (if enabled) by sending an ERR_COR Message. A Receiver without AER sends no ~~Error~~error Message for this case. Refer to Section 2.7.2.2 for special rules that apply for poisoned Memory Write Requests.

In Section 6.2.3.2.4.4, page 348, line 16, make the following edit:

If the severity of the Completion Timeout is non-fatal, and the Requester elects to attempt recovery by issuing a new request, the Requester must first handle the current error case as an Advisory Non-Fatal Error. A Requester with AER signals the error (if enabled) by sending an ERR_COR Message. A Requester without AER sends no ~~Error~~error Message for this case.

In Section 6.2.3.2.4.5, page 348, line 23, make the following edit:

When a Receiver receives an unexpected Completion and the severity of the Unexpected Completion error is non-fatal, the Receiver must handle this case as an Advisory Non-Fatal Error . A Receiver with AER signals the error (if enabled) by sending an ERR_COR Message. A Receiver without AER sends no ~~Error~~error Message for this case.

In Section 6.2.4.3, page 352, lines 8, 11, and 19, make the following edits:

Section 6.2.3.2.4 describes Advisory Non-Fatal Error cases, under which an agent with AER detecting an uncorrectable error of non-fatal severity signals the error (if enabled) using ERR_COR instead of ERR_NONFATAL. For the same cases, an agent without AER sends no ~~Error~~error Message. The remaining discussion in this section is in the context of agents that do implement AER.

For Advisory Non-Fatal Error cases, since an uncorrectable error is signaled using the correctable ~~Error~~error Message, control/status/mask bits involving both uncorrectable and correctable errors apply. Figure 6-2 shows a flowchart of the sequence. Following are some of the unique aspects for logging Advisory Non-Fatal Errors.

First, the uncorrectable error needs to be of severity non-fatal, as determined by the associated bit in the Uncorrectable Error Severity register. If the severity is fatal, the error does not qualify as an Advisory Non-Fatal Error, and will be signaled (if enabled) with ERR_FATAL.

Next, the specific error case needs to be one of the Advisory Non-Fatal Error cases documented in Section 6.2.3.2.4. If not, the error does not qualify as an Advisory Non-Fatal Error, and will be

signaled (if enabled) with an uncorrectable ~~Error~~error Message.

In Section 7.8.4, page 450, Table 7-12, make the following edit:

Bit Location	Register Description	Attributes
3	**Unsupported Request Reporting Enable** – This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending ~~Error~~error Messages (see Section 6.2.5 and Section 6.2.6 for details). For a multi-Function device, this bit controls error reporting for each Function from point-of-view of the respective Function. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.	RW

In Section 7.10.3, page 498, line 2, make the following edit:

The Uncorrectable Error Mask register controls reporting of individual errors by the device Function to the PCI Express Root Complex via a PCI Express ~~Error~~error Message. A masked error (respective bit Set in the mask register) is not logged in the Header Log register, does not update the First Error Pointer, and is not reported to the PCI Express Root Complex by this Function. Refer to Section 6.2 for further details. There is a mask bit per error bit of the Uncorrectable Error Status register. Register fields for bits not implemented by the Function are hardwired to 0b. Figure 7-33 details the allocation of register fields of the Uncorrectable Error Mask register; Table 7-30 provides the respective bit definitions.

In Section 7.10.6, page 502, line 2, make the following edit:

The Correctable Error Mask register controls reporting of individual correctable errors by this Function to the PCI Express Root Complex via a PCI Express ~~Error~~error Message. A masked error (respective bit Set in the mask register) is not reported to the PCI Express Root Complex by this Function. Refer to Section 6.2 for further details. There is a mask bit per error bit in the Correctable Error Status register. Figure 7-36 details the allocation of register fields of the Correctable Error Mask register; Table 7-33 provides the respective bit definitions.

C39 Atomic Operations ECN

In the *Atomic Operations ECN*, page 21, line 10 make following edit:

The AtomicOp Routing Supported bit must be Set for any Root Port that supports forwarding of AtomicOp Requests initiated by host software or Root Complex ~~Internal~~Integrated Endpoints. The AtomicOp Routing Supported bit must be Set for any Root Ports that support forwarding of AtomicOp Requests received on their Ingress Port to Root Complex Integrated Endpoints.

C40 Latency Tolerance Reporting ECN

In the *Latency Tolerance Reporting ECN*, page 7, line 26 make following edit:

It is recommended that Endpoints buffer Requests as much as possible, and then use the full Link bandwidth in bursts that are as long as the Endpoint can practically support, as this will generally lead to the best overall platform power efficiency.

C41 Capitalization of Upstream Port

In Section 7.8.1, page 466, Table 7-15, make the following edit:

Table 7-15: Link Control Register

Bit Location	Register Description	Attributes
9	**Hardware Autonomous Width Disable** – When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. For a Multi-Function device associated with an Uupstream Pport, the bit in Function 0 is of type RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Components that do not implement the ability autonomously to change Link width are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	RW/RsvdP (see description)