1. PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	PCIe BGA SSD 11.5x13 ECN
DATE:	January 25, 2017
AFFECTED DOCUMENT:	PCI Express M.2 Specification, Revision 1.1
SPONSOR:	HP, Intel, Lenovo, Micron, Samsung, SanDisk, Seagate, Toshiba

Part I

1.1. Summary of the Functional Changes

This proposal adds a new 11.5 mm x 13 mm PCIe BGA SSD form factor to the M.2 v1.1 specification.

1.2. Benefits as a Result of the Changes

Platform area savings (are able to benefit from increased battery size in turn), better thermals, lower z-height, support for lower signaling voltages aligning with industry current and future trends. This allows PCI Express interface usage in small form-factor designs.

1.3. Assessment of the Impact

The 11.5 mm x13 mm form factor has no direct effect on other M.2 form factors. It does, however, update the Type 1620 BGA SSD ball map with symbolic names (PWR_1/2/3) for the power rails pins, and allows new optional voltages, defined for the 11.5 mm x 13 mm, to be assigned to those pins on the Type 1620. It also fully defines the LED_1# signal for BGA SSDs, where previously the signal was present on the ball map, but was not fully defined.

1.4. Analysis of the Hardware Implications

New BGA form-factor and footprints defined for soldered-down BGA SSD.

1.5. Analysis of the Software Implications

N/A.

1.6. Analysis of the C&I Test Implications

N/A.

[Editor's note: Existing M.2 v1.1 text is black. New text is marked in blue with underscore. Material to be deleted ~~is red with strikethrough~~.]

2

2. Mechanical Specification

2.1. Overview

This specification defines a family of M.2 modules and the corresponding system interconnects based on a 75 position edge card connection scheme or a derivation of the card edge and a soldered-down scheme for system interfaces.

The M.2 family comprised of several module sizes and designated by the following names (see Figure 2):

- Type 1113
- Type 1216
- Type 1620
- Type 1630
- Type 2024
- Type 2226
- Type 2228
- Type 2230
- Type 2242
- Type 2260
- Type 2280
- Type 2828
- Type 3026
- Type 3030
- Type 3042
- Type 22110

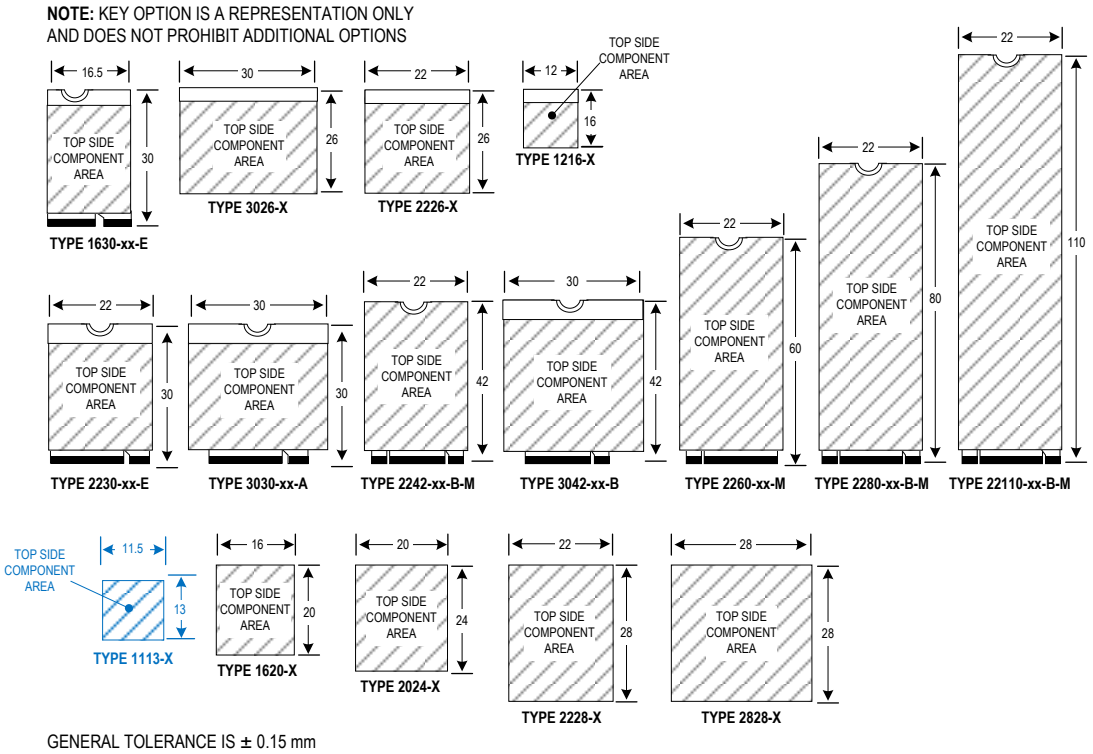


Figure 2. M.2 Family of Form Factors

The majority of M.2 types are connectorized using an edge connection scheme that can be either a single-sided or double-sided assembly. There will be several component Z-height options defined in this specification. The type of edge connector will cater to different platform Z-height requirements. In all cases, the board thickness is 0.8 mm ±10%. The T~~t~~ype 1216, T~~t~~ype 2226, and T~~t~~ype 3026~~are unique as they~~ are soldered down solutions that will have an LGA pattern on the back. Therefore, they can only be single-sided and the board thickness does not need to adhere to the 0.8 mm ±10% requirement. The Type 1113, Type 1620, Type 2024, Type 2228 and Type 2828 are soldered-down solutions that have BGA pattern on the back and are defined for BGA SSDs. These BGA solutions can be placed directly on host platforms as standalone BGA SSDs (see section 3.4 for the interface specification). Some BGA types can also be mounted on SSD Socket 2 or SSD Socket 3 modules (see sections 3.2 and 3.3 for interface specification). When a BGA SSD is mounted on SSD Socket 2 or SSD Socket 3 modules, the module is responsible for implementing the voltage conversion circuitry to provide the voltages ~~1.8 V and 1.2 V as~~ required.

The connectorized types include ~~edge connector requires~~ a mechanical key for accurate alignment. The location of the mechanical key along the Gold Finger contacts will make each key unique per a given socket connector. This prevents wrongful insertion of an incompatible board which prevents a safety hazard.

The board type, the type of assembly, the component Z-heights on top and bottom, and the mechanical key will make up the M.2 board naming convention detailed in the next section.

2.2. Card Type Naming Convention

Since there are various types of M.2 solutions and configurations, a standard naming convention will be employed to define the main features of a specific solution.

The naming convention will identify the following:

- The module size (width & length, both rounded down to remove any fraction)
- The component assembly maximum Z-height for the top and bottom sides of the module
- The Mechanical Connector Key/Module key location/assignment or multiple locations/assignments

These naming conventions will clearly define the module functionality, what connector it coincides with, and what Z-heights are met. Figure 3 diagrams the naming convention.

The module width options are: 11.5 mm, 12 mm, 16 mm, 16.5 mm, 20 mm, 22 mm, 28 mm, and 30 mm.

The module length can scale to various lengths to support the content and expand as the content increases. The lengths supported are: 13 mm, 16 mm, 20 mm, 24 mm, 26 mm, 28 mm, 30 mm, 42 mm, 60 mm, 80 mm, and 110 mm.

Together these two dimensions make up the first part of the module type definition portion of the module name.

The next part of the name describes whether the module is single-sided or double-sided and a secondary definition of what are the maximum Z-heights of the components on the top and bottom side of the module. Here we have specific Z-height limits that are either 2.0 mm, 1.75 mm, 1.5 mm, 1.35 mm, or 1.2 mm on the top-side and 1.5 mm, 1.35 mm, 0.7 mm and 0 mm on the bottom side. The letter S will designate Single-sided and the letter D will designate Double-sided. This will be complimented with a number that designates the specific Z-height combination option.

The last section of the name will designate the mechanical connector key/module key name and the coinciding pin location. These will be designated by a letter from A to M. In cases where the module will have a dual key scheme to enable insertion of the module into two different keyed sockets, a second letter will be added to designate the second mechanical connector key/module key.

Key ID assignment must be approved by the PCI-SIG. Unauthorized Key IDs would render the modules incompatible with the M.2 specification.

Figure 4 on the following page shows an example of module Type 2242 – D2 – B – M.

Module Nomenclature
Sample Type 2242-D2-B-M

Type XX XX – XX – X - X*

Width (mm)
11
12
16
20
22
28
30

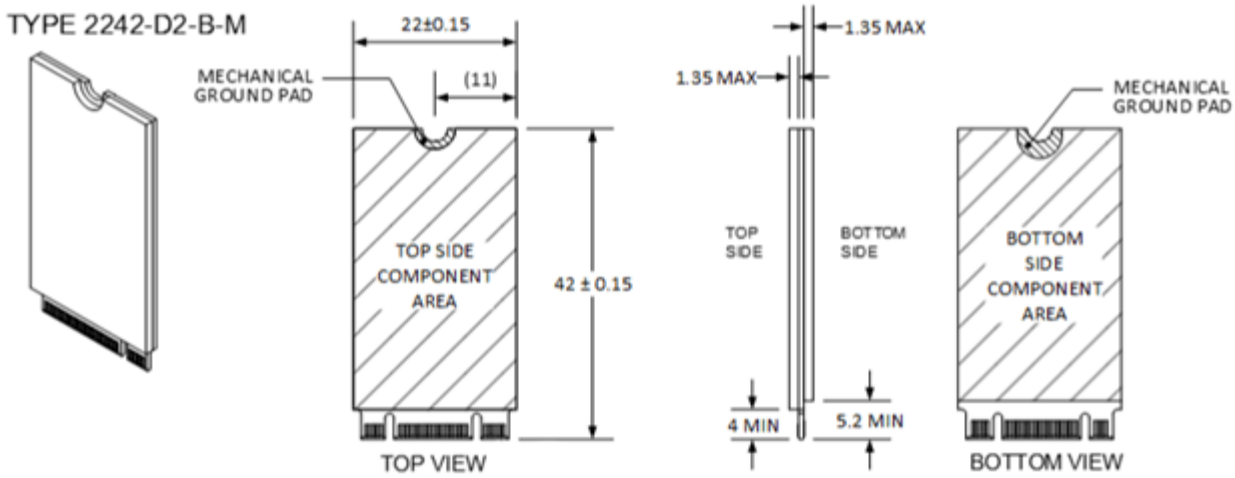
Length (mm)
13
15
20
24
26
28
30
42
60
80
110

Label**	Component Max Ht (mm)	
	Top Max	Bottom Max
S1	1.2(1)	0****
S2	1.35(1)	0****
S3	1.5(1)	0****
S4	1.75(1)	0****
S5	2.0(1)	0****
D1	1.2	1.35
D2	1.35	1.35
D3	1.5	1.35
D4	1.5	0.7
D5	1.5	1.5

Key ID	Pin	Interface
A	8-15	2x PCIe x1/USB 2.0/I2C/DP x4
B	12-19	PCIe x2/SATA/USB 2.0/USB 3.0/HSIC/SSIC/Audio/UIM/I2C/SMBus
C	16-23	PCIe/M-PCIe/USB 2.0/USB 3.0/SSIC/I2C-SlimBus/UIM/ANTCTL
D	20-27	Reserved for Future Use
E	24-31	2x PCIe x1/USB 2.0/I2C/SDIO/UART/PCM
F	28-35	Future Memory Interface (FMI)
G	39-46	Generic (Not used for M.2)***
H	43-50	Reserved for Future Use
J	47-54	Reserved for Future Use
K	51-58	Reserved for Future Use
L	55-62	Reserved for Future Use
M	59-66	PCIe x4/SATA/SMBus

* Use ONLY when a double slot is being specified.
** Label included in height dimension.
*** Key G is intended for customer use. Devices with this key will not be M.2 compliant. Use at your own risk.
**** Insulating label allowed on connector-based designs
(1) For BGA SSD, Max Height is measured with solder balls collapsed and is valid whether BGA is located directly on a platform or mounted on a module board

Figure 3. M.2 Naming Nomenclature



Note: For card-edge details, see section 2.3.4, Card PCB Details

Figure 4. Example of Type 2242-D2-B-M Nomenclature

The board is 22 mm x 42 mm, Double-sided with a maximum Z-height of 1.35 mm on both the Top and Bottom, and it has two mechanical connector keys/module keys at locations B and M which will enable it to plug into two types of connectors (Key B or Key M).

Table 1 shows the various options for board configurations as a function of the Socket, Module Function, and Module size.

Type 1113, Type 1216, Type 1620, Type 2024, Type 2226, Type 2228, Type 2828, and Type 3026 are ~~unique as they are~~ Soldered-Down solutions while all the others are connectorized with a PCB Gold Finger layout that coincides with an Edge Card connector. The Soldered-Down solutions do not have mechanical keys and their pinout configuration needs to be specifically called out.

Table 1. Optional Module Configurations

	Soldered-down			Connectorized			
	Type	Module Height Options	Pinouts Key	Connector Key	Type	Module Height Options	Module Key
Socket 1 Connectivity	1216	S1, S3	E	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	A, E	1630	S1, D1, S3, D3, D4	A, E, A+E
	2226	S1, S3	E	A, E	2230	S1, D1, S3, D3, D4	A, E, A+E
	3026	S1, S3	A+E	A, E	3030	S1, D1, S3, D3, D4	A, E, A+E
Socket 2 WWAN/ Other	N/A	N/A	N/A	B, C	3042	S1, D1, S3, D3, D4	B, C
	N/A	N/A	N/A	B, C	2242	S1, D1, S3, D3, D4	B, C
Socket 2 SSD/Other	N/A	N/A	N/A	B	2230	S2, D2, S3, D3, D5, S4, S5	B+M
	N/A	N/A	N/A	B	2242	S2, D2, S3, D3, D5, S4, S5	B+M
	N/A	N/A	N/A	B	2260	S2, D2, S3, D3, D5, S4, S5	B+M
	N/A	N/A	N/A	B	2280	S2, D2, S3, D3, D5, S4, S5	B+M
	N/A	N/A	N/A	B	22110	S2, D2, S3, D3, D5, S4, S5	B+M
	1113	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	1620	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2024	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2228	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2828	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
Socket 3 SSD Drive	N/A	N/A	N/A	M	2230	S2, D2, S3, D3, D5, S4, S5	M, B+M
	N/A	N/A	N/A	M	2242	S2, D2, S3, D3, D5, S4, S5	M, B+M
	N/A	N/A	N/A	M	2260	S2, D2, S3, D3, D5, S4, S5	M, B+M
	N/A	N/A	N/A	M	2280	S2, D2, S3, D3, D5, S4, S5	M, B+M
	N/A	N/A	N/A	M	22110	S2, D2, S3, D3, D5, S4, S5	M, B+M
	1113	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	1620	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2024	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2228	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2828	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A

2.3. Card Specifications

There are multiple defined card outlines. Card thickness is fixed at 0.8 mm ±10% with optional increased/decreased XY dimensions so as to incorporate more or less functionality on the board.

For purposes of the drawings in this specification, the following notes apply:

- All dimensions are in millimeters (mm), unless otherwise specified
- All dimension tolerances are ± 0.15 mm, unless otherwise specified
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads
- The board/module has a 4 mm tall strip at the lower end of the board intended to support the Gold Finger pads used in conjunction with an Edge Card connector. The Gold Fingers appear on both top and bottom side of the board/module PCB
- In some configuration, the board/module has a 3.8 mm strip intended to support RF connectors
- All connectorized versions have a mounting/retention screw (half-moon cutout) at the upper end of the board/module used to hold down the board onto the Motherboard or chassis
- The remainder of the board area available is intended for Active Components but not limited to this. Encroachment into this area can be done if extra area is needed for additional RF antenna connectors
- The diagrams showing mechanical connector key/module key locations in this document are for example only. Actual Key location/definition is part of the actual module name per the naming convention
- General Tolerance Summary as given in Table 2

Table 2. General Tolerance

	+ Plus	– Minus
PCB Size Tolerance	0.15 mm	0.15 mm
PCB Thickness	0.08 mm	0.08 mm
Bevel Capabilities	0.25 mm	0.25 mm
Drill Capabilities for Module key	0.05 mm	0.05 mm

2.3.6. Soldered-Down Form Factors for BGA SSDs

Following different sizes are defined for the soldered-down BGA SSDs:

- Type 1113
- Type 1620
- Type 2024
- Type 2228
- Type 2828

All these types are soldered-down and single-sided. They have a BGA land pattern on the backside.

To help prevent module-warp, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (for example, outer-to-outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

The target differential impedance of the PCIe and SATA signals on the package is 85Ω. Differential coupling from other signals must be reduced to ensure signal integrity of the differential pair.

[Editor's note: Insert the following section before Section 2.3.6.1, and adjust all subsequent section and figure numbers.]

2.3.6.1. Type 1113 Specification

The BGA package size of 11.5 mm x 13 mm contains the ball map for Type 1113.

Figure xx shows the mechanical outline drawing for BGA Type 1113 and Figure yy shows a recommended land pattern for the Type 1113 package. The dimensions shown in Figure yy are nominal.

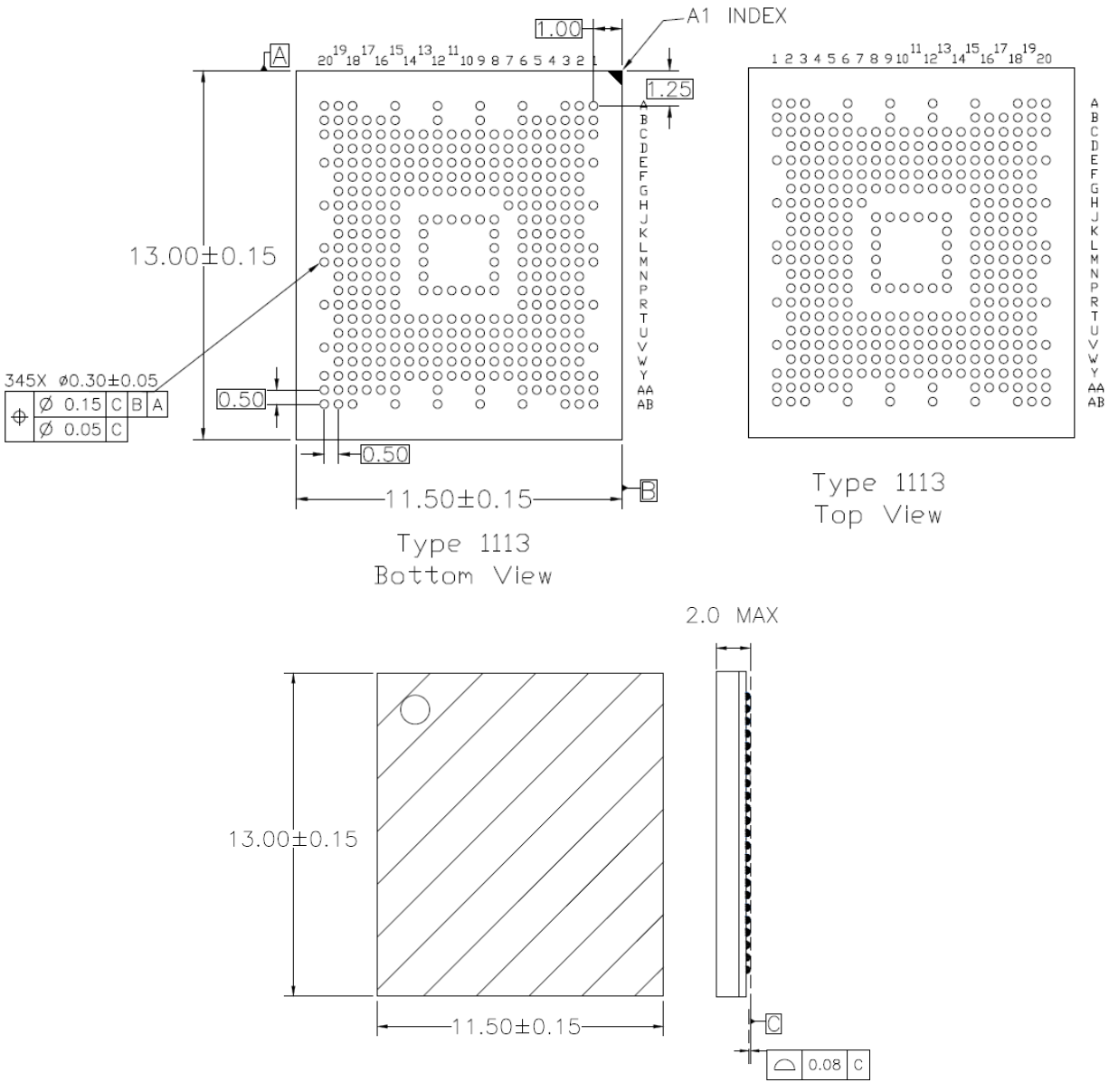


Figure xx M.2 Type 1113 S5 Mechanical Outline Drawing Example

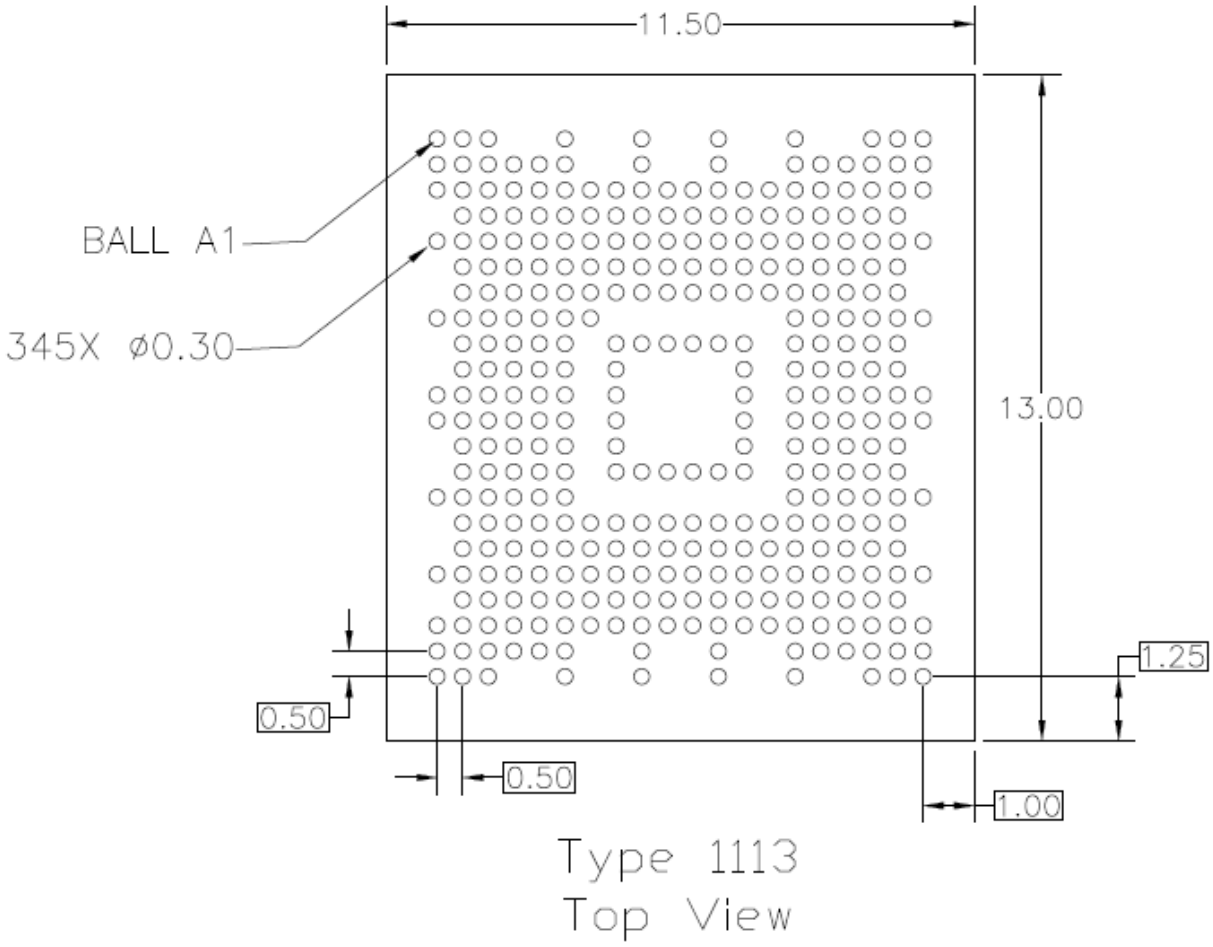


Figure yy Recommended Land Pattern for M.2 Type 1113 BGA (Top View)

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3.4 BGA SSD Interface Signals

Table and

Interface	Signal Name	I/O	Function	Voltage
Power and Grounds	~~+3.3 V~~PWR_1[1] (8 pins)	I	+3.3 V source	~~3.3 V~~
	~~+1.8 V~~PWR_2[1] (12 pins)	I	+1.8 V or +1.2 V source	~~1.8 V~~
	~~+1.2 V~~PWR_3[1] (12 pins)	I	+1.2 V, +1.1 V, or +0.9 V source	~~1.2 V~~
	GND (106 pins)		Return current path	~~0 V~~
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Card Electromechanical Specification*.	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Card Electromechanical Specification*. **Note:** This reference clock is the common ref clock that shall be used with PCIe.	
	PERST#	I	PE-Reset is a functional reset to the card as defined by the *PCI Express Mini Card Electromechanical Specification*.	1.8 V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Mini Card Electromechanical Specification*; Also used by L1 PM Substates.	1.8 V
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on platform. Active Low when used as PEWAKE#. When the add-in module supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the add-in module supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	1.8 V
SATA	SATA-A+, SATA-A-/ SATA-B+, SATA-B-	I/O	Refer to *Serial ATA Specification*.	
	DEVSLP	I		
	DAS/DSS#	I/O		

Interface	Signal Name	I/O	Function	Voltage
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input provided by the Platform chipset to reduce power and cost for the module. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	1.8 V
	PEDET	O	Host interface Indication; To be grounded for SATA, No Connect for PCIe.	0 V or NC
	LED_1#	O	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.	3.3 V
	RFU		Reserved for future use.	
	DNU		Do not use. Manufacturing purpose only.	
SSD Specific Optional Signals	XTAL_IN	I	Connection to crystal unit.	
	XTAL_OUT	O	Connection to crystal unit.	
	CAL_P	N/A	PHY calibration resistor.	
	RZQ_1, RZQ_2	N/A	Memory or NAND calibration resistor.	
	JTAG_TRST#	I	Refer to JTAG *Specification (IEEE 1149.1), Test Access Port and Boundary Scan Architecture* for definition of these balls.	3.3 V
	JTAG_TCK	I		
	JTAG_TMS	I		
	JTAG_TDI	I		
	JTAG_TD0	O		
	SMB_CLK	I/O	SMBus Clock, Open Drain with pull up on platform.	1.8 V
	SMB_DATA	I/O	SMBus Data, Open Drain with pull up on platform.	1.8 V
	ALERT#	O	Alert notification to master; Open Drain with pull up on platform; Active Low.	1.8 V
	DIAG0, DIAG1	I/O	Engineering test mode balls have been specified to allow for special access to DIAG for debug purposes.	

[1] The voltage sources are given symbolic names to allow a choice of voltages for the power rails. In earlier revisions of this specification the voltage sources for Types 1620, 2024, 2028, and 2828 were defined as fixed values. Henceforth, the voltage sources are given symbolic names, allowing a choice of voltages for each of the mandatory power rails.

[Editor's note: Inserting the following new table will require adjusting all subsequent table numbers.]

Table contain a list of the signals defined for BGA SSDs. The I/O direction indicated is from BGA module's perspective.

Table 39. BGA SSD System Interface Signal Table for Types 1620, 2024, 2228, and 2828

Interface	Signal Name	I/O	Function	Voltage
Power and Grounds	~~+3.3 V~~PWR_1[1] (8 pins)	I	+3.3 V source	~~3.3 V~~
	~~+1.8 V~~PWR_2[1] (12 pins)	I	+1.8 V or +1.2 V source	~~1.8 V~~
	~~+1.2 V~~PWR_3[1] (12 pins)	I	+1.2 V, +1.1 V, or +0.9 V source	~~1.2 V~~
	GND (106 pins)		Return current path	~~0 V~~
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Card Electromechanical Specification*.	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Card Electromechanical Specification*. **Note:** This reference clock is the common ref clock that shall be used with PCIe.	
	PERST#	I	PE-Reset is a functional reset to the card as defined by the *PCI Express Mini Card Electromechanical Specification*.	1.8 V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Mini Card Electromechanical Specification*; Also used by L1 PM Substates.	1.8 V
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on platform. Active Low when used as PEWAKE#. When the add-in module supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the add-in module supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	1.8 V
SATA	SATA-A+, SATA-A-/ SATA-B+, SATA-B-	I/O	Refer to *Serial ATA Specification*.	
	DEVSLP	I		
	DAS/DSS#	I/O		
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input provided by the Platform chipset to reduce power and cost for the module. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	1.8 V
	PEDET	O	Host interface Indication; To be grounded for SATA, No Connect for PCIe.	0 V or NC
	LED_1#	O	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.	3.3 V
	RFU		Reserved for future use.	
	DNU		Do not use. Manufacturing purpose only.	
SSD Specific	XTAL_IN	I	Connection to crystal unit.	
	XTAL_OUT	O	Connection to crystal unit.	

Interface	Signal Name	I/O	Function	Voltage
Optional Signals	CAL_P	N/A	PHY calibration resistor.	
	RZQ_1, RZQ_2	N/A	Memory or NAND calibration resistor.	
	JTAG_TRST#	I	Refer to JTAG *Specification (IEEE 1149.1), Test Access Port and Boundary Scan Architecture* for definition of these balls.	3.3 V
	JTAG_TCK	I		
	JTAG_TMS	I		
	JTAG_TDI	I		
	JTAG_TD0	O		
	SMB_CLK	I/O	SMBus Clock, Open Drain with pull up on platform.	1.8 V
	SMB_DATA	I/O	SMBus Data, Open Drain with pull up on platform.	1.8 V
	ALERT#	O	Alert notification to master; Open Drain with pull up on platform; Active Low.	1.8 V
	DIAG0, DIAG1	I/O	Engineering test mode balls have been specified to allow for special access to DIAG for debug purposes.	

[1] The voltage sources are given symbolic names to allow a choice of voltages for the power rails. In earlier revisions of this specification the voltage sources for Types 1620, 2024, 2028, and 2828 were defined as fixed values. Henceforth, the voltage sources are given symbolic names, allowing a choice of voltages for each of the mandatory power rails.

[Editor's note: Inserting the following new table will require adjusting all subsequent table numbers.]

Table 39a. BGA SSD System Interface Signal Table for Type 1113

Interface	Signal Name	I/O	Function	Voltage
Power and Grounds	PWR_1 (10 pins)	I	+3.3 V supply	
	PWR_2 (20 pins)	I	+1.2 V or +1.8 V supply	
	PWR_3 (10 pins)	I	+0.9 V, +1.1 V, or +1.2 V supply	
	GND (115 pins)		Return current path	
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Card Electromechanical Specification.*	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Card Electromechanical Specification.* **Note**: This reference clock is the common ref clock that shall be used with PCIe.	
	PERST#	I	PE-Reset is a functional reset to the card as defined by the *PCI Express Mini Card Electromechanical Specification*.	1.8 V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Mini Card Electromechanical Specification*; also used by L1 PM Substates.	1.8 V

Interface	Signal Name	I/O	Function	Voltage
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on platform. Active Low when used as PEWAKE#. When the add-in module supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the add-in module supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	1.8 V
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input provided by the platform chipset to reduce power and cost for the module. SUSCLK has a duty cycle that is able to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	1.8 V
	LED_1#	O	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.	3.3 V
	RFU		Reserved for future use.	
	DNU		Do not use. Manufacturing purpose only.	
	HSB		Host specific balls.	
SSD Specific Optional Signals	XTAL_IN	I	Connection to crystal unit.	N/A
	XTAL_OUT	O	Connection to crystal unit.	N/A
	CAL_P	N/A	PCIe PHY calibration resistor.	N/A
	RZQ_1, RZQ_2	N/A	Memory or NAND calibration resistor.	N/A
	JTAG_TRST#	I	Refer to JTAG *Specification (IEEE 1149.1), Test Access Port and Boundary Scan Architecture* for definition of these balls.	3.3 V
	JTAG_TCK	I		
	JTAG_TMS	I		
	JTAG_TDI	I		
	JTAG_TDO	O		
	SMB_CLK	I/O	SMBus Clock, Open Drain with pull up on platform.	1.8 V
	SMB_DATA	I/O	SMBus Data, Open Drain with pull up on platform.	1.8 V
	ALERT#	O	Alert notification to master; Open Drain with pull up on platform; Active Low.	1.8 V
	DIAG0, DIAG1	I/O	Engineering test mode balls have been specified to allow for special access to DIAG for debug purposes.	
	WP_L	I	Write protect signal to prevent writes from occurring to SPI NOR. Active low.	1.8 V
	SPI_CLK	I	SPI clock. Max frequency is 50 MHz.	1.8 V
	SPI_MOSI	I	Master Out Slave In signal for SPI NOR.	1.8 V
	SPI_MISO	O	Master In Slave Out signal for SPI NOR	1.8 V
	SPI_CS_L	I	Chip select for SPI NOR. Active low.	1.8 V

Interface	Signal Name	I/O	Function	Voltage
	SPI_18	I	+1.8 V supply. Optional voltage supply if SPI NOR included in package.	1.8 V
	REG_01	N/A	Connection to internal power rail. Value and usage is vendor specific.	N/A
	REG_02	N/A	Connection to internal power rail. Value and usage is vendor specific.	N/A
	REG_03	N/A	Connection to internal power rail. Value and usage is vendor specific.	N/A

3.4.1. ~~BGA SSD Specific~~ Power Sources and Grounds

In the BGA SSD, ~~there is provision for eight 3.3 V, twelve 1.8 V, twelve 1.2 V, and 104 GND balls. Each~~ the PWR_1, PWR_2, PWR_3, and GND balls shall tolerate a continuous load of up to 200 mA.

For Type 1113 only, the optional balls REG_01, REG_02, and REG_03 are for devices that require external components for voltage regulation inside the device. Values and components are defined by the device vendor.

Note: While the maximum current that is possible to be passed to the BGA may be calculated by multiplying the number of power pins by 200 mA, actual power system requirements will be determined between the platform and BGA SSD vendors.

3.4.2. PCI Express Interface

The PCI Express interface supported in BGA SSD is a two Lane interface for Type 1113, and a four Lane interface for the other BGA module types. See Section 3.3.2 for a detailed description of the PCIe signals.

3.4.2.1. PERST#, CLKREQ#, PEWAKE#

Definitions for these signals are the same as that in section 3.1.3, except that these signals are defined to be at signal levels of 1.8 V

See section 3.3.2 in this specification for a detailed description of the remaining PCIe signals.

3.4.3. SATA Interface (Informative)

SATA signals are not supported for Type 1113. For other BGA module types, see Section 3.3.3 for a detailed description of the SATA signals.

3.4.4. SSD Specific Signals

3.4.4.1. SUSCLK

Definition for this signal is the same as that in section 3.1.12.1 ~~3.1.11.1, *UIM POWER SRC*~~ in this specification, except that this signal is defined to be at signal levels of 1.8 V.

3.4.4.2. PEDET

The interface detect can be used by the host computer to determine the communication protocol that the M.2 module uses; SATA signaling (low) or PCIe signaling (high) in conjunction with a platform located pull-up resistor.

Note: This signal is not applicable to Type 1113, which supports only the PCIe interface.

[Editor's note: Inserting the following new section before Section 3.4.4.3, and adjust all subsequent section and figure numbers.]

3.4.4.3. Status Indicator (LED_1#)

See section 3.1.12.2, Status Indicators, for a more detailed description of the LED_1# signal.

3.4.4.4. RFU

Signals documented as RFU are reserved for future use. These balls must be soldered to a Platform board, but must be electrically no-connect on the Host ~~or~~ and the Adapter. These balls are reserved for future assignment as a functional signal.

3.4.4.5. DNU (Do Not Use)

Signals documented as DNU are for manufacturing only. These balls must be soldered to a platform, but must be electrically no-connect on the host. Signals documented as DNU are for manufacturing only.

3.4.4.6. HSB (Host Specific Balls)

Signals documented as HSB are not defined as a functional signal. These balls must be soldered to a platform, but must be electrically no-connect on the adapter. A host's use of this signal is undefined.

3.4.5. SSD Specific Optional Signals

Note: Physical balls need to be present on the package for these signals even if they are not being implemented.

3.4.5.1. CAL_P

This signal is optional and is not required to be connected on the SSD BGA component and is not required to be implemented on the platform boards. It is used as impedance reference for controller calibration.

3.4.5.2. RZQ_1 and RZQ_2

These signals are optional and are not required to be connected on the SSD BGA component and are not required to be implemented on the platform boards. These signals can be used as impedance reference for calibrating DRAM or NAND memory interface.

3.4.5.3. XTAL_OUT

This signal is optional and is not required to be connected on the SSD BGA component and is not required to be implemented on the platform boards. It connects to optional crystal output from BGA SSD module. Crystal unit characteristics are vendor specific.

3.4.5.4. XTAL_IN

This signal is optional and is not required to be connected on the SSD BGA component and is not required to be implemented on the platform boards. It connects to optional crystal output from the platform. Crystal unit characteristics are vendor specific.

3.4.5.5. JTAG Signals

This group of signals is optional. It is not required to be connected on the SSD BGA component and is not required to be implemented on the platform boards. IEEE Standard 1149.1 specifies the rules and permissions for designing an 1149.1-compliant interface. Inclusion of a *Test Access Port* (TAP) on a module allows boundary scan to be used for testing of the module on which it is installed. The TAP is comprised of five signals (the JTAG_TRST# signal is optional within the set of JTAG signals) that are used to interface serially with a TAP controller within the BGA based SSD device. The module vendor must specify TDO drive strength.

3.4.5.6. SMBus Pins

ALERT#, SMB_DATA and SMB_CLK signals are optional and are not required to be connected on the SSD BGA component and are not required to be implemented on the platform boards.

3.4.5.6.1. ALERT#

For a description of this signal, see section 3.2.12.2.1.

3.4.5.6.2. SMB_DATA

For a description of this signal, see section 3.2.12.2.2.

3.4.5.6.3. SMB_CLK

For a description of this signal, see section 3.2.12.2.3.

3.4.5.7. DIAG0, DIAG1

The DIAG0 and DIAG1 signals are optional for engineering or production implementation, are not required to be present on the SSD BGA component, and are not required to be implemented on the platform boards.

3.4.5.8 Serial Peripheral Interface (SPI) Pins

The WP_L, SPI_CLK, SPI_MOSI, SPI_MISO, SPI_CS_L, and SPI_18 signals are optional and define an interface for an optional SPI storage device in the adapter. These signals are defined only for the Type 1113. The implementation and details of SPI is dependent on the vendor.

3.4.6. BGA SSD Soldered-Down Module Pin-out

All pinout tables in this section are written from the module point of view when referencing signal directions. This section contains the module-side pinout map for Type 1620 BGA module.

Figure 104 shows module-side ballmap for Type 1620 BGA.

Figure 105 shows Type 1620 BGA module-side ballmap surrounded by Type 2024, Type 2228, and Type 2828 module-side ballmaps (Top View). There are additional sizes of 20 mm x 24 mm, 22 mm x 28 mm, and 28 mm x 28 mm defined for BGA SSD. Ballmaps for ~~the~~ Types 2024, 2228, and 2828 ~~these sizes~~ have ~~encompass the Type1620 ballmap with~~ additional DNU balls for mechanical stability. See section 2.3.6, Soldered-Down Form Factors for BGA SSDs for details on the location of these DNU balls for various BGA package sizes.

Figure 105a shows the Type 1113 BGA ballmap.

Optional signals are shown in blue. The optional signals are CAL_P, XTAL_OUT, XTAL_IN, RZQ_1, RZQ_2, DIAG0, DIAG1, JTAG_TRST#, JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, SMB_CLK, SMB_DATA, ~~and~~ ALERT#, WP_L, SPI_CLK, SPI_MOSI, SPI_MISO, SPI_CS_L, SPI_18, REG_01, REG_02, and REG_03.

The optional signals are handled as follows for the host and module.

- Host:
  - If not implemented, the landing pads shall not be electrically connected to the host.
  - If implemented, the host routes the signals as described in this specification.
- Module
  - If not implemented, the balls shall not be electrically connected to the module.
  - If implemented, the module routes the signals as described in this specification.

[Editor's note: For reviewers of this ECR, the changes in the BGA ball-out tables for Types 1620, 2024, 2228, and 2828 are in the labeling of the cells describing the power rails (i.e., used to be specific voltages, and are now PWR_1, PWR_2, PWR_3.]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_ OUT	XTAL_ IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PERp0	SATA-A- /PERn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		GND	GND	DNU	DNU	DNU
H				SATA-B+ /PETp0	SATA-B- /PETn0		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		RFU	RFU			
J	GND	GND	GND	GND	GND		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		GND	GND	DNU	DNU	DNU
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_ TCK	JTAG_ TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		GND	GND	DNU	JTAG_ TDI	JTAG_ TDO
T				PETp2	PETn2		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		RFU	RFU			
U	GND	GND	GND	GND	GND		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		GND	GND	DNU	SMB_ CLK	SMB_ DATA
V				PERp3	PERn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED_1#/ DAS	RFU	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PETp3	PETn3	GND	DNU	DNU	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

= No Solder Ball

Figure 104. Type 1620 BGA Module-side Ballmap (Top View)

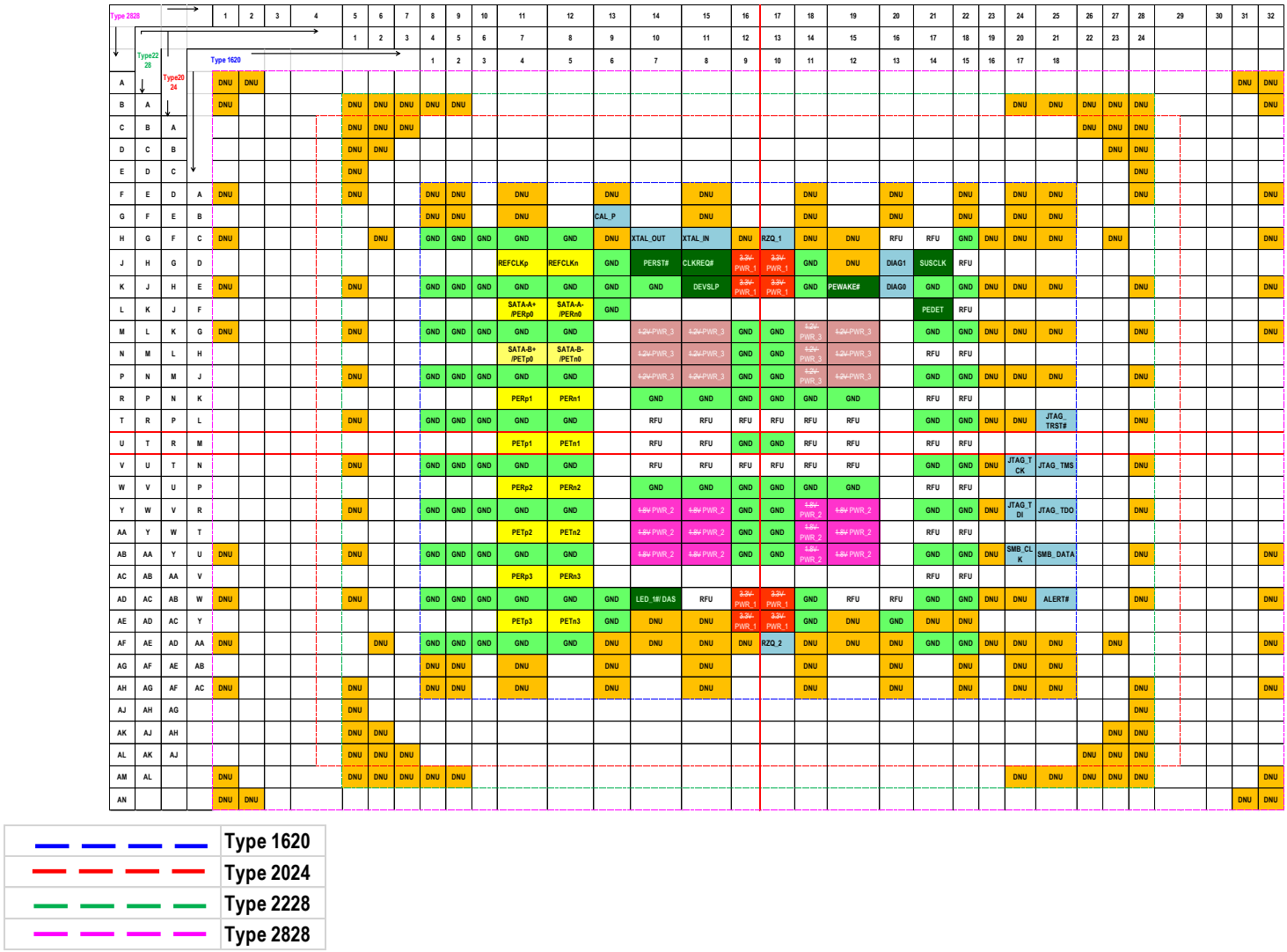
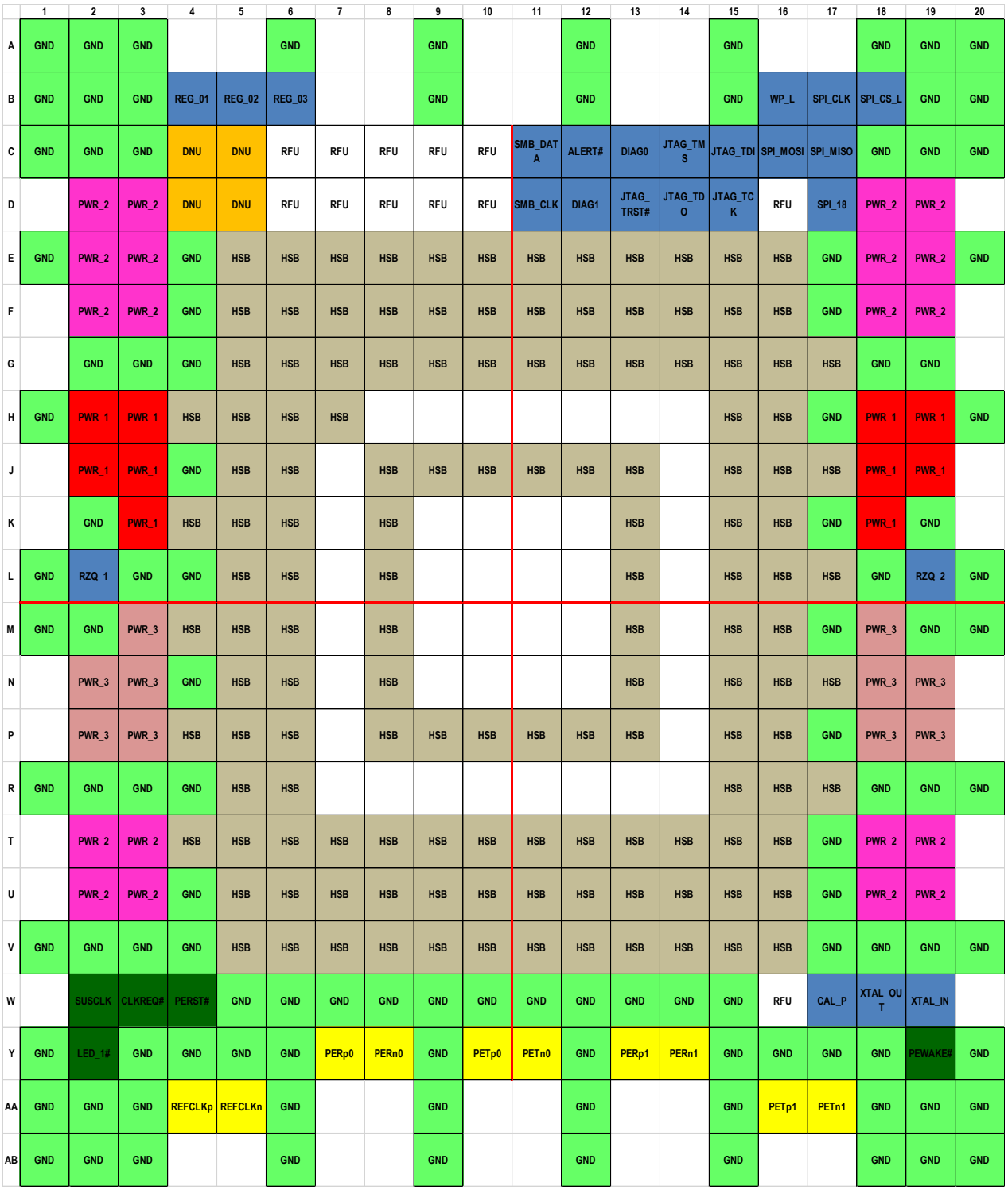


Figure 105. Type 1620 BGA Module-side Ballmap Surrounded by Type 2024, Type 2228, and Type 2828 Module-side Ballmaps (Top View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND
B	GND	GND	GND	REG_01	REG_02	REG_03			GND			GND			GND	WP_L	SPI_CLK	SPI_CS_L	GND	GND
C	GND	GND	GND	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_DATA	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPI_MOSI	SPI_MISO	GND	GND	GND
D		PWR_2	PWR_2	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPI_18	PWR_2	PWR_2	
E	GND	PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	GND
F		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	
H	GND	PWR_1	PWR_1	HSB	HSB	HSB	HSB								HSB	HSB	GND	PWR_1	PWR_1	GND
J		PWR_1	PWR_1	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	PWR_1	PWR_1	
K		GND	PWR_1	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_1	GND	
L	GND	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	GND
M	GND	GND	PWR_3	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	GND	GND
N		PWR_3	PWR_3	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	PWR_3	PWR_3	
P		PWR_3	PWR_3	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	PWR_3	PWR_3	
R	GND	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	GND
T		PWR_2	PWR_2	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
V	GND	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	GND
W		SUSCLK	CLKREQ#	PERST#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	CAL_P	XTAL_OUT	XTAL_IN	
Y	GND	LED_1#	GND	GND	GND	GND	PERp0	PERn0	GND	PETp0	PETn0	GND	PERp1	PERn1	GND	GND	GND	GND	PEWAKE#	GND
AA	GND	GND	GND	REFCLKp	REFCLKn	GND			GND			GND			GND	PETp1	PETn1	GND	GND	GND
AB	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND

Figure 105a. Type 1113 Module-side BGA Ballmap (Top View)

4

4. Electrical Requirements

4.3. Electrical Requirements for BGA SSDs

4.3.1. BGA SSD Voltage Supply Power-on Sequencing

The host should apply the following recommendations for sequencing the voltages on the ~~3.3 V~~ PWR_1 supply, the ~~1.8 V~~ PWR_2 supply, and the ~~1.2 V~~ PWR_3 supply during power-on:

- After the voltage on the ~~1.8 V~~ PWR_2 supply or the voltage on the ~~1.2 V~~ PWR_3 supply reach 300 mV, the voltage on the ~~1.8 V~~ PWR_2 supply should remain greater than the voltage on the ~~1.2 V~~ PWR_3 supply by at least 200 mV.
- The voltage on the ~~3.3 V~~ PWR_1 supply has no timing relationship relative to the voltage on the ~~1.2 V~~ PWR_3 supply or the voltage on the ~~1.8 V~~ PWR_2 supply.

If the power-on sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

Figure 106 shows three valid power-on ramp examples for the case where each of the power rails is assigned a different voltage. The 1st example shows PWR_2 reaching 300mV before PWR_3 reaches 100mV. The 2nd example shows PWR_2 well above 300mV by the time PWR_3 reaches 100mV. The 3rd case shows PWR_2 reaching 300mV at the same time as PWR_3. [Note: The PWR_1 rail is not shown since it has no timing relationship to the other rails.]

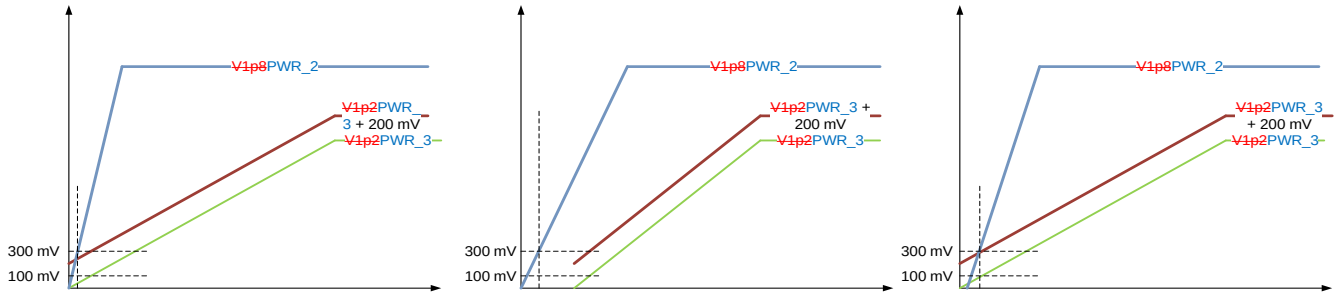


Figure 106. Power-on Sequencing

4.3.2. BGA SSD Voltage Supply Power-off Sequencing

The host should apply the following recommendations for sequencing the voltages on the 3.3 V PWR_1 supply, the 1.8 V PWR_2 supply, and the 1.2 V PWR_3 supply during power-off:

- Before the voltage on the 1.2 V PWR_3 supply and the voltage on the 1.8 V PWR_2 supply reach 300 mV, the voltage on the 1.8 V PWR_2 supply should remain greater than voltage on the 1.2 V PWR_3 supply by 200 mV.
- After both the voltage on the 1.8 V PWR_2 supply and the voltage on the 1.2 V PWR_3 supply are below 300 mV, there is no specified relationship between them.
- The voltage on the 3.3 V PWR_1 supply has no timing relationship relative to the voltage on the 1.2 V PWR_3 supply or the voltage on the 1.8 V PWR_2 supply.
- The voltage on all supplies should remain below 100 mV for at least 1 ms before the power-on sequence is restarted.

If the power-off sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

Figure 107 shows two valid power-off ramp examples for the case where each of the power rails is assigned a different voltage. [Note: The PWR_1 rail is not shown since it has no timing relationship to the other rails.]

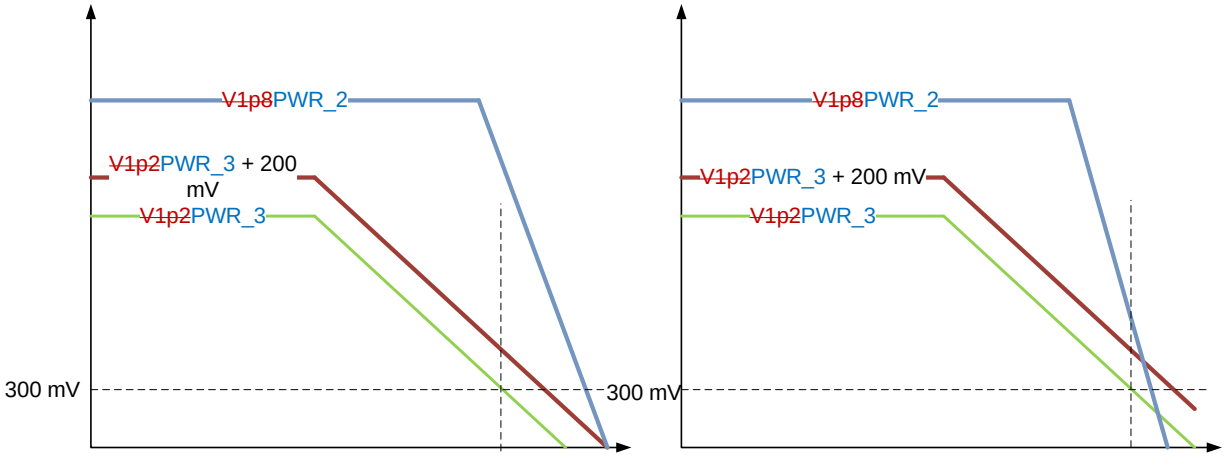


Figure 107. Power-off Sequence

4.3.3. BGA SSD Power Ramp Timing

The power ramp timing is defined as the time the power rail needs to ramp to a valid voltage (shown in Table 42). This timing is recommended for power-on only.

Table 42. Power Ramp Timing

Supply Voltage	Max*
3.3 V	35 ms
1.8 V	25 ms
1.2 V	20 ms
1.1 V	20 ms
0.9 V	20 ms
*The minimum tuning may be calculated from the maximum slew rate recommendation in Table 43.	

4.3.4. BGA SSD Power Rail Slew Rate

The maximum power rail slew rate is shown in Table 43. These values are only defined for ESD protection purpose. They are not meant for inrush current control.

Table 43. Power Rail Slew Rate

Symbol	Parameter	Max	Condition
$T_{SLEW\_3.3}$	Voltage slew rate of the 3.3 V power rail	100 kV/s	No Load
$T_{SLEW\_1.8}$	Voltage slew rate of the 1.8 V power rail	100 kV/s	No Load
$T_{SLEW\_1.2}$	Voltage slew rate of the 1.2 V power rail	100 kV/s	No Load
$T_{SLEW\_1.1}$	Voltage slew rate of the 1.1 V power rail	100 kV/s	No Load
$T_{SLEW\_0.9}$	Voltage slew rate of the 0.9 V power rail	100 kV/s	No Load

4.3.5. BGA SSD Power Rail Parameters

All supply voltages and tolerances referenced for BGA SSD devices in this specification are considered to be measured at the component ball or pin. Supply tolerances are assumed to incorporate any superposition of AC, DC and system transient effects measured at the component ball or pin.

Table XX describes the characteristics of the regulated power rails for BGA SSDs.

Table XX. Regulated Power Rail Parameters for BGA SSD Types

Nominal Voltage	Voltage Range	Platform Rail Type
+3.3 V	2.8 V to 3.6 V*	Always On
+1.8 V	1.7 V to 1.9 V	Always On
+1.2 V	1.14 V to 1.26 V	Always On
+1.1 V	1.06 V to 1.17 V	Always On
+0.9 V	0.86 V to 0.98 V	Always On
Note*: +3.3 V tolerance for BGA SSD differs from the tolerance in Table 44.		

4.4. Power

The M.2 module utilizes a single regulated power rail of 3.3 V provided by the platform. In some pinout variants, there is a dedicated VIO supply pin called VIO1.8V that is intended to only bias the I/O circuitry of the module. The main 3.3 V and the VIO voltage rail sources on the platform should always be on and available during the system's stand-by/suspend state to support the wake event processing on the communications card. Some NICs may require host (driver) intervention after a power-on.

The number of 3.3 V pins for any given pinout is determined by the maximum required instantaneous current typical of the solutions associated with each type of socket and the M.2 connector current handling capability per pin. The M.2 connector pin is defined as needing to support 500 mA/pin continuous. This yields the required number of power rail pins per pinout.

- Type 1630, intended for Socket 1, has two power pins allocated in the pinouts that supports up to 1 A continuous.
- Types 2230 and 3030, intended for Socket 1, have four power pins in their pinouts and can support up to 2 A continuous.
- The Socket 2 board types have five power pins in their pinouts and can support up to 2.5 A continuous.
- The Socket 3 board types, with a single Module Key, have nine power pins but can support up to 2.5 A continuous.
- The four extra power pins enable reduced IR drop for these devices.

The power rail voltage tolerance listed in Table 3 is ±5%. This is different from the ± 9% tolerance allowed in the Mini Card specification.

Note: Table 44 does not apply to BGA SSDs (see Table XX).

Table 3. Key Regulated Power Rail Parameters

Power Rail	Pin Name	Voltage Tolerance	Platform Rail Type
+3.3 V	3.3V	± 5%	Always On
+1.8 V	VIO1.8V	± 5.55%*	Always On
~~+1.2 V~~	~~1.2V~~	~~± 5%~~	~~Always On~~
~~+1.8 V~~	~~1.8V~~	~~± 5.55%~~	~~Always On~~

Note*: 1.7 V to 1.9 V Range

[Editor's note: This ECR moves the 1.2V and 1.8V levels into Table XX in section 4.3.5, since they were added solely for BGA SSD. The tolerances are also changed.]

5

5. Platform Socket Pinout and Key Definitions

All pinouts tables in this section are written from the platform/system point of view when referencing signal directions.

…

5.4. Soldered Down Pinouts Definitions

The soldered-down pinouts definitions are shown in the following figures:

- Figure 108, *Type 2226 LGA Pinout Using SDIO Based Socket 1 Pinout On Platform*
- Figure 109, *Type 1216 LGA Pinout Using SDIO Based Socket 1 Pinout On Platform*
- Figure 110, *Type 3026 LGA Pinout Using SDIO Based Socket 1 and Display Port Based Socket 1 Pinout On Platform*
- Figure 111, *Type 1620 BGA Socket Map Pinout On Platform (Top* View)
- Figure 112, *Type 1620, Type 2024, Type 2228, Type 2828 BGA Pinout On Platform Socket Map On Platform* (Top View)
- Figure

[Editor's note: For reviewers of this ECR, the changes in the BGA ball-out tables for Types 1620, 2024, 2228, and 2828 are in the labeling of the power rails (i.e., used to be specific voltages, and are now PWR_1, PWR_2, PWR_3.]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PETp0	SATA-A- /PETn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		GND	GND	DNU	DNU	DNU
H				SATA-B+/PERp0	SATA-B-/PERn0		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		RFU	RFU			
J	GND	GND	GND	GND	GND		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		GND	GND	DNU	DNU	DNU
K				PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PERp2	PERn2		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		RFU	RFU			
U	GND	GND	GND	GND	GND		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PETp3	PETn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED_1# / DAS	RFU	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PERp3	PERn3	GND	DNU	DNU	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

=> No solder ball

Figure 111. Type 1620 BGA Socket Map ~~Pinout~~ On Platform (Top View)

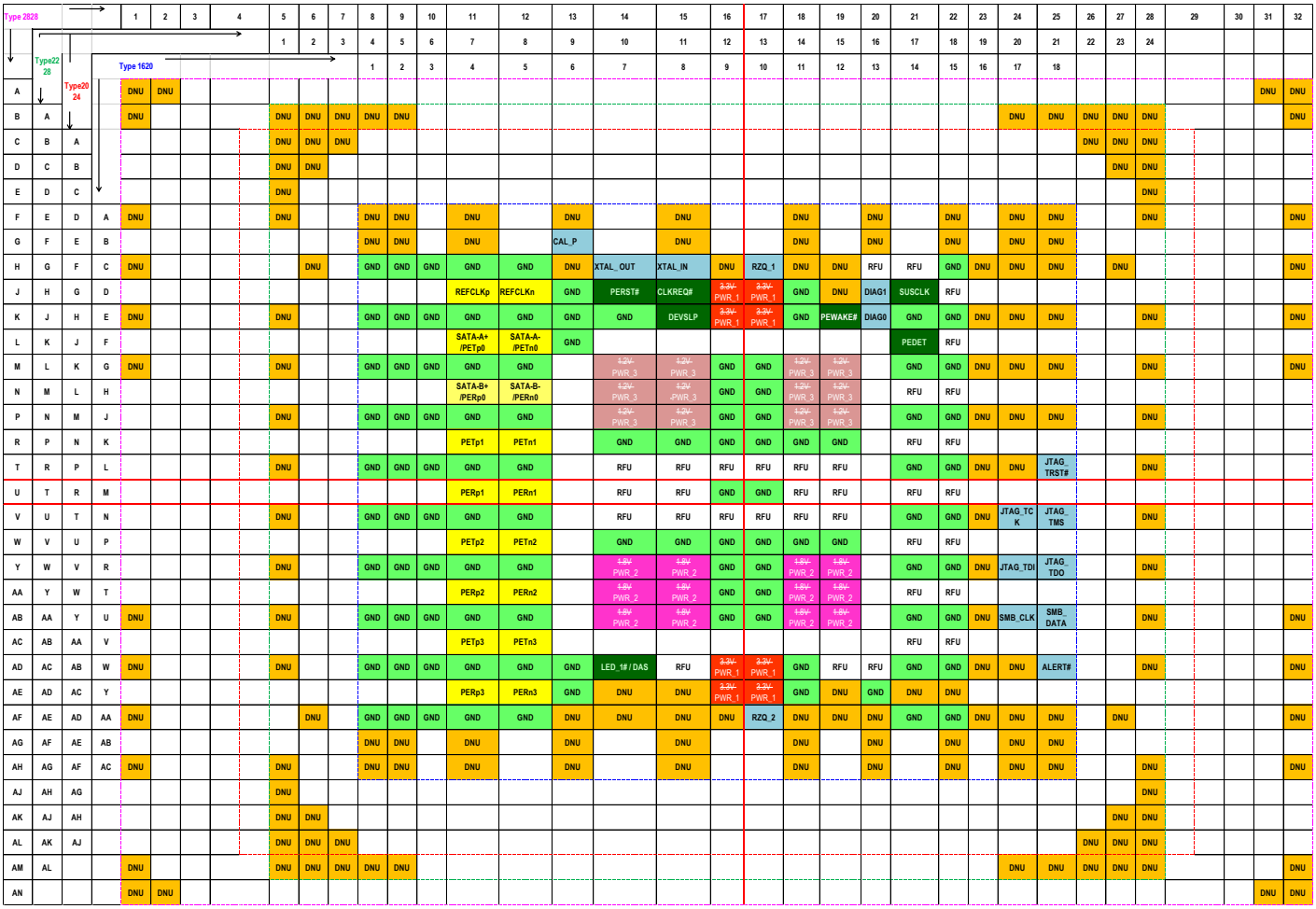


Figure 112. Type 1620, Type 2024, Type 2228, Type 2828 BGA ~~Pinout On Platform~~ Socket Map On Platform (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND
B	GND	GND	GND	REG_01	REG_02	REG_03			GND			GND			GND	WP_L	SPI_CLK	SPI_CS_L	GND	GND
C	GND	GND	GND	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_DATA	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPI_MOSI	SPI_MISO	GND	GND	GND
D		PWR_2	PWR_2	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPI_18	PWR_2	PWR_2	
E	GND	PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	GND
F		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	
H	GND	PWR_1	PWR_1	HSB	HSB	HSB	HSB								HSB	HSB	GND	PWR_1	PWR_1	GND
J		PWR_1	PWR_1	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	PWR_1	PWR_1	
K		GND	PWR_1	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_1	GND	
L	GND	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	GND
M	GND	GND	PWR_3	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	GND	GND
N		PWR_3	PWR_3	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	PWR_3	PWR_3	
P		PWR_3	PWR_3	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	PWR_3	PWR_3	
R	GND	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	GND
T		PWR_2	PWR_2	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
V	GND	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	GND
W		SUSCLK	CLKREQ#	PERST#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	CAL_P	XTAL_OUT	XTAL_IN	
Y	GND	LED_1#	GND	GND	GND	GND	PETp0	PETn0	GND	PERp0	PERn0	GND	PETp1	PETn1	GND	GND	GND	GND	PEWAKE#	GND
AA	GND	GND	GND	REFCLKp	REFCLKn	GND			GND			GND			GND	PERp1	PERn1	GND	GND	GND
AB	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND

Figure 1. Type 1113 BGA Socket Map On Platform (Top View)

6. Annex

6.1. Glossary

A	Amperage or Amp	**NIC**	Network Interface Card
BGA	Ball Grid Array	**N/C**	Not Connected
BIOS	Basic Input Output System	**OD**	Open Drain
BTO	Build-to-Order	**OEM**	Original Equipment Manufacturer
CEM	Card Electromechanical	**OS**	Operating System
CTO	Configure To Order	**PCIe**	Peripheral Component Interconnect Express
DC	Direct Current	**SATA**	Serial Advanced Technology Attachment or Serial ATA
DNU	Do Not Use	**PCM**	Pulse Code Modulation
DPR	Dynamic Power Reduction	**RF**	Radio Frequency
GND	Ground	**RFU**	Reserved for Future Use
GNSS	Global Navigation Satellite System (GPS+GLONASS)	**RMS**	Root Mean Square
HDR	Hybrid Digital Radio	**RoHS**	Restriction of Hazardous Substances Directive
HSIC	High Speed Inter-Chip	**RSS**	Root Sum Square
I/F	Interface	**RTC**	Real Time Clock
I/O (O/I)	Input/Output (Output/Input)	**SDIO**	Secure Digital Input Output
IR	Current x Resistance = Voltage	**SIM**	Subscriber Identity Module
I^2C	Inter-Integrated Circuit	**SSD**	Sold-State Drive
I2S	Integrated Interchip Sound	**SSIC**	Super Speed USB Inter-Chip
LED	Light Emitting Diode	**RF**	Radio Frequency
LGA	Land Grid Array	**USB**	Universal Serial Bus
M-PCIe	Mobile PCIe	**UART**	Universal Asynchronous Receive Transmit
mΩ	milli Ohm	**V**	Voltage
mA	milli Amp	**W**	Wattage or Watts
mm	milli meter	**WiGig**	60 GHz multi-gigabit speed wireless communication
mV	milli Volt	**WLAN**	Wireless Local Area Network
NFC	Near Field Communications	**WPAN**	Wireless Personal Area Network
M.2	Formerally called Next Generation Form Factor (NGFF)	**WWAN**	Wireless Wide Area Network
NB	Notebook		