PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	OCuLink Skew
DATE:	December 20, 2016
AFFECTED DOCUMENT:	OCuLink 1.0
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Part I

1.   Summary of the Functional Changes

A PCI Express Receiver is required to tolerate 6 ns of lane to lane skew when operating at 8.0 GT/s. The *PCI Express OCuLink Specification* allowed the cable assembly to consume the entire budget. The Transmitter and traces routing to the OCuLink connector need some of this budget. The *PCI Express Card Electromechanical Specification Revision 3.0* assigns 1.6 ns to the total interconnect lane to lane skew budget.

2.   Benefits as a Result of the Changes

Allowing the OCuLink cable ~~assemply~~assembly to have the full 6 ns of lane to lane skew requires additional buffers on all Receivers supporting this topology. This violates the general principal stated by the *PCI Express OCuLink Specification* that no changes are necessary for the PCI Express compliant component. By reducing the allowed lane to lane skew in the cable assembly, any compliant PCI Express Receiver is able to support OCuLink.

3.   Assessment of the Impact

The manufacturing tolerance of cable assemblies have a possibility of being more constrained based on the tighter lane to lane skew requirement. The propagation delay matching between optical modules within a cable assembly have a possibility of being more constrained.

4.   Analysis of the Hardware Implications

The total interconnect skew assigned to the interface in the *PCI Express Card Electromechanical Specification* is 1.6 ns. This consists of 0.35 ns for the add-in card 2-inch trace skew and 1.25 ns for the system board 7-inch trace skew.

For the OCuLink ~~invironment~~environment a 2-inch trace on each end between the Transceiver and connector is budgeted 2 × 0.35 ns = 0.7 ns for lane to lane skew. Since the total interconnect skew starts with 1.6 ns that leaves 1.6 ns – 0.7 ns = 0.9 ns for the cable assembly.

OCuLink cable assemblies need to be verified to be compliant to the tighter lane to lane skew requirement.

5.   Analysis of the Software Implications

No impact on software.

6.   Analysis of the C&I Test Implications

A different limit than initially released, but no new test.

Part II

Detailed Description of the change

Change Section 7.3 as follows:

7.3. Cable Electrical Specifications

The OCuLink cable assembly contains insulated conductors terminated in a connector at each end for use as a Link segment between host boards. This cable assembly is primarily intended as a point-to-point interface between host boards using controlled impedance cables. All cable assembly measurements are to be made between TP1 and TP4 with CCB test fixtures. These cable assembly Specifications are based upon twin axial cable characteristics. Table 7-1 provides a summary of the cable assembly characteristics and references addressing each parameter. Reported values are at 4 GHz. Note that plots show loss (positive values).

The total interconnect skew assigned to the interface in the *PCI Express Card Electromechanical Specification* is 1.6 ns. This consists of 0.35 ns for the add-in card 2-inch trace skew and 1.25 ns for the system board 7-inch trace skew. For the OCuLink environment, a 2-inch trace on each end between the Transceiver and connector is budgeted 2 X 0.35 ns = 0.7 ns for lane-to-lane skew. Starting with 1.6 ns, that leaves 1.6 ns – 0.7 ns = 0.9 ns for the cable assembly.

Table 7-1.   Cable Assembly Differential Characteristics Summary

Description	Reference	Value	Unit
Maximum insertion loss	7.3.2	15	dB
Minimum insertion loss	7.3.2	0	dB
Minimum return loss	7.3.3	Equation (7-5)	dB
Differential to common-mode return loss	7.3.4	Equation (7-6)	dB
Differential to common-mode conversion loss minus Insertion Loss	7.3.5	Equation (7-7)	dB
Common-mode to common-mode return loss	7.3.6	Equation (7-8)	dB
MDNEXT loss	7.3.7	Equation (7-9)	dB
MDFEXT loss	7.3.7	Equation (7-10)	dB
OCuLink Total Cable Assembly Skew (Sc)	7.3.8	~~6~~0.9 (max)	ns ~~MAX~~