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PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	OCuLink CPRSNT# Notice
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AFFECTED DOCUMENT:	OCuLink 1.0
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Part I:

1. Summary of the Functional Changes

The cable presence (CPRSNT#) signal was incompletely and inaccurately specified in the original OCuLink 1.0 specification. The definition for the logic levels of this signal contradicted the active low naming convention. The direction has multiple contradictions.

2. Benefits as a Result of the Changes

Specifying the proper functionality of the CPRSNT# signal allows designs to interoperate.

3. Assessment of the Impact

~~The CPRSNT# sideband is implementable.~~ Existing hardware designed to the previous specification may need to be modified to comply with these changes.

4. Analysis of the Hardware Implications

~~Specification provided that is necessary for hardware to be designed.~~The behavior of the CPRSNT# signal is changed from the previous specification.

5. Analysis of the Software Implications

No impact on software.

6. Analysis of the C&I Test Implications

No impact on testing.

NOTE: This ECR is to be submitted for review at the same time as the BP Type ECR. These documents complement each other and both are necessary to fully understand the proposed changes.

Part II:

Detailed description of the change

Change Sections 2.3 & 2.4 as follows (see next page)

2.3. Signal Description

Table 2-1. Signal Description

Signal	Description
PETp0, PETn0, PERp0, PERn0, PETp1, PETn1, PERp1, PERn1, PETp2, PETn2, PERp2, PERn2, PETp3, PETn3, PERp3, PERn3	Differential PCI Express Transmitter/Receiver Lanes (x4)
VSP	Vendor-Specific Position
CPRSNT#	Cable present signal
CWAKE#	Power management signal for Downstream device wakeup events.
PERST#	PCI Express Reset indicates when the applied main power is within the specified tolerance and is stable.
2-WIRE CLOCK	Management Bus Clock Internal applications must have 2-Wire Clock run down the cable end to end. External passive and active applications must have 2 Wire Clock terminated at the PCB and must not run down the cable end to end.
2-WIRE DATA	Management Bus Data Internal applications must have 2-Wire Data run down the cable end to end. External passive and active applications must have 2 Wire Data terminated at the PCB and must not run down the cable end to end.
3.3 V POWER	Power for the optional active cable circuitry (within the cable plug). External applications have optional implementations for +3.3 V. Internal applications have optional implementations for +3.3 V. (Vact = POWER 3.3 Vact TX, POWER 3.3 Vact RX). 3.3 V = Vman.
5 V POWER	External applications have optional end to end implementations for +5 V supplied by the root only.
All External OCuLink connectors require contacts for two power rails: +5 V and +3.3 V.	

See Appendix C and Appendix D for additional information for systems.

Auxiliary signals are provided on the connector to assist with system-level functionality or implementation. The PCI Express OCuLink cable connector and cabling support the following Auxiliary signals:

- CPRSNT# (required): Cable present detect, an active-low signal provided by an Endpoint ~~Downstream Subsystem~~ to indicate that it is both present and its power is within tolerance.
  - CPRSNT# = low level (Vman < 0.8 V) ==> ~~Low Level:~~ Cable ~~not~~ present and any power needed to operate the Endpoint is applied~~/or power not applied~~
  - ~~1.4 V < Vman < 1.8 V ==> Middle Level: Cable present, but power not applied~~
  - CPRSNT# = high level (Vman > 2.7 V) ==> ~~High Level:~~ Cable not present and/or power not applied

- CWAKE# (required): Cable Wake, an active-low signal that is driven by a Downstream Subsystem to re-activate a PCI Express hierarchy's main power rails. Although optional for Upstream and Downstream Subsystems, all cable assemblies must include CWAKE#.
- PERST# (Required): PCI Express Reset.
- VSP (optional) Vendor-specific Position, function and implementation specified by vendor.

2.4. Signal Compatibility Matrix

- All auxiliary signals are required from a cabling perspective.
- The signals listed in Table 2-2 are for an Upstream and/or Downstream Subsystem, with a brief description of features enabled by it.

Table 2-2. Signal Compatibility Matrix

Signal	Type	~~Root / Downstream Subsystem~~Downstream Port	Cable Assembly	~~End Point / Upstream Subsystem~~ Upstream Port	Comments
CPRSNT#	3.3 V Logic	Required ~~Output~~Input	Required	Required Output~~Input~~	Required on both sides of the cable. The driver is open-drain type and requires high impedance during power off states. Two ~~P~~possible states (see Section 2.3).~~:~~ The ROOT has a 4.7 kΩ resistor with a relative tolerance of 5% connected to VCC. The ENDPOINT has a 4.7 kΩ resistor with a relative tolerance of 5% connected to ground. ~~High (3.3 V) and (3.3 V)/2.~~
CWAKE#	3.3 V Logic	Optional Input	Required	Optional Output	Optional on both sides of the cable. The driver is open-drain type and requires high impedance during power off states. Signal becomes bidirectional if both ends support OBFF.
PERST#	3.3 V Logic	Required Output	Required	Required Input	When negated indicates when the applied main power is within the specified tolerance and is stable. (Cable installed and power not applied).
VSP		Optional I/O	Required (Note 1,2,3,4)	Optional I/O	Optional on both sides of the cable, function specified by vendor, is permitted to~~-~~ be used to support legacy functions or future functionality.
BP TYPE		Optional Input	Required	Optional Output	Input required to enable a full crossover internal cable solution.

Notes:

1. The use of SMBus across the cable is an optional feature. This allows the use of cables that adhere to SFF-8449 for a PCI Express interface with a reduced feature set. Active Optical Cable assemblies may not want to implement SMBus across the cable for cost or complexity reasons, and therefore is permitted to have a reduced feature set. The Upstream Subsystems should not be designed in such a way as to require the use of SMBus across the cable. However, the SMBus controller is still required by both Upstream and Downstream fixed ends to read the cable assembly information for configuration of the PCIe devices that are part of the cabled Link.
2. It is recommended that systems employing VSP for REFCLK functionality utilize pins A12+/A13- for the ROOT and pins B12+/B13- for the ENDPOINT.
3. SRIS architecture on Upstream and Downstream Subsystems is required if supporting no-wire VSP positions between Upstream and Downstream Subsystems.
4. Verify systems enabling unshielded wire at VSP positions meet EMI emission and EMI susceptibility limits, as required by target market regulatory bodies.