



PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Power-up requirements for PCIe side bands in a Vbat powered system
DATE:	October 20, 2014
AFFECTED DOCUMENT:	PCI Express M.2 Specification, Revision 1.0, as revised by "Power-up requirements for PCIe side bands (PERST#, etc.)" ECN.
SPONSOR:	Stefan Nilsson, Ericsson; Dave Landsman, SanDisk; Ramdas Kachare, LSI

Part I

1. Summary of the Functional Changes

In ECN "Power-up requirements for PCIe side bands (PERST#, etc.)" - submitted by Dave Landsman and Ramdas Kachare - section 3.1.3.2.1 is redefined to provide a more realistic timing model for reset.

This ECN is based on the mentioned ECN and adds timing information for PCIe start-up of a system that is powered from VBAT. In such a system a special signal is needed to switch on and off the card since battery voltage – VBAT - is permanently applied. There is a signal available – FULL_CARD_POWER_OFF# - that can be used for this purpose. The ECN covers the needed additions to support power-up in a VBAT powered system. Updates of section '3.2.10.1 FULL_CARD_POWER_OFF#' – to make the text clearer are also proposed.

2. Benefits as a Result of the Changes

This change provides the timing for power-up of a VBAT powered PCIe module where the 3.3 V supply ramp-up cannot be used to provide start timing for the power-up sequence of a module. All timing will be exactly the same as for a module powered by the 3.3 V power rail with the exception that start timing will be referenced from de-assertion of the FULL_CARD_POWER_OFF# signal.

3. Assessment of the Impact

There is no specification legacy with regard to using FULL_CARD_POWER_OFF# for this purpose.

4. Analysis of the Hardware Implications

FULL_CARD_POWER_OFF# is already defined for usage on VBAT powered modules. Thus there shall be no HW impact.

5. Analysis of the Software Implications

None

6. Analysis of the C&I Test Implications

None

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Part II

Detailed Description of the change

Black text is taken from the “Power-up requirements for PCIe side bands (PERST#, etc.)” ECN. Added text is red.

3.1.x Power-up Timing (after existing 3.1.3 and before existing 3.1.4)

Figure 79a provides an overview of the M.2 device power up sequence for a module powered from +3.3 V power rail, while Figure 79b provides an overview of the M.2 power up sequence for a module powered by a direct VBAT connection. In the case of a direct VBAT connection, the de-assertion of FULL_CARD_POWER_OFF# triggers start of the module power-up sequence. It is assumed that VBAT will be within its specified voltage range (see section 4.3) well before FULL_CARD_POWER_OFF# becomes de-asserted. See section 3.2.10.1 for details about the FULL_CARD_POWER_OFF# signal. Table 16 lists the power-up timing variable values.

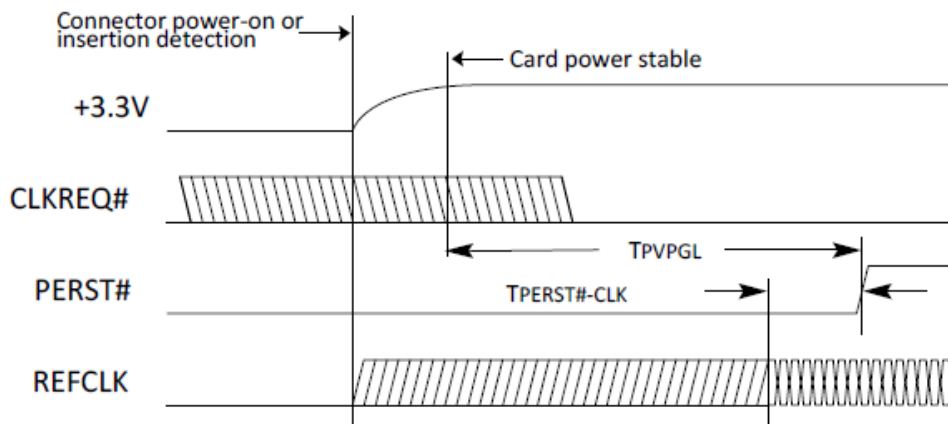


Figure 79a. Power-Up Timing Sequence for a module powered from a 3.3V power rail

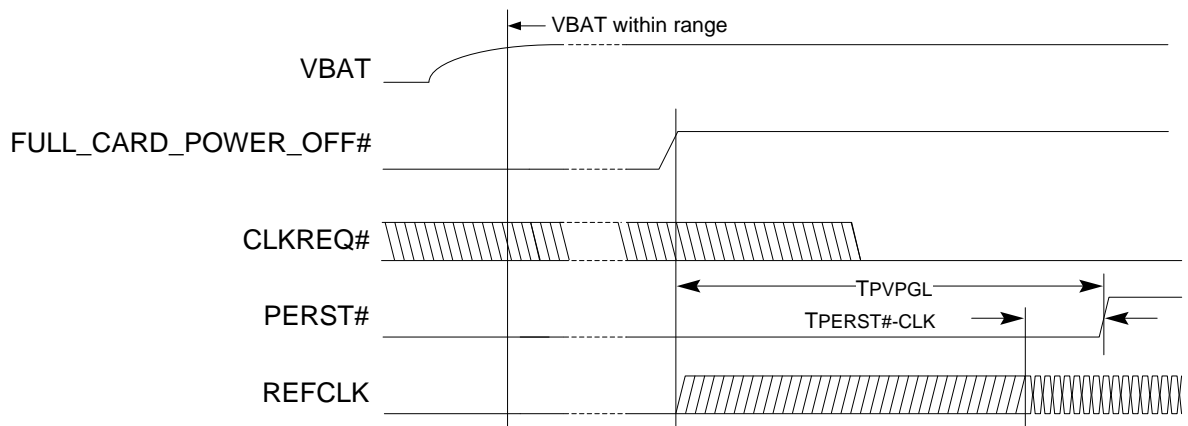


Figure 79b. Power-Up Timing Sequence for a module powered by a direct VBAT connection

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Symbol	Parameter	Min	Max	Units
T _{PVPG} L	Power Valid to PERST# Input inactive	Implementation specific; recommended 50 ms		ms
T _{PERST#-CLK}	REFCLK stable before PERST# inactive	100		μs

Table 16. Power-Up Timing Variables

3.1.x.1 PERST# Power-up Timing

The host shall delay de-assertion of PERST# for a period of time (T_{PVPG}L) after power is stable on the card (see Figure 79a or Figure 79b). See section 3.1.3.4 for further details on PERST#.

The PCI Express Specification (see Revision 3.0 or later, Conventional Reset) requires that a card must be in the LTSSM Detect state within 20 ms of PERST# being de-asserted and ready for Configuration Requests within 120 ms of PERST# being de-asserted.

The value of T_{PVPG}L is left as implementation specific, with a recommended value as a guideline. In considering the value of T_{PVPG}L:

- Card and host implementers should consult PCIe Express Reset Rules and platform BIOS and OS requirements governing card readiness timing requirements following the de-assertion of PERST#.
- Host implementers should consult card vendors for their T_{PVPG}L values, based on vendor specific card startup requirements.

3.1.x.2 REFCLK Power-up Timing

The host shall ensure that the reference clock is in the active clock state for at least a period of time specified by T_{PERST#-CLK}, prior to PERST# de-assertion. See section 3.1.3.1 for further details on REFCLK.

3.1.x.2 CLKREQ# Power-up Timing

See section 3.1.3.2 for details on CLKREQ#.

3.2.10.1. FULL_CARD_POWER_OFF#

FULL_CARD_POWER_OFF# signal is an Active Low input signal that is used to turn off the entire module. If When FULL_CARD_POWER_OFF# the input signal is de-asserted (i.e., driven high (≥1.19 V)), the Module shall will be enabled. If When FULL_CARD_POWER_OFF# the input signal is asserted (i.e., driven low signal (≤0.2 V) or Tri-stated), it will force the module shall be to shut down.

The FULL_CARD_POWER_OFF# pin shall needs to be internally pulled low on the module with a weak pull-down resistor of >20 kΩ. The module design shall must ensure that the operation of this pin is asynchronous to any other interface operation.

FULL_CARD_POWER_OFF# The input must be 3.3 V tolerant but may can be driven by either 1.8 V or 3.3 V GPIO. Host-side implementation for this signal to be defined by Module vendor including timing diagrams, operation sequencing etc. that are implementation specific.