PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Tighten Mini Card Power Rail Voltage Tolerance
DATE:	March 3, 2014
AFFECTED DOCUMENT:	PCI Express Mini-CEM 2.0
SPONSOR:	Jim Panian, Qualcomm

Part I

1. Summary of the Functional Changes

Modify the Mini Card specification to tighten the power rail voltage tolerance.

2. Benefits as a Result of the Changes

A power rail voltage tolerance change would provide the necessary voltage headroom needed for proper operation of the USB PHY circuitry under corner case supply voltages from the platform.

3. Assessment of the Impact

The host system power rail must be tuned to meet the new voltage tolerance requirements. Mini Card implementations must be compatible with the change. Aligns with the M.2 card power rail voltage tolerance specification on the low end.

4. Analysis of the Hardware Implications

None

5. Analysis of the Software Implications

None.

6. Analysis of the C&I Test Implications

None.

Part II

Detailed Description of the change

Change Section 3.4.3, Power, page 61 as follows:

3.4.3. Power

PCI Express Mini Card has two defined power rails: +3.3Vaux and +1.5V. Table 3-12 lists the voltage tolerances and power ratings for each PCI Express Mini Card slot implemented in a system.

Table 3-12: Power Ratings

	Voltage Tolerance	D0-D2, $D3_{hot}$ Power[1]		$D3_{cold}$ Power[2, 3]	
		Peak (max) mA	Normal (max) mA	Peak (max) mA	Normal (max) mA
3.3Vaux	~~±9%~~ +9% -5%	2,750	1,100	2,750 (wake enabled)	250 (wake enabled) 5 (no wake enabled)
+1.5V	±5%	500	375	N/A	N/A

1. For USB: Power states greater than Bus Suspend.
2. For USB: Wake enabled is USB Remote wakeup-Enabled and No Wake enabled is USB Remote wakeup- Disabled.
3. This D3 current limit only applies when the +1.5V voltage source is not available; i.e., the card is in $D3_{cold}$.

Definitions:
Peak – The highest averaged current value over any 100-microsecond period
Normal – The highest averaged current value over any 1-second period

Note: For Peak, the value of "100-microsecond period" was derived as follows: The period of time that the current is to be measured and averaged over must be less than a single GPRS slot time. This enables measurement of the average peak current within a single GPRS slot. There are 4.6 milliseconds/GPRS frame and eight slots per GPRS frame = 575 microseconds/slot. The 100-microsecond period < 575-microsecond period.

The operation of the +3.3Vaux power source shall conform to the *PCI Bus Power Management Interface Specification* and the *Advanced Configuration and Power Interface (ACPI) Specification*, except as otherwise specified by this document. If the host does not support wake from D3, +3.3Vaux may be removed by the host when +1.5V is removed.