PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Add USB 3.0 to the Mini Card
DATE:	August ~~8~~6, 2014
AFFECTED DOCUMENT:	PCI Express Mini-CEM 2.0
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Part I

1. Summary of the Functional Changes

Modify the Mini Card specification to enable USB 3.0.

2. Benefits as a Result of the Changes

Mobile broadband peak data rates continue to increase. With LTE category 5, USB 2.0 will not meet the performance requirements. LTE category 5 peak data rates are 320 Mbps downlink; 75 Mbps uplink. Most USB 2.0 implementations achieve a maximum of about 240 Mbps throughput. Looking longer term, the ITU has set a target of 1 Gbits/s for low mobility applications for IMT Advanced.

Mobile broadband devices will be deployed in other form factors which will utilize USB 3.0 such as USB 3.0 dongles. It is sensible to also extend USB 3.0 support to the Mini Card.

3. Assessment of the Impact

USB 3.0 will use the same differential transmit/receive pins as are currently used by PCI Express:

Pin 33 – PETp0; Pin 31 – PETn0; Pin 25 – PERp0; Pin 23 – PERn0

4. Analysis of the Hardware Implications

1. USB 3.0 shares the differential transmit/receive pins with PCIe.
2. How the platform selects which of the two interfaces to activate is platform-specific.

5. Analysis of the Software Implications

None.

6. Analysis of the C&I Test Implications

None.

Part II

Detailed Description of the change

Change Section 1.2, Specification References, page 9 as follows:

- *Universal Serial Bus Specification, Revision 2.0*
- *Universal Serial Bus Specification, Revision 3.0*

Change Section 2.1, Overview, Figure 1-2 on page 8 as follows:

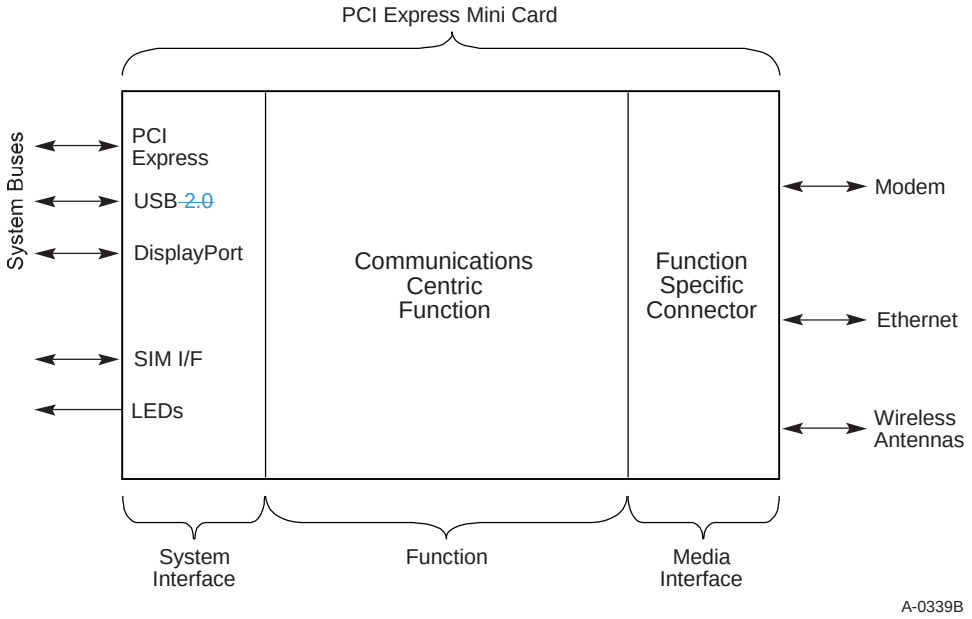

Figure 0-12: Logical Representation of the PCI Express Mini Card Specification

Change Section 2.1, Overview, Table 2-1 on page 11 as follows:

Table 0-1: Mini Card Form Factors

Card Type	Pin Count	PCI Express	USB ~~2.0~~	DisplayPort
Full-Mini Card	52	✓	✓	
Half-Mini Card	52	✓	✓	
Display-Mini Card	76	✓	✓	✓

Change Section 3.2.2, PCI Express Interface, on page 43 as follows:

3.2.2 PCI Express Interface

The PCI Express interface supports a x1 PCI Express interface (one Lane). A Lane consists of an input and an output high-speed differential pair. Also supported is a PCI Express reference clock. Refer to the *PCI Express Base Specification* for more details on the functional requirements for the PCI Express interface signals.

The PCI Express interface and the USB 3.0 interface cannot operate simultaneously, as they share the same pins. How the platform selects which of the two interfaces to activate is platform-specific

Change Table 3.1, page 41 as follows:

Table 3-~~2~~1: PCI Express Mini Card System Interface Signals

Signal Group	Signal	Direction	Description
Power	+3.3Vaux (5 pins)		3.3 V source
	+1.5V (3 pins)		1.5V source
	GND (14 pins)		Return current path
PCI Express	PETp0, PETn0 PERp0, PERn0	Input/Output	PCI Express x1 data interface: one differential transmit pair and one differential receive pair. (Note: these signals overlay the USB 3.0 data interface at the socket.)
	REFCLK+, REFCLK–	Input	PCI Express differential reference clock (100 MHz)
Universal Serial Bus (USB)	SSTX+ SSTX- SSRX+ SSRX-	Input/Output	USB 3.0 SuperSpeed serial data interface. One differential transmit pair and one differential receive pair (Note: these signals overlay the PCI Express x1 data interface at the socket)
	USB_D+, USB_D–	Input/Output	USB serial data interface compliant to the USB 2.0 specification

Change Section 3.2.3, page 44 as follows:

3.2.3 USB Interface

The USB 2.0 interface supports USB 2.0 in all three modes (Low Speed, Full Speed, and High Speed). ~~Because~~ Since there is not a separate USB-controlled voltage bus, USB functions implemented on a PCI Express Mini Card add-in card are expected to report as self-powered devices. All electrical characteristics, enumeration, bus protocol, and bus management features for this interface are defined by *Universal Serial Bus Specification, Revision 2.0*

USB-based Mini Cards that implement a wakeup process are required to use the in-band wakeup protocol ~~(across the USB_D+/USB_D- pins~~) as defined in the *Universal Serial Bus Specification* and shall not use the WAKE# signal to enable the in-band wakeup process.

The USB 3.0 interface supports USB 3.0 (Superspeed) at Gen 1. The SuperSpeed differential transmit lines (SSTX+, SSTX-) are required to implement the transmit path of a USB 3.0 SuperSpeed interface. These pins shall be connected to the transmitter differential pair in the system and to the receiver differential pair on the module.

Likewise, SuperSpeed differential receive lines (SSRX+, SSRX-) are required to implement the receive path of a USB 3.0 SuperSpeed interface. These pins shall be connected to the receiver differential pair in the system and to the transmitter differential pair on the module.

Note: for host systems that implement USB 3.0 support, the SuperSpeed differential transmit/receive pins are shared with the PCI Express interface.

The *Universal Serial Bus Specification, Revision 3.0* defines all electrical characteristics, enumeration, bus protocol and bus management features for this interface.

If the USB 3.0 interface is not supported then~~,~~ ~~all USB pins must be left unconnected.~~ ~~The~~the four SuperSpeed differential pins may ~~then~~ be used as PCI Express differential pins.

Change Table 3-8, page 54 as follows:

3.3 Connector Pin-out Definitions

The following sections illustrate signal pin-outs for the system connector. Table 3-8 lists the pin-out for both the 52-pin and 76-pin system connectors. For the 52-pin version of the connector, pins 53-76 are not present.

Table 3-8: System Connector Pin-out

Pin #	Name	Pin #	Name
75	GND	76	MLDIR
73	ML0p	74	GND
71	ML0n	72	GND
69	GND	70	ML1p
67	GND	68	ML1n
65	ML2p	66	GND
63	ML2n	64	GND
61	GND	62	ML3p
59	GND	60	ML3n
57	AUXp	58	GND
55	AUXn	56	GND
53	DMC#	54	HPD
Mechanical Key			
51	W_DISABLE2#	52	+3.3Vaux
49	Reserved	50	GND
47	Reserved	48	+1.5V
45	Reserved	46	LED_WPAN#
43	GND	44	LED_WLAN#
41	+3.3Vaux	42	LED_WWAN#
39	+3.3Vaux	40	GND
37	GND	38	USB_D+
35	GND	36	USB_D-
33	PETp0 or SSTX+	34	GND

Pin #	Name	Pin #	Name
31	PETn0 or SSTX-	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0 or SSRX+	26	GND
23	PERn0 or SSRX-	24	+3.3Vaux
21	GND	22	PERST#
19	UIM_IC_DP	20	W_DISABLE1#
17	UIM_IC_DM	18	GND
Mechanical Key			
15	GND	16	UIM_SPU

13	REFCLK+	14	UIM_RESET
11	REFCLK-	12	UIM_CLK
9	GND	10	UIM_DATA
7	CLKREQ#	8	UIM_PWR
5	COEX2	6	1.5V
3	COEX1	4	GND
1	WAKE#	2	3.3Vaux