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PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Transition of NFC Signals from 3.3V to 1.8V
DATE:	October 19, 2014
AFFECTED DOCUMENT:	M.2 Spec Rev 1.0
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Part I

1. Summary of the Functional Changes

The proposed change is to change the current voltage level of the NFC related signals (I2C DATA, I2C CLK and ALERT#) on the Connectivity pinouts and definitions from 3.3V to 1.8V signal level to better align with future platforms operating signal levels typical in the industry.

The change is being proposed to simply change the definition in the spec because no one in the WG has given any indication that the NFC signals are being used at their current 3.3V definition nor are they planning to use them at 3.3V in the near future.

2. Benefits as a Result of the Changes

To better align with theindustry transition to 1.8V IO signal levels both on platform

3. Assessment of the Impact

No known impact

4. Analysis of the Hardware Implications

No expected contention because no one seems to have ever used or wired up these signals.

5. Analysis of the Software Implications

N/A.

6. Analysis of the C&I Test Implications

N/A.

Part II

Detailed Description of the change

Change Table 15 as follows:

			compliant to the *USB 2.0 Specification*	
I2C	ALERT#	O	IRQ line to host processor; Open Drain with pull up on platform; Active Low	~~3.3~~1.8 V
	I2C_CLK	I	I2C clock input from host. Open Drain with pull up on platform	~~3.3~~1.8 V

Signal Group	Signal	I/O	Description	Voltage
	I2C_DATA	I/O	I2C data. Open Drain with pull up on platform	~~3.3~~1.8 V
Display Port	DP_HPD	I or O	Hot Plug Detect. Direction is determined by DP_MLDIR	3.3 V
	DP_MLDIR	I/O	Display Port data interface direction	0 V/ 3.3 V/

Change Table 22 as follows:

Table 22. SDIO Based Module Solution Pinout (Module Key E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PETn1	67
64	RESERVED	RESERVED/PETp1	65
62	ALERT# (O)(0/1.8V)	GND	63
60	I2C_CLK (I)(0/1.8V)	RESERVED/PERn1	61
58	I2C_DATA (I/O)(0/1.8V)	RESERVED/PERp1	59
56	W_DISABLE1# (I)(0/3.3V)	GND	57
54	W_DISABLE2# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (I)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKn0	49
46	COEX2(I/O)(0/1.8V)	REFCLKp0	47

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Change Table 23 as follows:

Table 23. Display Port Based Module Solution Pinout (Module Key A)

74	3.3V	GND	75
72	3.3V	REFCLKn1	73
70	PEWAKE1# (I/O)(0/3.3V)	REFCLKp1	71
68	CLKREQ1# (I/O)(0/3.3V)	GND	69
66	PERST1# (I)(0/3.3V)	PETn1	67
64	RESERVED	PETp1	65
62	ALERT# (O)(0/1.8V)	GND	63
60	I2C_CLK (I)(0/1.8V)	PERn1	61
58	I2C_DATA (I/O)(0/1.8V)	PERp1	59
56	W_DISABLE1# (I)(0/3.3V)	GND	57
54	W_DISABLE2# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (I)(0/3.3V)	GND	51
		REFCLKn0	49

Change Table 24 as follows:

Table 24. Socket 1 Module Pinout with Dual Module Key (A-E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PETn1	67
64	RESERVED	RESERVED/PETp1	65
62	ALERT# (O)(0/1.8V)	GND	63
60	I2C_CLK (I)(0/1.8V)	RESERVED/PERn1	61
58	I2C_DATA (I/O)(0/1.8V)	RESERVED/PERp1	59
56	W_DISABLE1# (I)(0/3.3V)	GND	57
54	W_DISABLE2# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (I)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKn0	49

Update text in Chapter 4.1 as follows:

4.1. 3.3 V Logic Signal Requirements

The 3.3 V card logic levels for single-ended digital signals (WAKE#, CLKREQ#, PERST#, SUSCLK, W_DISABLE#, UART_WAKE, ~~I2C,~~ DP_MLDIR, LED#) are given in Table 36.

Table 36. DC Specification for 3.3 V Logic Signaling

Symbol	Parameter	Condition	Min	Max	Unit	Notes
+3.3 V	Supply Voltage		3.135	3.465	V	
V_{IH}	Input High Voltage		2.0	3.6	V	
V_{IL}	Input Low Voltage		0.5	0.8	V	

Update text in Chapter 4.2 as follows:

4.2. 1.8 V Logic Signal Requirements

The 1.8 V card logic levels for single-ended digital signals (SDIO, UART, I2C, PCM/I2S, etc.) are given in Table 37.

Table 37. DC Specification for 1.8 V Logic Signaling

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{DD18}	Supply Voltage		1.7	1.9	V	
V_{IH}	Input High Voltage		0.7*V_{DD18}	V_{DD18}+0.3	V	
V_{IL}	Input Low Voltage		-0.3	0.3*V_{DD18}	V	
V_{OH}	Output High Voltage	I_{OH} = -1mA V_{DD18} Min	V_{DD18}-0.45		V	
V_{OL}	Output Low Voltage	I_{OL} = 1mA		0.45	V	

Change Table 44 as follows:

Table 44. Socket 1-DP Pin-Out Diagram (Mechanical Key A) On Platform

74	3.3V	GND	75
72	3.3V	REFCLKn1	73
70	PEWAKE1# (I/O)(0/3.3V)	REFCLKp1	71
68	CLKREQ1# (I/O)(0/3.3V)	GND	69
66	PERST1# (O)(0/3.3V)	PERn1	67
64	RESERVED	PERp1	65
62	ALERT# (I)(0/1.8V)	GND	63
60	I2C_CLK (O)(0/1.8V)	PETn1	61
58	I2C_DATA (IO)(0/1.8V)	PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKn0	49
		REFCLKp0	47

Change Table 45 as follows:

Table 45. Socket 1-SD Pin-Out Diagram (Mechanical Key E) On Platform

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PERn1	67
64	RESERVED	RESERVED/PERp1	65
62	ALERT# (I)(0/1.8V)	GND	63
60	I2C_CLK (O)(0/1.8V)	RESERVED/PETn1	61
58	I2C_DATA (I/O)(0/1.8V)	RESERVED/PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
		REFCLKn0	49