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PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	M.2 COEX Signal Definition - UART
DATE:	October 19, 2014
AFFECTED DOCUMENT:	M.2 Spec Revision 1.0
SPONSOR:	Ra'anan Sover; Intel Corp

Part I

1. Summary of the Functional Changes

Definition of two of the three COEX pins as a UART Tx/Rx communication path between Socket 1 and Socket 2 in favor of WWAN ←→ Connectivity coexistence. The intent is to definitively define the location of the source and sink sides of the signal path.

2. Benefits as a Result of the Changes

Improved Coexistance alignement across the industry. Potential interoperability (Mix-n-Match) through the adoption of already existing standard coexistence protocol defined in the BT-SIG. Prevent potential damage/contention due to lack of alignement when mixed and matched.

3. Assessment of the Impact

Should not affect current situation or current use of these signals.

4. Analysis of the Hardware Implications

Same platform COEXx ←→ COEXx connections

5. Analysis of the Software Implications

N/A

6. Analysis of the C&I Test Implications

N/A

Part II

Detailed Description of the change

Change Capter 1.3 to include reference to the BT SIG document as follows:

- EIA-364 Electrical Connector/Socket Test Procedures including Environmental Classifications
- EIA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications
- BT-SIG - Draft Improvement Proposal Document For Coexistence, V10r00, January 19 2010

Change Table 15 as follows:

	~~LED_2#~~		status indicators via LED devices that will be provided by the system.	
	~~COEX[1..3]~~ COEX_RXD COEX_TXD COEX3	I O I/O	Coexistence between WiFi+BT and WWAN on Socket 2. UART TxD and RxD signals per BT-SIG coexistence protocol + an undefined signal	1.8 V
NFC-UIM Signals	UIM_POWER_SRC/GPIO1	I	UICC power out from BB PMU	Per ISO 7816 Specification
	UIM_POWER_SNK	O	NFC PMU power to the UICC	
	SWP	I/O	UICC Secure element	

PCI Express M.2 Specification
Revision 1.0, November 1, 2013 94

Change Chapter 3.1.11.4 as follows:

3.1.11.4. Coexistence Signals

~~COEX1~~COEX_RXD, ~~COEX2~~ COEX_TXD and COEX3 are provided to allow for the implementation of wireless coexistence solutions between the radio(s) on the M.2 Card and other off-card radio(s). These other radios can be located on another M.2 Card located in the same host platform or as alternate radio implementations (for example, using a PCI Express M.2 CEM or a proprietary form-factor add-in solution).

The COEX_RXD and COEX_TXD signals are for a UART communication path between the WWAN radio solution and the wireless solutions on the Connectivity module. The coexistence protocol of these signals is based on the BT-SIG coexistence protocol.

- The COEX_TXD is the UART Transmit signal from the Connectivity module to the WWAN solution
- The COEX_RXD is the UART Receive signal from the WWAN solution to the Connectivity module.

The pin assignment can be seen in the pinout diagrams and coincides with the signals in the Socket 2 pinouts.

The functional definition of ~~these pins~~the COEX3 pin is OEM-specific and should be coordinated between the host platform OEM and card vendors. The ordered labeling of these signals in this specification is intended to help establish consistent implementations, where practical, across multiple instances of cards in the host platform.

Change Table 22 as follows:

Table 22. SDIO Based Module Solution Pinout (Module Key E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PETn1	67
64	RESERVED	RESERVED/PETp1	65
62	ALERT# (O)(0/3.3V)	GND	63
60	I2C_CLK (I)(0/3.3V)	RESERVED/PERn1	61
58	I2C_DATA (I/O)(0/3.3V)	RESERVED/PERp1	59
56	W_DISABLE1# (I)(0/3.3V)	GND	57
54	W_DISABLE2# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (I)(0/3.3V)	GND	51
48	COEX_RXD (I)(0/1.8V)	REFCLKn0	49
46	COEX_TXD (O)(0/1.8V)	REFCLKp0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PETn0	43
40	VENDOR DEFINED	PETp0	41
38	VENDOR DEFINED	GND	39
36	UART_CTS (I)(0/1.8V)	PERn0	37

Change Table 23 as follows:

Table 23. Display Port Based Module Solution Pinout (Module Key A)

74	3.3V	GND	75
72	3.3V	REFCLKn1	73
70	PEWAKE1# (I/O)(0/3.3V)	REFCLKp1	71
68	CLKREQ1# (I/O)(0/3.3V)	GND	69
66	PERST1# (I)(0/3.3V)	PETn1	67
64	RESERVED	PETp1	65
62	ALERT# (O)(0/3.3V)	GND	63
60	I2C_CLK (I)(0/3.3V)	PERn1	61
58	I2C_DATA (I/O)(0/3.3V)	PERp1	59
56	W_DISABLE1# (I)(0/3.3V)	GND	57
54	W_DISABLE2# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (I)(0/3.3V)	GND	51
48	COEX_RXD (I)(0/1.8V)	REFCLKn0	49
46	COEX_TXD (O)(0/1.8V)	REFCLKp0	47
44	COEX3 (I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PETn0	43
40	VENDOR DEFINED	PETp0	41
38	VENDOR DEFINED	GND	39
36	GND	PERn0	37
34	DP_ML0p	PERp0	35
32	DP_ML0n	GND	33
		DP_HPD (I/O)(0/3.3V)	31

Change Table 24 as follows:

Table 24. Socket 1 Module Pinout with Dual Module Key (A-E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PETn1	67
64	RESERVED	RESERVED/PETp1	65
62	ALERT# (O)(0/3.3V)	GND	63
60	I2C_CLK (I)(0/3.3V)	RESERVED/PERn1	61
58	I2C_DATA (I/O)(0/3.3V)	RESERVED/PERp1	59
56	W_DISABLE1# (I)(0/3.3V)	GND	57
54	W_DISABLE2# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (I)(0/3.3V)	GND	51
48	COEX_RXD (I)(0/1.8V)	REFCLKn0	49
46	COEX_TXD (O)(0/1.8V)	REFCLKp0	47
44	COEX3 (I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PETn0	43
40	VENDOR DEFINED	PETp0	41
38	VENDOR DEFINED	GND	39
36	N/C	PERn0	37
34	N/C	PERp0	35
32	N/C	GND	33

Change Diagram 87 as follows:

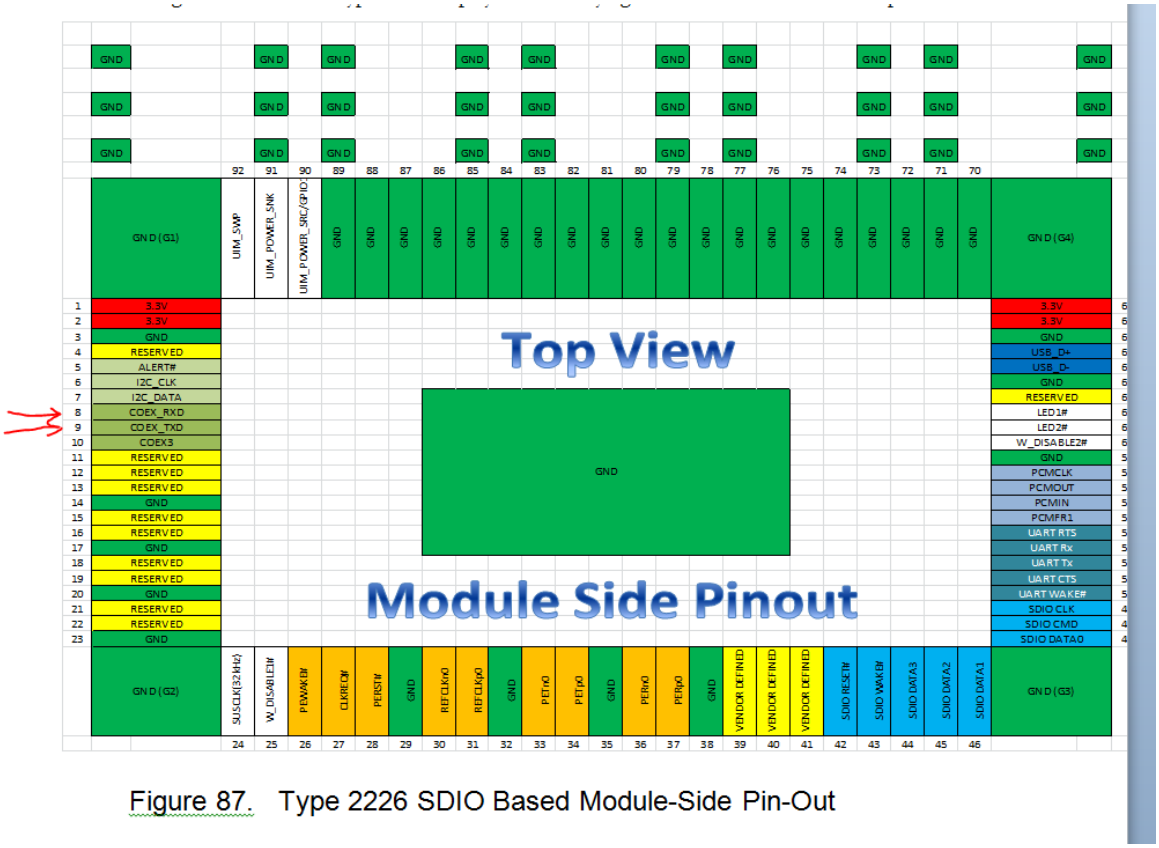


Figure 87. Type 2226 SDIO Based Module-Side Pin-Out

Change Diagram 88 as follows:

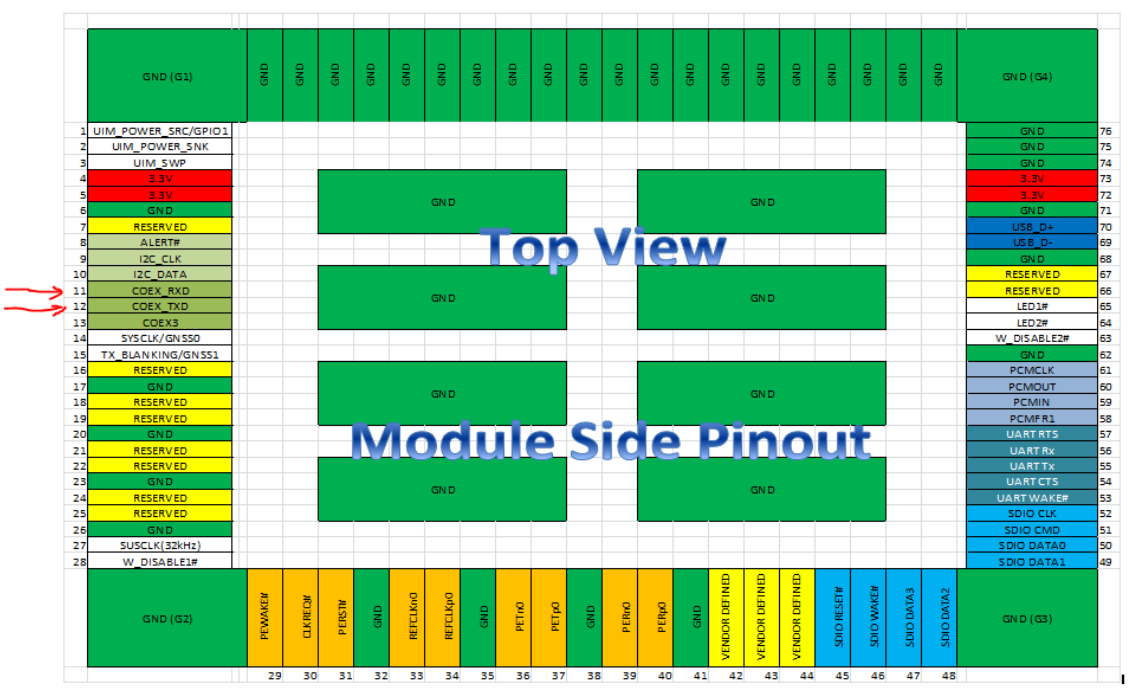


Figure 88. Type 1216 SDIO Based Module-Side Pin-Out

Change Diagram 89 as follows:

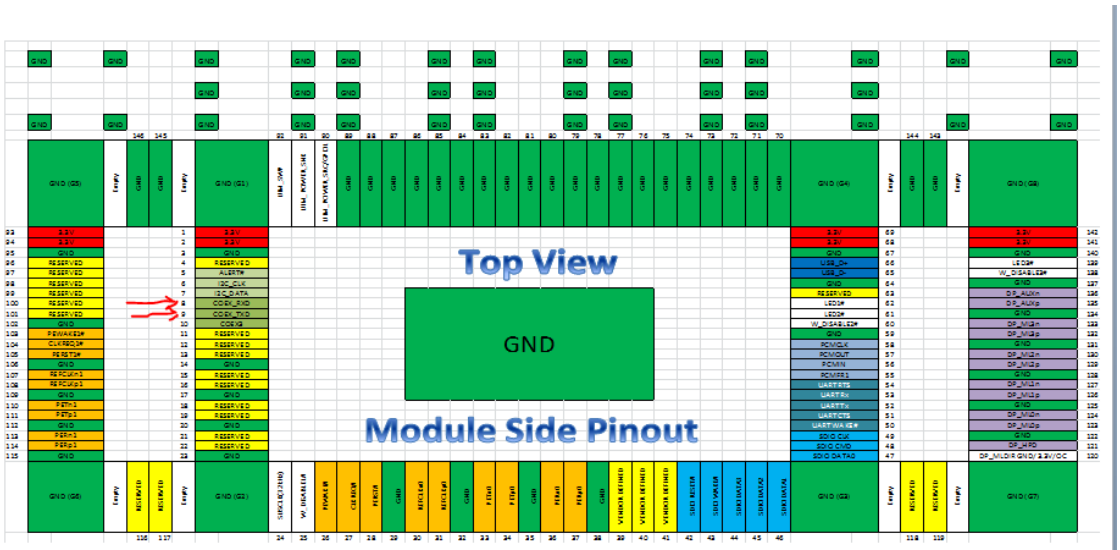


Figure 89. Type 3026 Display Port Pinout Extension Over an SDIO Based Module-Side Pin-Out

Change Table 25 as follows:

			pull-up resistor on the card.	
	LED_1#	O	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.	3.3 V
	~~COEX[1..3]~~COEX_TXD COEX_RXD COEX3	O I I/O	Coexistence between WWAN and WiFi+BT on Socket 1. UART TxD and RxD signals per BT-SIG coexistence protocol + an undefined signal	1.8 V
Supplemental Communication Specific Signals	FULL_CARD_POWER_OFF#	I	A single control to turn Off the WWAN solution. It is Active Low. This is only required on Tablet devices working directly off VBAT	1.8 V
	RESET#	I	A single control to Reset the WWAN solution. Active Low. This is needed when working in	1.8 V

Change Chapter 3.2.9.4 as follws:

3.2.9.4. Coexistence Signals

See section 3.1.11.4, *Coexistence Signals* for a more detailed description of the COEX_TXD, COEX_RXD and COEX3 signals.

Change Table 28 as follws:

Table 28. Socket 2 SSIC-based WWAN Module Pinout

74	3.3V	CONFIG_2 (States 8, 9, 10, 11)	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 (States 8, 9, 10, 11)	69
66	SIM_DETECT (I)	RESET# (I)(0/1.8V)	67
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
58	N/C	ANTCTL0 (O)(0/1.8V)	59
56	N/C	GND	57
54	N/C	N/C	55
52	N/C	N/C	53
50	N/C	GND	51

Change Table 29 as follows:

Table 29. Socket 2 USB3.0-based WWAN Module Pinout

74	3.3V	CONFIG_2 (States 4, 5, 6, 7)	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 (States 4, 5, 6, 7)	69
66	SIM_DETECT (I)	RESET# (I)(0/1.8V)	67
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
58	N/C	ANTCTL0 (O)(0/1.8V)	59
56	N/C	GND	57
54	N/C	N/C	55
52	N/C	N/C	53
50	N/C	GND	51
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O) (0/1.8V)	N/C	49

Change Table 30 as follows:

Table 30. Socket 2 PCIe-based WWAN Module Pinout

74	3.3V	CONFIG_2 (States 2, 3, 12, 13)	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 (States 2, 3, 12, 13)	69
66	SIM_DETECT (I)	RESET# (I)(0/1.8V)	67
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
58	N/C	ANTCTL0 (O)(0/1.8V)	59
56	N/C	GND	57
54	PEWAKE# (I/O)(0/3.3V)	REFCLKp	55
52	CLKREQ# (I/O)(0/3.3V)	REFCLKn	53
50	PERST# (I)(0/3.3V)	GND	51
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	PERp0	49

Change Chapter 5.1.1 as follows:

5.1.1. Socket 1-DP (Mechanical Key A) On Platform

- Socket 1-DP pinout Key A is intended to support Wireless Connectivity devices including combinations of WiFi, BT, NFC, and/or WiGig. Other Combos are possible provided they use the defined Host I/Fs in the pinout.
- PCIe Lane 0 is intended for use with the WiFi.
- PCIe Lane 1 is intended for use with the WiGig if the PCIe Lane 0 is not shared with the WiFi.
- Four Lane Display Port with assorted sideband signaling is also intended for use with the WiGig.
- LED1# and W_DISABLE1# are intended for use with the WiFi and WiGig.
- USB and LED2# are intended for use with the BT. There is only one W_DISABLE# supported by default. However, an adjacent Reserved pin (Pin 54) can be used alternatively as W_DISABLE2# for the BT.
- I2C and ALERT are intended for use with NFC.
- COEX ~~can be used as needed by~~signals are used for coexistence between the different Wireless Comms. Two signals have unique directionality associated with them. All ~~These~~ these COEX signals should be connected to the Socket 2 COEX signals for coexistence with the WWAN solution.

Change Table 44 as follows:

74	3.3V	GND	75
72	3.3V	REFCLKn1	73
70	PEWAKE1# (I/O)(0/3.3V)	REFCLKp1	71
68	CLKREQ1# (I/O)(0/3.3V)	GND	69
66	PERST1# (O)(0/3.3V)	PERn1	67
64	RESERVED	PERp1	65
62	ALERT# (I)(0/3.3V)	GND	63
60	I2C_CLK (O)(0/3.3V)	PETn1	61
58	I2C_DATA (IO)(0/3.3V)	PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX_TXD (O)(0/1.8V)	REFCLKn0	49
46	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
44	COEX3 (I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	GND	PETn0	37
34	DP_ML0p	PETp0	35
32	DP_ML0n	GND	33
		DP_HPD (I/O)(0/3.3V)	31

Change Chapter 5.1.2 as follows:

- PCIe Lane 1 PET and PER are intended for future expansion in case a two Lane PCIe is needed (for example, with WiGig Combo).
- I2C and ALERT# are intended for use with NFC.
- COEX ~~can be~~signals are used ~~as needed by~~for coexistence between the different Wireless Comms. Two signals have unique directionality associated with them. All ~~These~~ these COEX signals should be connected to Socket 2 COEX signals for coexistence with the WWAN solution.
- Other Comm/Host I/F combinations are possible. Actual implementation needs to be defined and agreed upon by Vendor←→Customer.

Change Table 45 as follows:

Table 45. Socket 1-SD Pin-Out Diagram (Mechanical Key E) Platform

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PERn1	67
64	RESERVED	RESERVED/PERp1	65
62	ALERT# (I)(0/3.3V)	GND	63
60	I2C_CLK (O)(0/3.3V)	RESERVED/PETn1	61
58	I2C_DATA (I/O)(0/3.3V)	RESERVED/PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX_TXD (O)(0/1.8V)	REFCLKn0	49
46	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
44	COEX3 (I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0/1.8V)	PETn0	37

Change Chapter 5.2.2 as follows:

5.2.2. Socket 2 Pin-Out (Mechanical Key B) On Platform

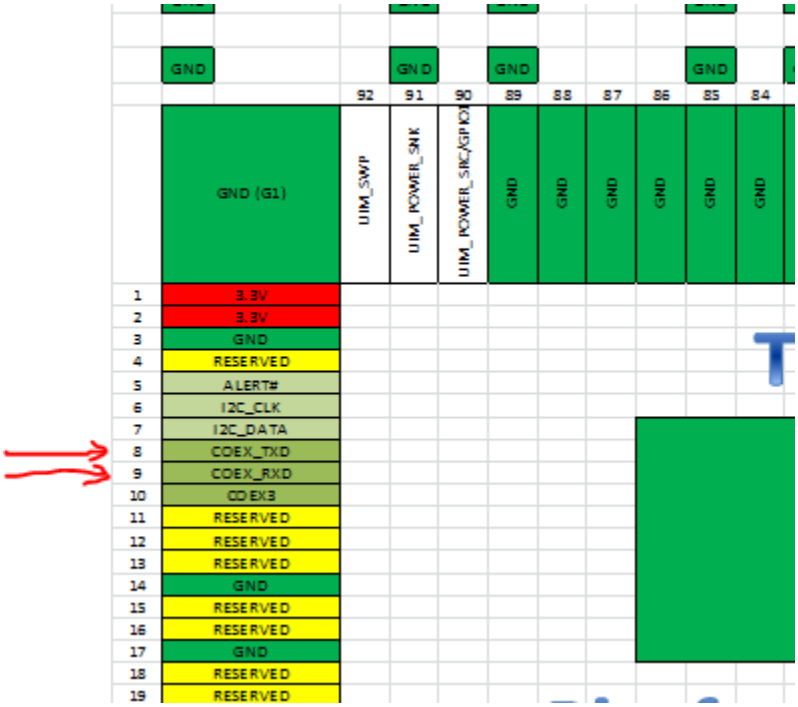
- Socket 2 pinout is intended to support WWAN+GNSS, SSD, and Other types of Add-In solutions with the defined and configurable Host I/Fs.
- WWAN can make use of USB2.0, USB3.0, PCIe (up to two Lanes), or SSIC host I/Fs. The actual implemented I/F is identified through the Configuration pins state (1 of 16 states) on the Module side. LED1# and W_DISABLE1# are intended for use with the WWAN solution. There are additional WWAN and GNSS related pins including W_DISABLE2#, DPR, and WAKE_ON_WWAN#
- The UIM and SIM Detect pin are used in conjunction with a SIM device in support of the WWAN solution.
- The COEX signals are used for coexistence between the different Wireless Comms. Two signals have unique directionality associated with them. All these COEX signals should be connected to Socket 1 COEX signals for coexistence with the Connectivity solution~~and~~
- The ANTCTL pins are placeholders for future expansion and definition of these functions.
- The GPIO0..11 pins are configurable with four different variants. These variants can be in support of the GNSS interface, second UIM/SIM, Audio interfaces, HSIC and IPC sidebands.

Change Table 47 as follows:

Table 47. Socket 2 Pinout Diagram (Mechanical Key B)

74	3.3V	CONFIG_2	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	CONFIG_1	69
66	SIMDETECT(O)	RESET#(O)(0/1.8V)	67
64	COEX_RXD(I)(0/1.8V)	ANTCTL3(I)(0/1.8V)	65
62	COEX_TXD(O)(0/1.8V)	ANTCTL2(I)(0/1.8V)	63
60	COEX3(I/O)(0/1.8V)	ANTCTL1(I)(0/1.8V)	61
58	N/C	ANTCTL0(I)(0/1.8V)	59
56	N/C	GND	57
54	PEWAKE#(I/O)(0/3.3V)	REFCLKp	55
52	CLKREQ#(I/O)(0/3.3V)	REFCLKn	53
50	PERST#(O)(0/3.3V)	GND	51
48	GPIO_4(I/O)(0/1.8V*)	PETp0/SATA-A+	49

Chage Figure 92 as follows:



Change Figure 93 as follows:

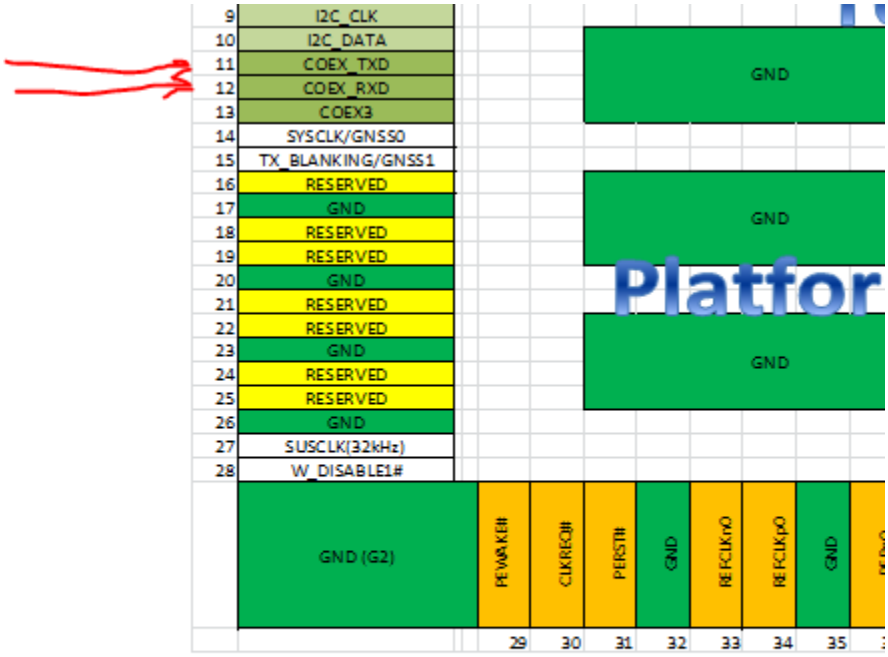


Figure 93. Type 1216 LGA P
Out on Platform

Change Figure 94 as follows:

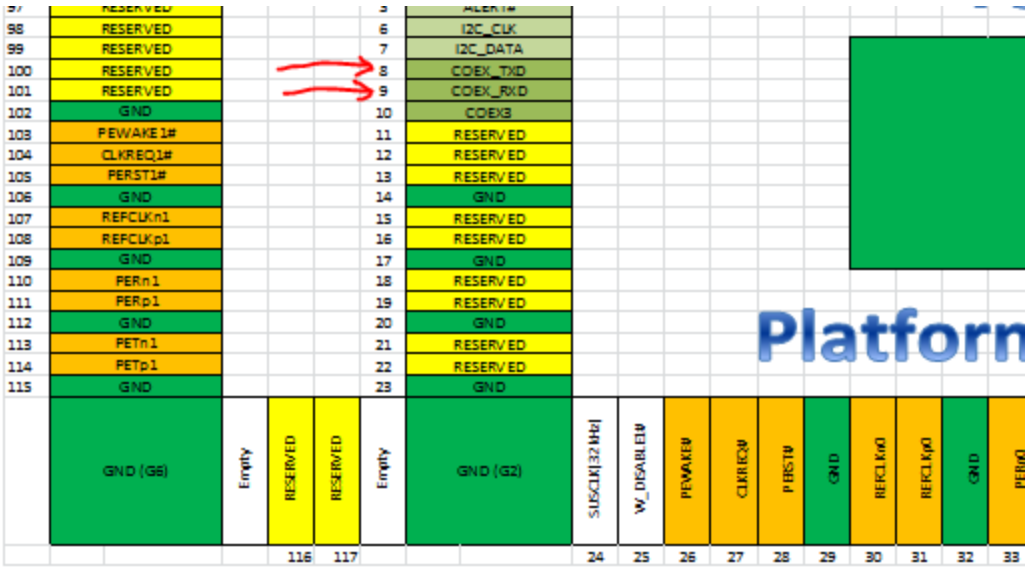


Figure 94. Type 3026 LGA Pin-
Based Pin-Out on Pl

Addition of Figure 97 to show COEX UART signal directions as follows:

Figure 95 and Figure 96 are examples of signaling directions and name changes from platform to module. Other cases exist for other signals in various Sockets, such as the USB3.0 Tx and Rx, SSIC_Tx and SSIC_Rx.

The two COEX signals between the WWAN device on Socket 2 and the Connectivity device on Socket 1 have defined directions and shown in Figure 97. At the platform, the three COEX signals should be connected pin to pin as shown in Figure 97.

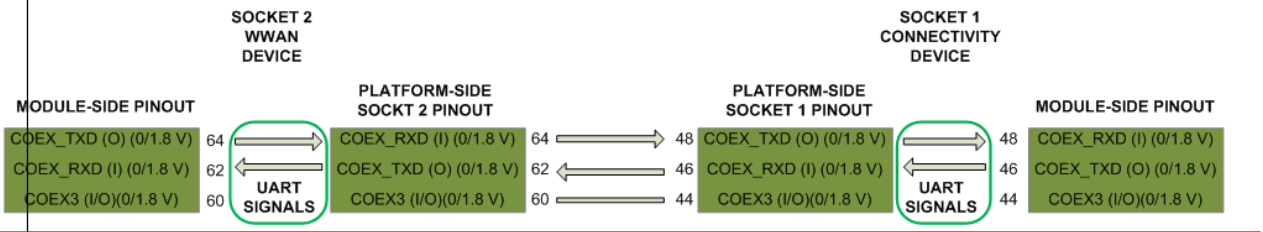


Figure 97. COEX_TXD and COEX_RDX Signal Directions

All subsequent Figure Numbers and references to figures will need to be updated. Including ToC.