PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	M.2 Signal Definition – Audio & ANTCTL Functions
DATE:	May 20, 2014 (Updated Sept 3, 2014)
AFFECTED DOCUMENT:	M.2 Spec Revision 1.0
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Part I

1. Summary of the Functional Changes

Definition of the four Audio pins to provide definitive functions assigned to each pin of the Audio interface.

Definition of the four ANTCTL pins to provide definitive functions assigned to each pin of the ANTCTL interface.

2. Benefits as a Result of the Changes

Improved Audio & ANTCTL alignment across the industry. This will allow OEM and Platfrom designers to enjoy interoperability (Mix-n-Match) of different WWAN modules through the adoption of well defined interfaces. It will also prevent potential damage/contention due to misalignment. when mixed and matched.

3. Assessment of the Impact

Should not affect current situation or current use of these signal.

4. Analysis of the Hardware Implications

None based on feedback from M.2 members survey of use and existing implementation.

5. Analysis of the Software Implications

N/A

6. Analysis of the C&I Test Implications

N/A

Part II

Detailed Description of the change

Change Table 25 as follows:

			performed.	
Supplemental Communication Specific Signal **continued…**	ANTCTL[0..3]	I/O ~~O~~	These signals are used for Antenna Control. ~~and should be routed to the appropriate Antenna Control Circuitry on the platform~~ Two modes of operation are supported: GPIO & RFFE – See section 3.2.10.5 for details	1.8 V Nominal/ 2.8 V Max
	IPC_[0..7]	I/O	Pins to facilitate IPC signals exchanged between the host and the card. Functions are BTO/CTO.	1.8 V
	AUDIO[0..3]	I/O	Pins for the use of audio. ~~Some examples of audio interfaces are SLIMBus, I2S and PCM. Functions are BTO/CTO~~ Two modes of operation are supported: I2S & SLIMBus – See section 3.2.10.3.2 for details	1.8 V
	WAKE_ON_WWAN#	O	Used to wake the platform by the WWAN device	1.8 V
	DPR	I	This signal is an input directly to the WWAN module from a suitable SAR sensor. The specific implementation will be determined by the module vendor and their customer	1.8 V

Change Chapter 3.2.10.3.2 as follows:

3.2.10.3.2. Audio Signals

AUDIO0–3

These pins are reserved for Audio use. ~~However the s~~ Specific implementations will be part of a BTO option determined specifically by the module vendor and their customers. Supported options and pin allocations are shown in Table xx.

Table xx. Audio Pin Mode & Function Assignment

M.2 Audio Pins		Pin Mode & Function					
Pin #	Pin Name	I2S Mode			SLIMBus Mode		
		Function	Direction	Voltage	Function	Direction	Voltage
20	Audio_0	I2S_CLK	I/O	1.8 V	SLIMBus_CLK	O	1.8 V
22	Audio_1	I2S_RX	I	1.8 V	SLIMBus_DAT	I/O	1.8 V
24	Audio_2	I2S_TX	O	1.8 V	Reserved		
28	Audio_3	I2S_WS	I/O	1.8 V	Reserved		

Change Chapter3.2.10.5 as follows:

3.2.10.5. Antenna Control

ANTCTRL (0-3) are provided to allow for the implementation of antenna tuning solutions. The number antenna control lines required will depend on the application and antenna/band requirements.

The functional definition of the antenna control pins are OEM-specific and should be coordinated between the host platform OEM and card vendors. The ordered labeling of these signals in this specification is intended to help establish consistent implementations—where practical—across multiple instances of cards in the host platform. Supported options and pin allocations are shown in Table xy.

Table xy. Antenna Control Pin Mode & Function Assignment

M.2 Antenna Control		Pin Mode & Function					
Pin #	Pin Name	GPIO Mode			RFFE Mode		
		Function	Direction	Voltage	Function	Direction	Voltage
59	ANTCTL0	GPIO0(LSB)	O	1.8 V[1]	Reserved		
61	ANTCTL1	GPIO1	O	1.8 V[1]	RFFE_SDATA	I/O	1.8 V
63	ANTCTL2	GPIO2	O	1.8 V[1]	RFFE_SCLK	O	1.8 V
65	ANTCTL3	GPIO3(MSB)	O	1.8 V[1]	RFFE_VIO	O	1.8 V

[1] In GPIO Mode Operating voltage for pins is 1.8 V Nominal BUT can be up to 2.8 V to allow direct operation of antenna controllers using multiple silicon technologies.