PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	System Board Eye Height Specification Update
DATE:	May 19, 2008; approved by the CEM WG 12/5/08
AFFECTED DOCUMENT:	PCI Express Card Electromechanical Specification, Revision 2.0
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Part I

1. Summary of the Functional Changes

This ECN modifies the system board transmitter path requirements (V_{TXS} and V_{TXS_d}) at 5 GT/s. As a consequence the minimum requirements for the add-in card receiver path sensitivity at 5 GT/s are also updated.

Section 4.7.4, Table 4-13: Change the minimum specification for V_{RXA} and V_{RXA_d} to 250 mV

Section 4.7.6, Table 4-15: Change the minimum specifications for V_{TXS} and V_{TXS_d} to 250 mV

2. Benefits as a Result of the Changes

These changes will relax the routing constraints on system boards, making longer trace lengths possible. This is especially important in cases where a single root complex drives multiple PCI-Express connectors, employing high density routing with both strip-line and micro-strip traces.

3. Assessment of the Impact

These changes have no impact for existing system boards, as any design which is compliant to the current specification will automatically be compliant to the updated specification as well.

These changes could have limited impact for existing add-in cards, because the requirements for the receiver path sensitivity are slightly more restrictive. However, simulations have shown that common FR4 add-in card receive path within the length range (4") and PCB impedance range (68 – 105 ohms) allowed by the 2.0 CEM specification will not cause the voltage to drop to 120 mV at the add in card pins if the system board voltage is 250 mV or greater. Exceptions could be possible with extreme discontinuities in the receive path (many vias, etc.) – but this would no be expected in reasonable implementations.

4. Analysis of the Hardware Implications

For system boards, these changes will allow longer trace lengths.

For add-in cards, these changes will reduce the attenuation allowed between the PCI-Express edge finger and PCI-Express receiver. However, for designs with form factors compliant to the PCI Express Card Electromechanical Specification, this should not limit the flexibility for receiver placement.

5. Analysis of the Software Implications

There are no changes required in the software/firmware involved in the normal operation of the PCI-Express interface.

The limits built into the compliance software for the electrical layer (SIGtest) should be updated to reflect the new eye-height specification.

Part II

Detailed Description of the change

Change Table 4-13 in Section 4.7.4, page 53 as follows:

Table 4-13: Add-in Card Minimum Receiver Path Sensitivity Requirements at 5 GT/s

Parameter	Min	Max	Unit	Comments
V_{RXA}	250	1200	mV	Notes 1, 2, 3
V_{RXA_d}	250	1200	mV	Notes 1, 2, 3
1.5 – 100 MHz RMS Jitter	3.4		ps RMS	
33 kHz Refclk Residual	75		ps PP	
< 1.5 MHz RMS Jitter	4.2		ps RMS	
1.5 – 100 MHz DJ	30		ps PP	
> 100 MHz DJ	27		ps PP	

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Change Table 4-15 in Section 4.7.6, page 58 as follows:

Table 4-15: System Board Transmitter Path Compliance Eye Requirements at 5 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXS}	250	1200	mV	Notes 1, 2, 4
V_{TXS_d}	250	1200	mV	Notes 1, 2, 4
T_{TXS} (with crosstalk)	95		ps	
T_{TXS_d} (without crosstalk)	108		ps	

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