PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Update DMTF SM CLP Specification References
DATE:	8/2009
AFFECTED DOCUMENT:	PCIFW30_CLP_1_0_071906.pdf
SPONSOR:	Austin Bolen, Dell Inc.

Part I

1. Summary of the Functional Changes

Update references to sections in the DMTF Server Management Command Line Protocol (SM CLP) Specification (DSP0214) to match the most recent version SM CLP Specification (v1.0.2).

Clarify that the references to the DMTF SM CLP specification are referencing v1.0.2.

Adds a reference to the DMTF SM CLP specification in section 1.2 Reference Documents.

No functional changes.

2. Benefits as a Result of the Changes

Clarifies DMTF specification references.

3. Assessment of the Impact

Specification clarification only.

4. Analysis of the Hardware Implications

None.

5. Analysis of the Software Implications

None.

6. Analysis of the C&I Test Implications

None.

Part II

Detailed Description of the change

Update the ECN for SM CLP (PCIFW30_CLP_1_0_071906.pdf) as follows:

5.2.1.25 DMTF Server Management Command Line Protocol (SM CLP) Support

The Option ROM may optionally provide an entry point that will support device configuration via the DMTF SM CLP standard.10 This interface will follow an API defined in the DMTF SM CLP Specification 1.0 Final Standard. This interface is accessed with a FAR CALL in Big Real mode where the system ROM will pass in a DMTF SM CLP compatible configuration message that will target the device or a child of that device. This interface may be called multiple times in order to completely configure a device during pre-boot. It is the responsibility of the System ROM to perform any discovery, enumeration, and subsequent translation of the SM CLP UFiTs for any given Container in an implementation.
The option ROM code should assume that the system firmware will call the entry point in Big Real Mode and with a minimum of 4 KB for the stack and at least 128KB of extended memory available via PMM.

Input parameters are described below:

~~ES:EDI = pointer to Command Line Protocol string buffer (NULL Terminated)~~
~~EBX = Command Status:~~
~~Bit 0: Privilege Bit:~~
~~0 = No Privileges~~
~~1 = Administrator Privileges~~
~~Bits 7-31: Reserved~~
~~Bits 15-8: Session ID~~
~~Bits 31-16: Process ID~~

Table 5-5: Input Arguments for SM CLP Entry Point

Argument Number	Register	Meaning
1	[AH]	Bus number
2	[AL]	Upper 5 bits are the Device number
3	[AL]	The lower 3 bits are the Function number
4	[ES:EDI]	Pointer to NULL-terminated SM CLP Command Line string buffer
5	[DS:ESI]	Pointer to SM CLP Command Response string buffer

AX contains the Bus/Device/Function of the source of the PCI option ROM, same as the PCI option ROM INIT and Configuration entry points described earlier in this specification. This provides an indicator of which PCI device is being targeted to the SM CLP code. If a PCI option ROM's SM CLP entry point supports more than one device as an SM CLP target, the Command Line Protocol string buffer must also be examined for target information, according the the SM ME Addressing Specification. ES:EDI points to a Command Line string as defined in the SM CLP Specification

(see section 5.1.9, "Input Data"). DS:ESI points to a buffer of at least 4K bytes in size. Strings are always NULL-terminated.

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Note: The scope of the target in the SM CLP Command Line string buffer is limited to the Address Space of the PCI device and is not expected to be scoped to the overall containing Computer System. SM CLP implementations in PCI option ROMs are expected to adhere to the SM ME Addressing Specification with the exception that Collections, Logical Devices, Computer Systems, and other Managed Elements are allowed to be in the root of the Address Space.

The output parameters are described below:

~~ES:EDI = pointer to Command Line Protocol Return string buffer (NULL Terminated)~~
~~EBX = Return Status Flags~~
~~Bit 0: Success flag~~
~~0 = Command Accepted~~
~~1 = Command Failed~~
~~Bits 7-1: Reserved (always set to 0)~~
~~Bits 15-8: Return Status Code~~
~~0 = Command Completed Successfully~~
~~1 = Command Accepted, In Progress~~
~~2 = Invalid Target Specified~~
~~3 = Target Busy~~
~~4 = Insufficient Privilege~~
~~5 = Insufficient Resources~~
~~6 = Other Failure~~
~~7 - 255 = Reserved for future use~~
~~Bits 31-16: Process ID~~

Table 5-6: Output Arguments for SM CLP Entry Point

Argument Number	Register	Meaning
1	[AH]	If [AL] = 2 (COMMAND_PROCESSING_FAILED) the contents of [AH] are derived from the SM CLP Processing Error Value (see SM CLP Specification – Table 6: Processing Error Values and Tags). If [AL] = 3 (COMMAND_EXECUTION_FAILED) the contents of [AH] are derived from the SM CLP CIM Status Code Values (see SM CLP Specification – Table 9: CIM Status Code Values and Descriptions)
2	[AL]	SM CLP Command Status (see SM CLP Specification – Table 4: Command Status Values and Tags)
3	[EAX]	Bit 31: OEM Code Flag 0 = Execution Code is ~~a~~n SM CLP Probable Cause Value (see SM CLP Specification Table 11: Probable Cause Values and Descriptions) 1 = Execution Code is an OEM Specific value
4	[EAX]	Bits 30-16: Execution Code
5	[ES:EDI]	Pointer to NULL-terminated SM CLP

		Command Line string buffer
6	[DS:ESI]	Pointer to NULL-terminated SM CLP Command Response string buffer

AL contains 0 for a successful command completion status. If AL is returned with a value of 2, a command processing error is signified and AH will contain a code signifying the cause of the processing error. If AL is returned with a value of 3, an execution error has occurred and the upper 16-bits of EAX will contain an execution error code. Bit 31 of EAX specifies whether the Execution Code is an SM CLP defined code or an OEM-specific code. The string buffer pointers (ES:EDI and DS:ESI) and the contents of the SM CLP Command Line string buffer are preserved. The SM CLP Command Response string buffer is filled in by the option ROM in the "keyword=value" format described in the SM CLP Specification (see section 5.1.10, "Output Data"), unless otherwise requested via the SM CLP –output option in the Command Line string buffer. Option ROM support for this default "keyword=value" output format is required, while support for other SM CLP output formats is optional (the SM CLP option ROM should return an OPTION NOT SUPPORTED error in AH if the SM CLP –output option requested by the caller is not supported by the option ROM).

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All other x86 registers are preserved.

Note that not all PCI 3.0 system firmware will support calling the DMTF SM CLP entry point. The support for this function can be determined by examining the results of the "PCI BIOS Present" call described in Section 2.5.2. This is useful for diagnostics and validation in determining if the DMTF SM CLP interface will be used. In addition an Expansion ROM may change its configuration behavior if it determines that the PCI 3.0 system firmware will not call the DMTF SM CLP API. Similarly an Expansion ROM is not required to have a DMTF SM CLP entry point. If the entry point is not present, the "Pointer to the DMTF SM CLP entry point" field in the PCI Data Structure (see Section 5.2.1) should be null.

The normal power-up sequence concerning SM CLP is as follows:

1) **An SM CLP configuration session is started via a remote console.**
2) **The system ROM facilitates the configuration of the PCI device(s) by passing SM CLP commands via the SM CLP Entry Point interface.**
3) **The Expansion ROM SM CLP code stores the configuration settings in a non-volatile location associated with the targeted PCI device so that the configuration information is available to the PCI device's option ROM Init code on current and subsequent boots.**
4) **The system ROM initializes the PCI device(s) by calling the PCI Expansion ROM Init entry point.**

Note: SM CLP configuration sessions that occur after the PCI Expansion ROM Init code has executed may require the system to be rebooted so that the new configuration changes can take effect.

Update Footnote at bottom of page 91 as follows:

10 This document references v1.0.2 of the DMTF SM CLP Specification which is available from the DMTF group at http://www.dmtf.org/standards/published_documents/DSP0214_1.0.2.pdf ~~apps/org/workgroup/svrmgmt/ in the~~

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http://www.dmtf.org/standards/smash.

~~Server Management Working Group. The PCI 3.0 Firmware Specification defers to the DMTF specification for any differences in description or implementation.~~

Add a reference to the DMTF SM CLP Specification in Section 1.2 Reference Documents as follows:

DMTF Server Management Command Line Protocol (SM CLP) Specification, v1.0.2, Document Number DSP0214, March 7, 2007,
http://www.dmtf.org/standards/published_documents/DSP0214_1.0.2.pdf