PCI-SIG ENGINEERING CHANGE NOTICE

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|---|---|
| **TITLE:** | Separate Refclk Independent SSC Architecture (SRIS) |
| **DATE:** | Updated 10 January 2013 |
| **AFFECTED DOCUMENT:** | PCI Express Base Spec. Rev. 3.0 |
| **SPONSOR:** | Intel, HP, AMD |

# Part I

## 1. Summary of the Functional Changes

Provide specifications to enable separate Refclk with Independent Spread Spectrum Clocking (SSC) architecture.

Below is a summary of changes made to the base spec:

1. Section 4.2.5.6: Says no L0s support.
2. Section 4.2.7: Some explanation of the new option with independent SSC clocks.
3. Section 4.2.7.3 and 4.2.7.4: SKP Ordered Set frequency updates.
4. Section 4.3.7.4: Changes in electrical sub-block for 2.5 and 5.0 GT/s Separate Refclk No SSC architecture.
5. New Section 4.3.7.5: Changes in electrical sub-block for 2.5 and 5.0 GT/s Separate Refclk Independent SSC architecture.
6. Section 4.3.8.4: Changes in electrical sub-block for 8.0 GT/s Separate Refclk No SSC architecture.
7. New Section 4.3.8.5: Changes in electrical sub-block for 8.0 GT/s Separate Refclk Independent SSC architecture.

## 2. Benefits as a Result of the Changes

Provide technical details to enable a valuable clocking architecture that is mentioned in the spec but currently without any enabling detail. In particular, this separate Refclk with independent SSC architecture can be used to enable a new class of PCIe applications involving cables without needing complex system level solutions for EMI/RFI containment.

## 3. Assessment of the Impact

There is no impact on transmitter and Refclk components. An existing transmitter and Refclk that are PCIe spec compliant can be used in the separate Refclk with independent SSC architecture without any change.

An existing receiver that is designed for the common refclk architecture, however, may not function in the separate Refclk with independent SSC architecture. It may need to be modified. Jitter analysis needs to be performed with modified behavioral CDR jitter transfer functions; Refclk and receiver compliance tests need to be modified slightly. The body of this ECR describes the specific changes.

It is emphasized that this ECR is optional.

Such silicon can and will continue to be used for the CEM, MiniCard, or any other existing form factor that does not require the separate Refclk with independent SSC. *However, the silicon (Rx) that supports the separate Refclk with independent SSC will work in any existing PCIe application with the common Refclk architecture.*

This ECR is intended to enable the separate refclk with independent SSC architecture to broaden the PCIe applications, mainly for cabling. The applications that take advantage of this architecture will be in different form factors or connectors from the currently existing PCIe form factors or connectors, and there is not any interoperability requirement between the "new" and "old" form factors/connectors. System OEMs should be able to manage the two silicon SKUs.

When PCIe electrical switches, redrivers, or repeaters are concerned, there may be the following impacts:

- There is no impact to the passive switch since it includes no Rx. The electrical switch that is currently used in the common Refclk architecture may continue to be used for the separate Refclk with independent SSC architecture.

- It is not expected that this ECR will have any impact to existing redrivers that do not do retiming. The redriver that is currently used in the common Refclk architecture may continue to be used for the separate Refclk with independent SSC architecture.

- For repeaters that do retiming, the existing parts that are designed for the common Refclk architecture will not generally work for the separate Refclk with independent SSC; a new repeater will be required that meet requirements outlined in this ECR. System OEMs will manage those repeater SKUs.

## 4. Analysis of the Hardware Implications

1. Receiver's elastic buffer will need to be deeper to handle the timing skew created by independent SSC.

2. Informative Gen2 receiver's CDR jitter transfer function needs to be second order high-pass with -3dB frequency at 5MHz.

3. Informative Gen3 receiver's CDR jitter transfer function needs to be second order high-pass with -3dB frequency at 10MHz.

## 5. Analysis of the Software Implications

None. It is required that the system is set up through hardware or implementation-specific firmware to operate with independent reference clocks with SSC.

## 6. Analysis of the C&I Test Implications

1. Refclk jitter should be tested with new behavioral CDR jitter transfer function. Currently compliant Refclk should pass without further efforts.

2. Receiver stress tests should be performed with separate Refclk and independent SSC enabled. This should not cause any issue with test equipment (BERT in this case) since SSC can be enabled or disabled easily. For a discrete clock chip on the DUT's test board, however, some kind of hardware strap or software control via I2C may be needed.

3. Some previously Reserved fields are now defined.

## Part II

**Detailed Description of the change**

*Change Section 4.2.5.6, page 245 as follows:*

### 4.2.5.6. L0s

L0s is intended as a power savings state. When operating with separate reference clocks with independent ~~SSC~~ (Spread Spectrum Clocking (SSC)) ~~mode~~ (see Section 4.2.7), L0s is not supported and must not be advertised in the capability registers. See Section 4.3.7.3 for a definition of SSC.

*Change Section 4.2.7, page 314 as follows:*

### 4.2.7. Clock Tolerance Compensation

SKP Ordered Sets (defined below) are used to compensate for differences in frequencies between bit rates at two ends of a Link. The Receiver Physical Layer logical sub-block must include elastic buffering which performs this compensation. The interval between SKP Ordered Set transmissions is derived from the absolute value of the Transmit and Receive clock frequency difference specified in Table 4-18. ~~Having worse case clock frequencies at the limits of the tolerance specified will result in a 600 ppm difference between the Transmit and Receive clocks of a Link. As a result, on average, the Transmit and Receive clocks can shift one clock every 1666 clocks.~~
The specification supports two kinds of clocking where the Tx and Rx Refclk rates differ. One allows for a worst case 600 ppm difference with no SSC (Separate Reference Clocks With No SSC - SRNS), and the other for a 5600 ppm difference for separate refclks utilizing independent SSC (Separate Reference Clocks with Independent SSC - SRIS) (SSC introduces a 5000 ppm difference, and Tx/Rx crystal tolerance introduces another 600 ppm). Note that the common Refclk architecture utilizes the same Refclk for Tx and Rx and so does not introduce any difference between the Tx and Rx Refclk rates.

Specific form factor specifications are permitted to require the use of only SRIS, only SRNS, or to provide a mechanism for clocking architecture selection. Upstream Ports are permitted to implement support for any combination of SRIS and SRNS (including no support for either), but must conform to the requirements of any associated form factor specification. Downstream Ports supporting SRIS must also support SRNS unless the port is only associated with a specific form factor(s) which modifies these requirements. Port configuration to satisfy the requirements of a specific associated form factor is implementation specific.

If the clock tolerance is 600 ppm, on average, the Tx and Rx clocks can shift one clock every 1666 clocks. If the clock tolerance is 5600 ppm, a shift of one clock can occur every 178 clocks.

If the receiver is capable of operating with SKP Ordered Sets being generated at the rate used in SRNS even though the Port is running in SRIS, the Port is permitted to Set its bit for the appropriate data rate in the Lower SKP OS Reception Supported Speeds Vector field of the Link Capabilities 2 register. If the transmitter is capable of operating with SKP Ordered Sets being generated at the rate used in SRNS even though the Port is running in SRIS, the Port is permitted to Set its bit for the appropriate data rate in the Lower SKP OS Generation Supported Speeds Vector field of the Link Capabilities 2 register. System software must check that the bit is Set in the Lower SKP OS Reception Supported Speeds Vector field before setting the appropriate data rate's bit in the link partner's Enable Lower SKP OS Generation Vector field of the Link Control 3 register. Any software transparent extension devices (such as a repeater) present on a Link must also support lower SKP OS Generation for system software to set the bit in the Enable Lower SKP OS Generation Vector field. Software determination of such support in such extension devices is implementation specific. When the bit for the data rate that the link is running in is Set in the Enable Lower SKP OS Generation Vector field, the transmitter schedules SKP Ordered Set generation in L0 at the rate used in SRNS, regardless of which clocking architecture the link is running in. In other LTSSM states, SKP Ordered Set scheduling is at the appropriate rate for the clocking architecture.

Components supporting SRIS may need more entries in their elastic buffers than designs supporting SRNS only. This requirement takes into account the extra time it may take to schedule a SKP Ordered Set if the latter falls immediately after a maximum payload sized packet.

*Change Section 4.2.7.3, page 316 line 11as follows:*

…

- When using 8b/10b encoding: If the Link is operating in SRNS, or in SRIS and the bit corresponding to the current Link speed is Set in the Enable Lower SKP OS Generation Vector field, and the LTSSM is in L0, a SKP Ordered Set must be scheduled for transmission at an interval between 1180 and 1538 Symbol Times. If the Link is operating in SRIS and either the bit corresponding to the current Link speed is Clear in the Enable Lower SKP OS Generation Vector field or the LTSSM is not in L0, a SKP Ordered Set must be scheduled for transmission at an interval of less than 154 Symbol Times.

- When using 128b/130b encoding: If the Link is operating in SRNS or in SRIS and the bit corresponding to the current Link speed is Set in the Enable Lower SKP OS Generation Vector field and the LTSSM is in L0, a SKP Ordered Set must be scheduled for transmission at an interval between 370 to 375 blocks, when the LTSSM is not in the Loopback state or is a Loopback Slave that has not started looping back the incoming bit stream. If the Link is operating in SRIS and either the bit corresponding to the current Link speed is Clear in the Enable Lower SKP OS Generation Vector field or the LTSSM is not in L0, a SKP Ordered Set must be scheduled for transmission at an interval less than 38 blocks, when the LTSSM is not in the Loopback state or is a Loopback Slave that has not started looping back the incoming bit stream. When the LTSSM is in the Loopback state and the Link is operating in SRNS, the Loopback Master must schedule two SKP Ordered Sets to be transmitted, at most two blocks apart from each other, at an interval between 370 to 375 blocks. When the LTSSM is in the Loopback state and the Link is operating in SRIS, the Loopback Master must schedule two SKP Ordered Sets to be transmitted, at most two blocks apart from each other, at an interval of less than 38 blocks.

…

*Change Section 4.2.7.4, page 317, line 5 as follows:*

…

Receivers shall be tolerant to receive and process SKP Ordered Sets at an average interval between 1180 to 1538 Symbol Times when using 8b/10b encoding and 370 to 375 blocks when using 128b/130b encoding when the Link is operating in SRNS or in SRIS and its bit for the current Link speed is Set in the Lower SKP OS Reception Supported Speeds Vector field. Receivers shall be tolerant to receive and process SKP Ordered Sets at an average interval of less than 154 Symbol Times when using 8b/10b encoding and less than 38 blocks when using 128b/130b encoding when the Link is operating in SRIS.

…

*Add Section 4.3.4.4.6 as follows:*

#### 4.3.4.4.6. Separate Refclk with Independent SSC (SRIS) RX Architecture

The testing of the Separate Refclk with Independent SSC RX Architecture is the same as the Common clock architecture with the following modifications:

- The DUT shall be driven with an independent SSC modulated reference clock for all testing. SSC shall meet the frequency limits and maximum deviation range defined in table 4-34.
- The generator shall be driven with an independent SSC modulated reference clock for the stressed voltage test. SSC shall have a triangular profile and meet the frequency limits and maximum deviation range defined in table 4-34.
- The generator shall provide a 33 kHz Sj tone with 25 ns peak to peak amplitude during the stressed eye test.
- The generator shall transmit with a nominal unit interval of 125 ps + 2500 PPM during the stressed eye test.
- Sj shall be swept over the range shown in Figure 4-x0 during the stressed eye test:

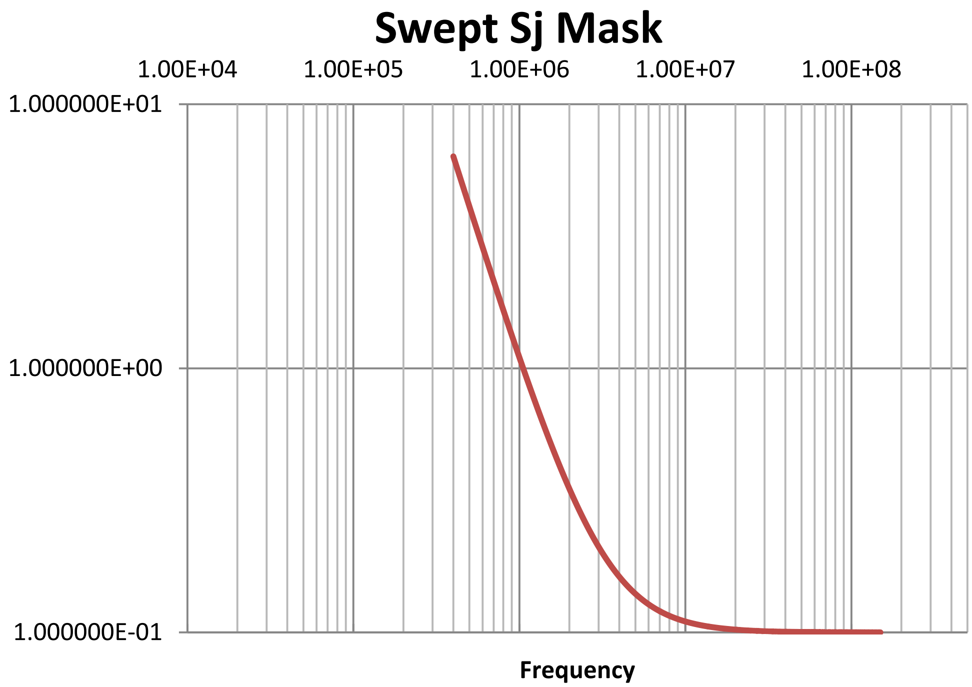


**Figure 4-x0: Swept Sj Mask**

*Change Section 4.3.7.3, page 401 as follows:*

### 4.3.7.3. Bit Rate Tolerance and Spread Spectrum Clocking

The tolerance for the Refclk is 100 MHz ±300 ppm, where this number is defined with spread spectrum clocking (SSC) turned off. SSC may be implemented as a method of reducing EMI. The Refclk rate for a single source may be modulated from +0 to -5000 ppm of the nominal data rate frequency, at a modulation rate lying within a 30 kHz – 33 kHz range. The maximum rate of change of the frequency on a reference clock with SSC active is 1250 ppm/µs.

*Change Section 4.3.7.4 as follows:*
*Note: The new section 4.3.7.5 is based on this section. To simplify reviewing, this section is reproduced entirely in this ECN, even though much of it is unchanged.*

### 4.3.7.4. Separate Refclk with No SSC (SRNS) Architecture

It is also possible to architect a PCI Express implementation with separate Refclk sources for the Tx and Rx. Since this architecture employs two independent clock sources, the amount of jitter impinging on the Receiver is the RSS sum, rather than the difference of the PLL transfer characteristics. As a consequence, the jitter requirements for the Refclks in a separate Refclk architecture are substantially tighter than for a common Refclk Rx architecture. Furthermore, it is not in general possible to guarantee interoperability between separate Refclk architecture components and those using other clock architectures. T~~t~~his specification does not explicitly define the requirements for separate Refclk architecture, but instead will defer to the appropriate form factor specification.

When tolerancing a PCI Express Rx in this separate Refclk architecture, the generator and DUT are furnished with separate Refclks that each are within ±300 PPM of the nominal frequency of 100 MHz. SSC must be turned off for both Refclk sources. These limitations are required to guarantee proper operation of the buffering and flow control in the Rx.

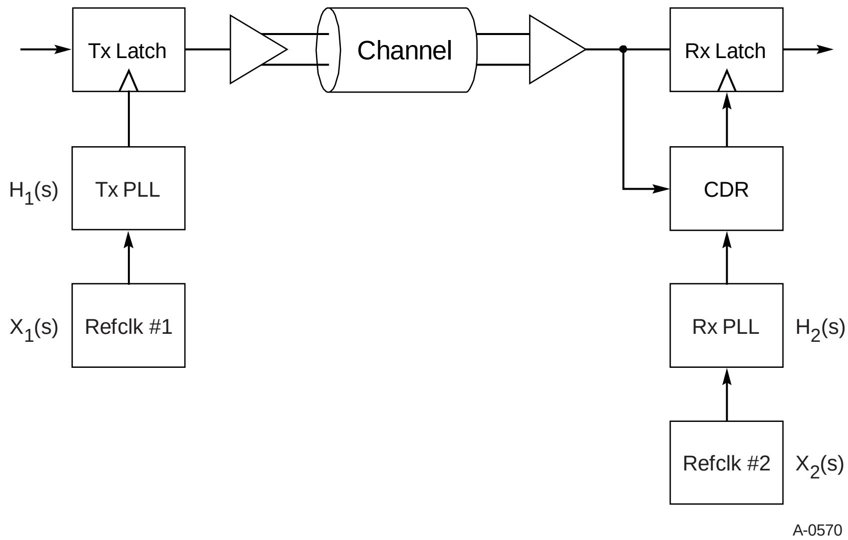


**Figure 4-92: Separate Refclk With No SSC (SRNS) Architecture**

The impact of tighter Refclk margins for the separate Refclk architecture may be seen by examining the phase jitter transfer equations below. Since both Refclks are independent, their phase jitter is passed through the Tx and Rx PLLs independently, and the maximum PLL BW/peaking of 16 MHz/3 dB must be assumed. Additionally, since both Tx and Rx Refclks are independent, their Rj terms add as an RSS value. Consequently, the jitter characteristics for the separate Refclk architecture must be considerably tighter than for the other two architectures.

$$H_1(s)=\left[\frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2}\right] \quad H_2(s)=\left[\frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2}\right]$$

**Equation 4.3.6**

$$X_{SC}(s)=\sqrt{\left[X_1(s)*H_1(s)\right]^2+\left[X_2(s)*H_2(s)\right]^2}$$

*Add Section 4.3.7.5 as follows:*
*Note: The text in this section is based onSection 4.3.7.4. Reviewers may wish read the two sections together.*

## 4.3.7.5. Separate Refclk with Independent SSC (SRIS) Architecture

It is also possible to architect a PCI Express implementation with separate Refclk sources with independent SSC for the Tx and Rx. This architecture employs two independent clock sources each having independent spread spectrum clocking (SSC). The Receiver must be able to track and reject the resultant phase drift between the Tx and Rx. Changes in the logical sub-block are also required for this separate Refclk with Independent SSC architecture; refer to the logical sub-block section for all relevant information concerning SRIS (sections 4.2.5.6, 4.2.7, 4.2.7.3 and 4.2.7.4).

Figure 4-92a below shows the block diagram of the separate Refclk architecture. Since Refclk #1 and Refclk #2 are independent from each other, their respective jitter at the Rx Latch are simply X1(s)*H1(s)*H_CDR(s) and X2(s)*H2(s)*H_CDR(s); where H_CDR(s) is the CDR's jitter transfer function. However, since Refclk jitter is primarily Rj, their combined impact should be the Root Sum Square (RSS) of the individual terms.

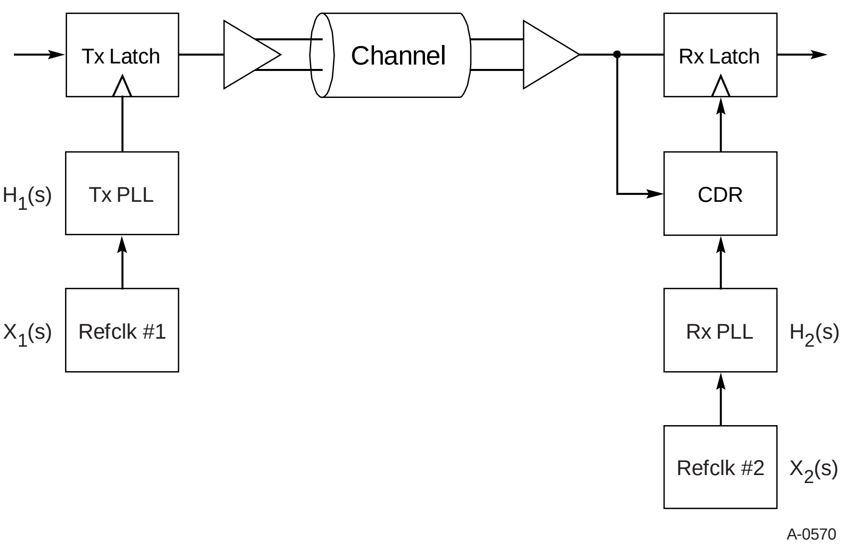


**Figure 4-92a: Separate Refclk With Independent SSC Architecture**

For the separate Refclk with independent SSC architecture, the informative CDR jitter transfer function is a second order high-pass function with the -3 dB corner frequency at 5 MHz, see Figure 4-9x1 and Equation 4.3.7.

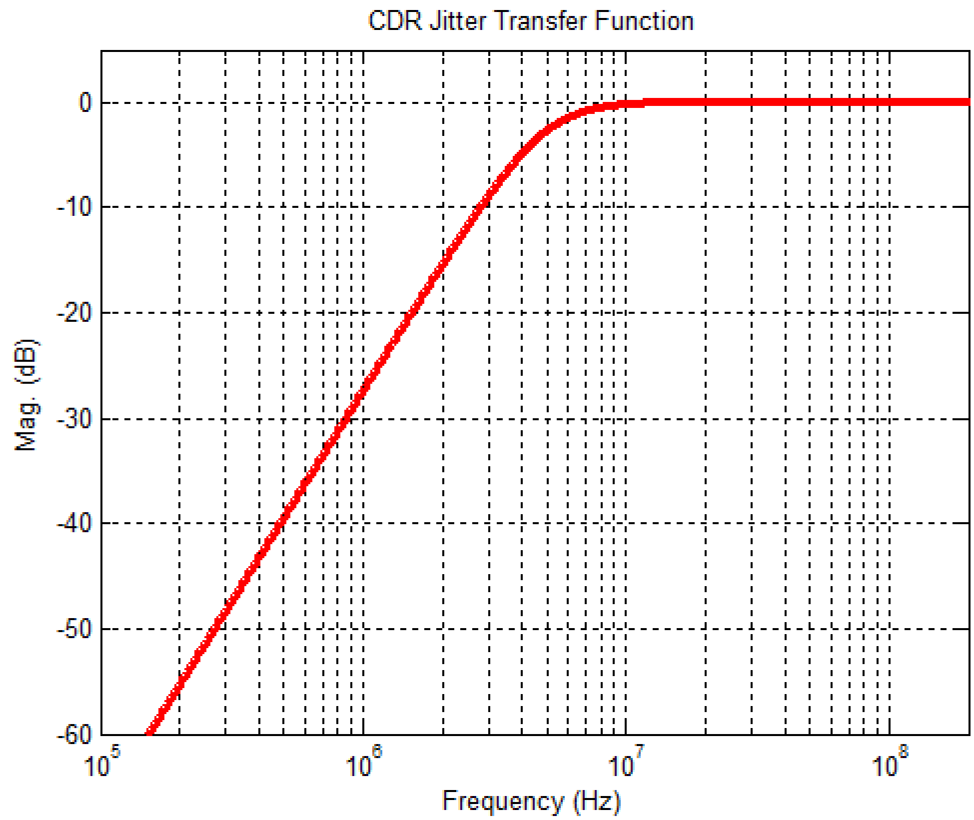


**Figure 4-x1: Informative CDR Jitter Transfer Function for the Separate Refclk with Independent SSC (SRIS) Architecture at 5.0 GT/s**

$$H_{JTF}(s) = \frac{s^2}{s^2+2\zeta\omega_m s+\omega_m{}^2}$$

**Equation 4.3.7**

**where** $f_m = \frac{2*5.0\ \mathrm{MHz}}{\sqrt{1+2\zeta^2+\sqrt{1+(1+2\zeta^2)^2}}}$ $\zeta = .707$ **and** $\omega_m = 2\pi f_m$.

**Table 4-x1: Parameters for Separate Refclk With Independent SSC Architecture (SRIS) at 5.0 GT/s**

| Symbol | Description | Limits | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $F_{REFCLK}$ | Refclk frequency | 99.97 | 100.03 | MHz |
| $T_{REFCLK\text{-}RMS\text{-}SRIS}$ | RMS Refclk jitter for Separate Refclk Independent SSC architecture[1] | | 2.0 | ps RMS |
| $F_{SSC}$ | SSC frequency range | 30 | 33 | kHz |
| $T_{SSC\text{-}FREQ\text{-}DEVIATION}$ | SSC deviation | | +0.0/-0.5 | % |

Notes:

1. The Refclk jitter is measured after applying PLL transfer function (16 MHz, 2 dB) and CDR jitter transfer function defined in Figure 4-9x1.

~~1.~~2. The maximum rate of change of the clock frequency is 1250 ppm/μs.

**Table 0-x2: Informative Total Jitter Budget for 5.0 GT/s Signaling for Separate Refclk With Independent SSC (SRIS) Architecture**

| **Jitter Contribution** | **Max Dj (ps)** | **Tj at BER 1e-12 (ps)** |
|---|---|---|
| Tx + Refclk #1 | 30 | 64.5 |
| Media | 58 | 58 |
| Rx + Refclk #2 | 63.2 | 97.7 |

To summarize, a PCI Express link at 5.0 GT/s can be built using the separate Refclk with independent SSC architecture. Relative to the common Refclk architecture, the only electrical specification changes at 5.0 GT/s are the receiver CDR's jitter transfer function (Figure 4-9x1), the resulting Refclk jitter number (Table 4-x1), and the requirement to test the receiver with separate reference clocks with independent SSC enabled.

*Note: The new section 4.3.8.5 is based on this section. To simplify reviewing, this section is reproduced entirely in this ECN, even though much of it is unchanged.*

*Change Section 4.3.8.4, pages 412 as follows:*

#### 4.3.8.4. Separate Refclk with No SSC (SRNS) Architecture

The 8.0 GT/s PCI Express Base Specification does not explicitly define the requirements for a separate Refclk architecture. This is the identical position taken by the base specification for 2.5 GT/s and 5.0 GT/s.

When tolerancing a PCI Express Rx in this separate Refclk architecture, the generator and DUT are furnished with separate Refclks that each are within ±300 PPM of the nominal frequency of 100 MHz. SSC must be turned off for both Refclk sources. These limitations are required to guarantee proper operation of the buffering and flow control in the Rx.

*Add Section 4.3.8.5 as follows:*

#### 4.3.8.5. Separate Refclk With Independent SSC (SRIS) Architecture

It is possible to architect an 8.0 GT/s PCI Express implementation with separate Refclk sources with independent SSC for the Tx and Rx. Figure 4-92a shows a high level block diagram of the separate Refclk architecture. Since this architecture employs two independent clock sources, the Receiver must be able to track and reject the phase drift due to the two independent SSC clocks. Changes in the logical sub-block are also required for the separate Refclk architecture; please refer to the logical sub-block section for all relevant information concerning SRIS (see Sections 4.2.5.6, 4.2.7, 4.2.7.3 and 4.2.7.4).

For the common Refclk architecture, the 8.0 GT/s specification contains a behavioral CDR model shown in Figure 4-67; it is a first order high-pass function with the -3dB corner frequency at 10MHz. Furthermore, during the receiver stressed jitter test (section 4.3.4.4), the receiver's CDR bandwidth and its low frequency jitter tracking capability are required to pass the jitter mask (Figure 4-74). For the separate Refclk with independent SSC architecture, the CDR needs to have a second order high-pass behavior to reject the extra phase drift due to independent SSC. This new behavioral CDR jitter transfer function is shown in Figure 4-9x2 and Equation 4.3.8. The stressed jitter test is also modified to account for the requirement that the CDR can reject jitter from two separate reference clocks with SSC. Other test parameters and requirements such as transmitter jitters (Table 4-19) and the receive stressed voltage eye (Table 4-22) remain unchanged.

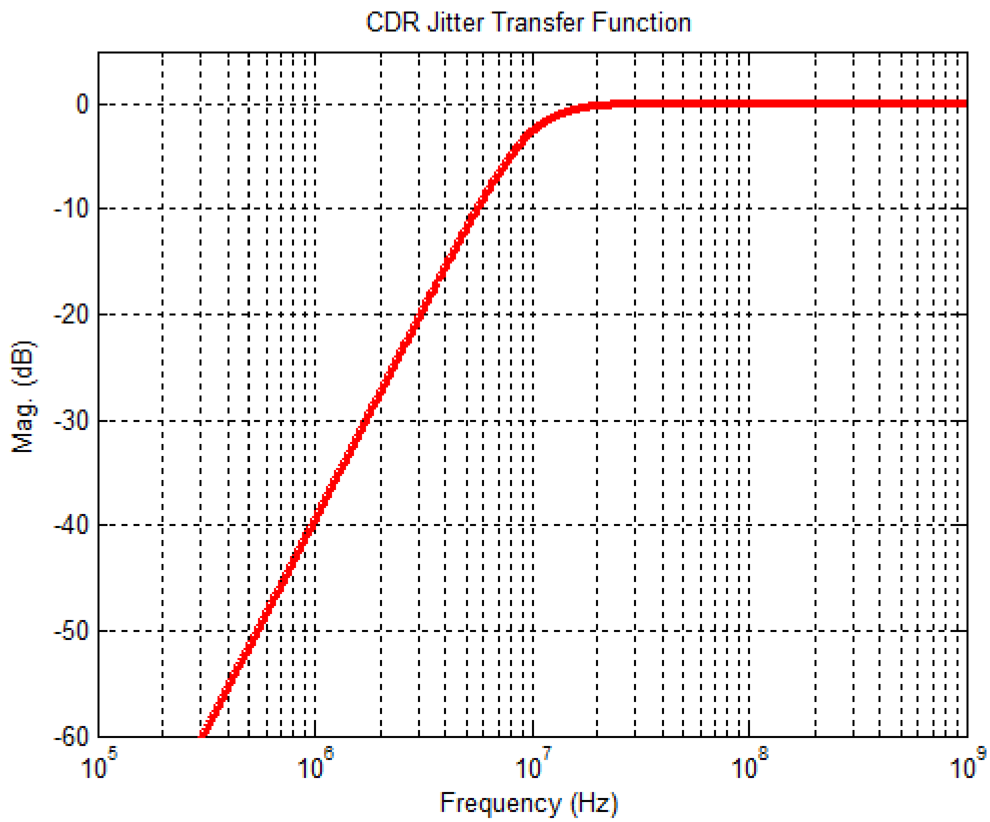


**Figure 4-9x2: Informative CDR Jitter Transfer Function for the Separate Refclk With Independent SSC (SRIS) Architecture at 8.0 GT/s**

$$H_{JTF}(s) = \frac{s^2}{s^2+2\zeta\omega_m s+\omega_m{}^2}$$ **Equation 4.3.8**

**where** $f_m = \frac{2*10.0\ \text{MHz}}{\sqrt{1+2\zeta^2+\sqrt{1+(1+2\zeta^2)^2}}}$ $\zeta = .707$ **and** $\omega_m = 2\pi f_m$.

The new CDR jitter transfer function impacts the Refclk jitter specification. This Refclk jitter number is captured as $T_{REFCLK\text{-}RMS\text{-}SRIS}$ in Table 4-9x2.

**Table 4-9x2: Parameters for Separate Refclk With Independent SSC (SRIS) Architecture at 8.0 GT/s**

| Symbol | Description | Limits | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $F_{REFCLK}$ | Refclk frequency | 99.97 | 100.03 | MHz |
| $T_{REFCLK-RMS-SRIS}$ | RMS Refclk jitter for separate Refclk independent SSC architecture[1] | | 0.5 | ps RMS |
| $F_{SSC}$ | SSC frequency range | 30 | 33 | kHz |
| $T_{SSC-FREQ-DEVIATION}$ | SSC deviation | | +0.0/-0.5 | % |

Notes:

1. The Refclk jitter is measured after applying PLL transfer function (4 MHz, 2 dB) and CDR jitter transfer function defined in Figure 4-9x2.
2. The maximum rate of change of the clock frequency is 1250 ppm/µs.
3. The maximum rate of change of the clock phase is 3 ns/µs.

*In Section 7.8.18, modify Table 7-26 as follows, make corresponding changes to figure 7-27:*

## 7.8.18. Link Capabilities 2 Register (Offset 2Ch)

…

**Table 7-26: Link Capabilities 2 Register**

| Bit Location | Register Description | Attributes |
|---|---|---|
| 9:15 | **Lower SKP OS Generation Supported Speeds Vector** – If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate.<br><br>Bit definitions within this field are:<br><br>Bit 0 2.5 GT/s<br>Bit 1 5.0 GT/s<br>Bit 2 8.0 GT/s<br>Bits 6:3 RsvdP<br><br>Multi-Function devices associated with an Upstream Port must report the same value in this field for all Functions.<br><br>Behavior is undefined if a bit is Set in this field and the corresponding bit is not Set in the Supported Link Speeds Vector. | Hwinit/RsvdP |

| | | |
|---|---|---|
| 16:22 | **Lower SKP OS Reception Supported Speeds Vector** – If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS.<br><br>Bit definitions within this field are:<br><br>Bit 0 2.5 GT/s<br>Bit 1 5.0 GT/s<br>Bit 2 8.0 GT/s<br>Bits 6:3 RsvdP<br><br>Multi-Function devices associated with an Upstream Port must report the same value in this field for all Functions.<br><br>Behavior is undefined if a bit is Set in this field and the corresponding bit is not Set in the Supported Link Speeds Vector. | Hwinit/RsvdP |

*Modify Section 7.27 as follows:*

## 7.27. Secondary PCI Express Extended Capability

The Secondary PCI Express Extended Capability structure must be implemented in any Function or RCRB where any of the following are true:

- The Supported Link Speeds Vector field indicates that the Link supports Link Speeds of 8.0 GT/s or higher (see Section 7.8.18 or 7.14.2).
- Any bit in the Lower SKP OS Generation Supported Speeds Vector field is Set (see Section 7.8.18)

~~is required for all ports and RCRbs that support a Link speed of 8.0 GT/s or higher.~~ To support future additions to this capability, this capability may be present in any Function or RCRB associated with a Link. For a Multi-Function Device associated with an Upstream Port~~s~~, this capability ~~must be implemented~~ is present only in Function 0 of the Device ~~and must not be implemented in other Functions~~.

*In Section 7.27.2, modify Table 7-114 as follows, make the corresponding changes to Fiture 7-134:*

### 7.27.2. Link Control 3 Register (Offset 04h)

…

**Table 7-114: Link Control 3 Register**

| Bit Location | Register Description | Attributes |
|---|---|---|
| … | | |

| | | |
|---|---|---|
| 9:15 | **Enable Lower SKP OS Generation Vector –** When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. See section 4.2.7 for additional requirements.<br><br>Bit definitions within this field are:<br><br>Bit 0 2.5 GT/s<br>Bit 1 5.0 GT/s<br>Bit 2 8.0 GT/s<br>Bits 6:3 RsvdP<br><br>Bits in this field are RW if the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is Set, otherwise they are permitted to be hardwired to 0.<br><br>Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not Set.<br><br>The default value of this field is 000 0000b. | RW/RsvdP |