PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	PLL Bandwidth Test Limits
DATE:	Updated 24 January 2014
AFFECTED DOCUMENT:	PCI Express Architecture PHY Test Specification 3.0
SPONSOR:	PCI-SIG Serial Enabling Workgroup (SEG)

Part I

1. Summary of the Functional Changes

Modifies the limits used by the PLL bandwidth test to allow guardband for a single PLL test solution to be used at PCI-SIG compliance workshops without impacting pass/fail results for member companies.

2. Benefits as a Result of the Changes

Allow a single PLL test solution to be used at PCI-SIG compliance workshops without impacting pass/fail results for member companies.

3. Assessment of the Impact

4. Analysis of the Hardware Implications

None.

5. Analysis of the Software Implications

None.

6. Analysis of the C&I Test Implications

Allow a single PLL test solution to be used at PCI-SIG compliance workshops without impacting pass/fail results for member companies.

Part II

Detailed Description of the change

Modify Section 2.1.12 as follows:

…

7. The -3 dB point must fall between the frequencies specified for the current data rate and the maximum peaking must be less than maximum allowed peaking for the current data rate. When testing is done at PCI-SIG compliance workshops ~~with a single test solution~~ a relaxation of +/- 0.5 MH~~h~~z on bandwidth limits and +0.25 dB on the peaking are allowed against the specified pass/fail value to allow~~account~~ for test equipment variation.