PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	L1 PM Substates with CLKREQ, Revision 1.0a
DATE:	Last Modified ~~15 Aug 2012~~ 31 May 2013; Protocol Workgroup Final Approval: 23 Aug 2012 Errata for Rev 1.0a PWG approved 30 May 2013
AFFECTED DOCUMENTS:	PCI Express Base Specification Revision 3.0, PCI Express Base Specification Revision 2.1, PCI Express Mini Card Electromechanical Specification Revision 1.2, PCI Express Card Electromechanical Specification Revision 2.0, 8.0 GT/s Receiver Impedance ECN
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Part I

1. Summary of the Functional Changes

This ECR defines an optional mechanism, that establishes, depending on implementation, one or more substates of the L1 Link state, which allow for dramatically lower idle power, including near complete removal of power for high speed circuits. The new L1 PM Substates are applicable in both the ASPM and PCI-PM L1 Link states. L1 PM Substate management utilizes a per-Link sideband signal called CLKREQ#. For those implementations that already have a CLKREQ# signal, the CLKREQ# signal is repurposed and results in no new pins being required. For other implementations, the CLKREQ# signal needs to be added; the number of pins and associated routing linearly scales with the number of Ports.

As noted above, this ECN defines functionality based on the use of CLKREQ#. A subsequent ECN is planned to define an in-band mechanism that would provide similar capabilities to those defined in this ECN using CLKREQ#.

2. Benefits as a Result of the Changes

Current PCIe specifications do not provide mechanisms to enable very lower power consumption when a PCIe Link is idle. This limits the application of PCIe technologies in low-power and battery-based applications such as embedded, handheld and tablet computers. It also leads to excessive power waste in high-lane-count PCIe solutions such as desktops, servers, storage, and PCIe Switch-based solutions. Further, with the growing world-wide attention to power efficiency, economic as well as increased regulatory requirements are driving the need to enhance the PCIe specifications to reduce idle power consumption.

3. Assessment of the Impact

The new mechanism impacts all components that support this optional capability. The new mechanism is only enabled when supported by both Ports on a Link and the Link itself (due to the required sideband signal). If any component does not support the capability, then the capability must not be enabled and the solution continues to operate using the existing legacy L1 semantics.

4. Analysis of the Hardware Implications

This ECR applies to the Link power control and reference clock mechanisms associated with a Link between an Upstream Port and a Downstream Port. See (1) above.

PHY power gating mechanisms must be added to take advantage of the PHY power savings opportunities enabled by this optional capability.

All Port and component state must be preserved in all L1 PM Substates to the same degree as required in L1 without these new mechanisms.

CLKREQ# is added as an optional pin on the CEM connector.

5. Analysis of the Software Implications

Capability discovery and enabling are required.

6. Analysis of the C&I Test Implications

Optional normative functionality will be subject to C&I tests as required for optional features.

Part II

Detailed Description of the change

4.2.6.4.1. Recovery.RcvrLock

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The Transmit Margin field of the Link Control 2 register is sampled on entry to this substate and becomes effective on the transmit package pins within 192 ns of entry to this substate and remains effective until a new value is sampled on a subsequent entry to this substate from L0, L0s, or L1.

• After activating any inactive Lane, the Transmitter must wait for its TX common mode to settle before exiting Electrical Idle and transmitting the TS1 Ordered Sets with the following exceptions.

- When exiting from the L1.2 L1 PM Substate, common mode is permitted to be established passively during L1.0, and actively during Recovery. In order to ensure common mode has been established in Recovery.RcvrLock, the Downstream Port must maintain a timer, and the Downstream Port must not send TS2 training sequences until a minimum of $T_{COMMONMODE}$ has elapsed since the Downstream Port has started both transmitting and receiving TS1 training sequences. See section 5.5.3.3.

4.2.6.7.2. L1.Idle

- ❑ Transmitter remains in Electrical Idle.
  - ❑ The DC common mode voltage must be within specification, except as allowed by L1 PM Substates, when applicable.[1]
- ❑ A substate of L1 is entered when the conditions for L1 PM Substates are satisfied (see section 5.5).
  - The L1 PM Substate must be L1.0 when L1.Idle is entered or exited.
- ❑ Next state is Recovery if ~~any Receiver detects~~ exit from Electrical Idle is detected on any Lane of a configured Link, or directed, after remaining in this substate for a minimum of 40 ns in speeds other than 2.5 GT/s.
  - Ports are not required to arm the Electrical Idle exit detectors on all Lanes of the Link.

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[1] The common mode being driven must meet the Absolute Delta Between DC Common Mode During L0 and Electrical Idle ($V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$) specification (see Table 4-18).

Note: the following text can be found in the ECN – 8G_Receiver_Impedance

- Next state is Recovery after a 100 ms timeout if the current data rate is 8.0 GT/s or higher and the Port's Receivers do not meet the ZRX-DC specification for 2.5 GT/s (see Table 4-24). All Ports are permitted, but not encouraged, to implement the timeout and transition to Recovery when the data rate is 8.0 GT/s or higher.
  - This timeout is not affected by the L1 PM Substates mechanism.

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5.2. Link State Power Management

PCI Express defines Link power management states, replacing the bus power management states that were defined by the PCI Bus Power Management Interface Specification. …

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L1 – Higher latency, lower power "standby" state.

L1 support is required for PCI-PM compatible power management. L1 is optional for ASPM unless specifically required by a particular form factor.

When L1 PM Substates is enabled by setting one or more of the enable bits in the L1 PM Substates Control 1 Register this state is referred to as the L1.0 substate.

All main power supplies must remain active during L1. As long as they adhere to the advertised L1 exit latencies, implementations are explicitly permitted to reduce power by applying techniques such as, but not limited to, periodic rather than continuous checking for Electrical Idle exit, checking for Electrical Idle exit on only one Lane, and powering off of unneeded circuits. All platform-provided component reference clocks must remain active during L1, except as permitted by Clock Power Management and/or L1 PM Substates when enabled. A component's internal PLLs may be shut off during L1, enabling greater power savings at a cost of increased exit latency.[2]

The L1 state is entered whenever all Functions of a Downstream component on a given Link are programmed to a D-state other than D0. The L1 state also is entered if the Downstream component requests L1 entry (ASPM) and receives positive acknowledgement for the request.

Exit from L1 is initiated by an Upstream-initiated transaction targeting a Downstream component, or by the Downstream component's initiation of a transaction heading Upstream. Transition from L1 to L0 is typically a few microseconds.

TLP and DLLP transmission is disabled for a Link in L1.

L1 PM Substates –- optional L1.1 and L1.2 substates of the L1 low power Link state for PCI-PM and ASPM.

In the L1.1 substate, the Link common mode voltages are maintained. The L1.1 substate is entered when the Link is in the L1.0 substate and conditions for entry into L1.1 substate are met. See Section 5.5.1. for details.

[2] For example, disabling the internal PLL may be something that is desirable when in $D3_{hot}$, but not so when in D1 or D2.

In the L1.2 substate, the Link common mode voltages are not required to be maintained. The L1.2 substate is entered when the Link is in the L1.0 substate and conditions for entry into L1.2 substate are met. See Section 5.5.1. for details.

Exit from all L1 PM Substates is initiated when the CLKREQ# signal is asserted (see Sections 5.5.2.1 and 5.5.3.3).

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5.3.2.1. Entry into the L1 State

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Components on either end of a Link in L1 may optionally disable their internal PLLs in order to conserve more energy. Note, however, that platform supplied main power and reference clocks must continue to be supplied to components on both ends of a Link in the L1.0 substate of L1.

Refer to Sections 5.5.1 for entry into the L1 PM Substates.

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5.3.2.2. Exit from L1 State

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2. The Upstream component detects that a configuration cycle is intended for a Link that is currently in a low power state, and as a result, initiates a transition of that Link into the L0 state.
3. If the Link is in either L1.1 or L1.2 substates of L1, then the Upstream component initiates a transition of the Link into the L1.0 substate of L1.

Note to editor: update bullet numbering accordingly

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5.4.1. Active State Power Management (ASPM)

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The L1 Link state is optimized for maximum power savings at a cost of longer entry and exit latencies. L1 reduces Link power beyond the L0s state for cases where very low power is required and longer transition times are acceptable. ASPM support for the L1 Link state is optional unless specifically required by a particular form factor.

Optional L1 PM Substates L1.1 and L1.2 are defined. These substates can further reduce Link power for cases where very low idle power is required, and longer transition times are acceptable.

5.4.1.2.1. Entry into the L1 State

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See Section 5.5.1. for details on transitions into either the L1.1 or L1.2 substates.

5.4.1.2.2. Exit from the L1 State

Components on either end of a Link may initiate an exit from the L1 Link state.

See Section 5.5.1. for details on transitions to this state from either the L1.1 or L1.2 substates.

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5.5. L1 PM Substates

L1 PM Substates establish a Link power management regime that creates lower power substates of the L1 Link state (see **Figure 5-x1**), and associated mechanisms for using those substates. The L1 PM Substates are:

- L1.0 substate
  - The L1.0 substate corresponds to the conventional L1 Link state. This substate is entered whenever the Link enters L1. The L1 PM Substate mechanism defines transitions from this substate to and from the L1.1 and L1.2 substates.
  - The Upstream and Downstream Ports must be enabled to detect Electrical Idle exit as required in Section 4.2.6.7.2.
- L1.1 substate
  - Link common mode voltages are maintained.
  - Uses a bidirectional open-drain clock request (CLKREQ#) signal for entry to and exit from this state.
  - The Upstream and Downstream Ports are not required to be enabled to detect Electrical Idle.
- L1.2 substate
  - Link common mode voltages are not required to be maintained.
  - Uses a bidirectional open-drain clock request (CLKREQ#) signal for entry to and exit from this state.
  - The Upstream and Downstream Ports are not required to be enabled to detect electrical idle (EI).

Ports that support L1 PM Substates must not require a reference clock while in L1 PM Substates other than L1.0.

Ports that support the L1.2 substate for ASPM L1 must support Latency Tolerance Reporting (LTR).

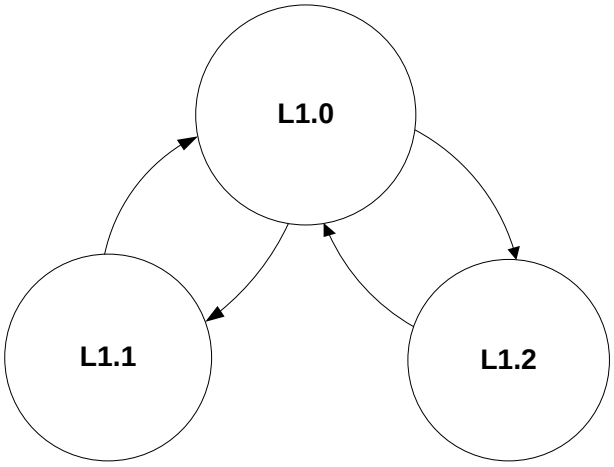

Figure 5-x1: State Diagram for L1 PM Substates

When enabled, the L1 PM Substates mechanism applies the following additional requirements to the CLKREQ# signal:

- The CLKREQ# signal must be supported as a bi-directional open drain signal by both the Upstream and Downstream Ports of the Link. Each Port must have a unique instance of the signal, and the Upstream and Downstream Port CLKREQ# signals must be connected.
- It is permitted for the Upstream Port to de-assert CLKREQ# when the Link is in the PCI-PM L1 or ASPM L1 states, or when the Link is in the L2/L3 Ready pseudo-state; CLKREQ# must be asserted by the Upstream Port when the Link is in any other state.
- All other specifications related to the CLKREQ# signal that are not specifically defined or modified by L1 PM Substates continue to apply.

If these requirements cannot be satisfied in a particular system, then L1 PM Substates must not be enabled.

IMPLEMENTATION NOTE

CLKREQ# Connection Topologies

For an Upstream component the connection topologies for the CLKREQ# signal can vary. A few examples of CLKREQ# connection topologies are described below. For the Downstream component these cases are essentially the same, however from the Upstream component's perspective, there are some key differences that are described below.

Example 1: Single Downstream Port with a single PLL connected to a single Upstream Port (see Figure 5-x2).

In this platform configuration the Upstream component (A) has only a single CLKREQ# signal. The Upstream and Downstream Ports' CLKREQ# (A and B) signals are connected to each other. In this case, Upstream component (A), must assert CLKREQ# signal whenever it requires a reference clock.

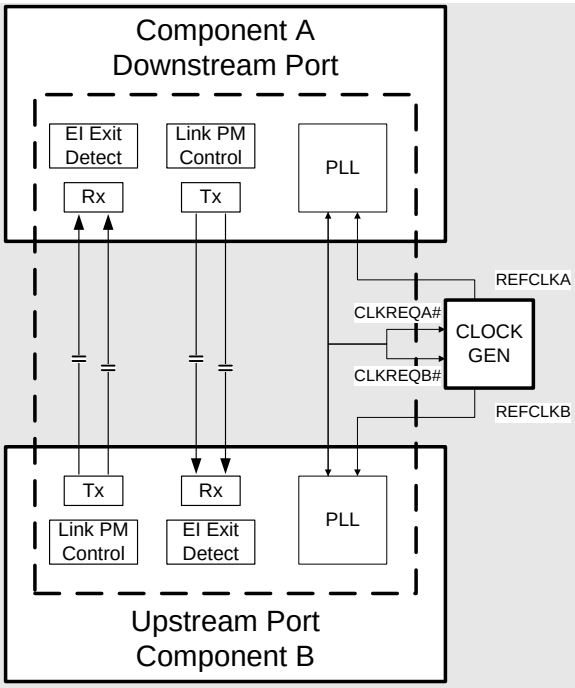

Figure 5-x2: Downstream Port with a Single PLL

Example 2: Upstream component with multiple Downstream Ports, with a common shared PLL, connected to separate Downstream components (see Figure 5-x3).

In this example configuration, there are three instances of CLKREQ# signal for the Upstream component (A), one per Downstream Port and a common shared CLKREQ# signal for the Upstream component (A). In this topology the Downstream Port CLKREQ# (CLKREQB#, CLKREQC#) signals are used to connect to the CLKREQ# signal of the Upstream Port of the Downstream components (B and C). The common shared CLKREQ# (CLKREQA#) signal for the Upstream component is used to request the reference clock for the shared PLL. The PLL control logic in Upstream component (A) can only be turned off and CLKREQA# be de-asserted when both the Downstream Ports are in L1.1 or L1.2 Substates, and all internal (A) consumers of the PLL don't require a clock.

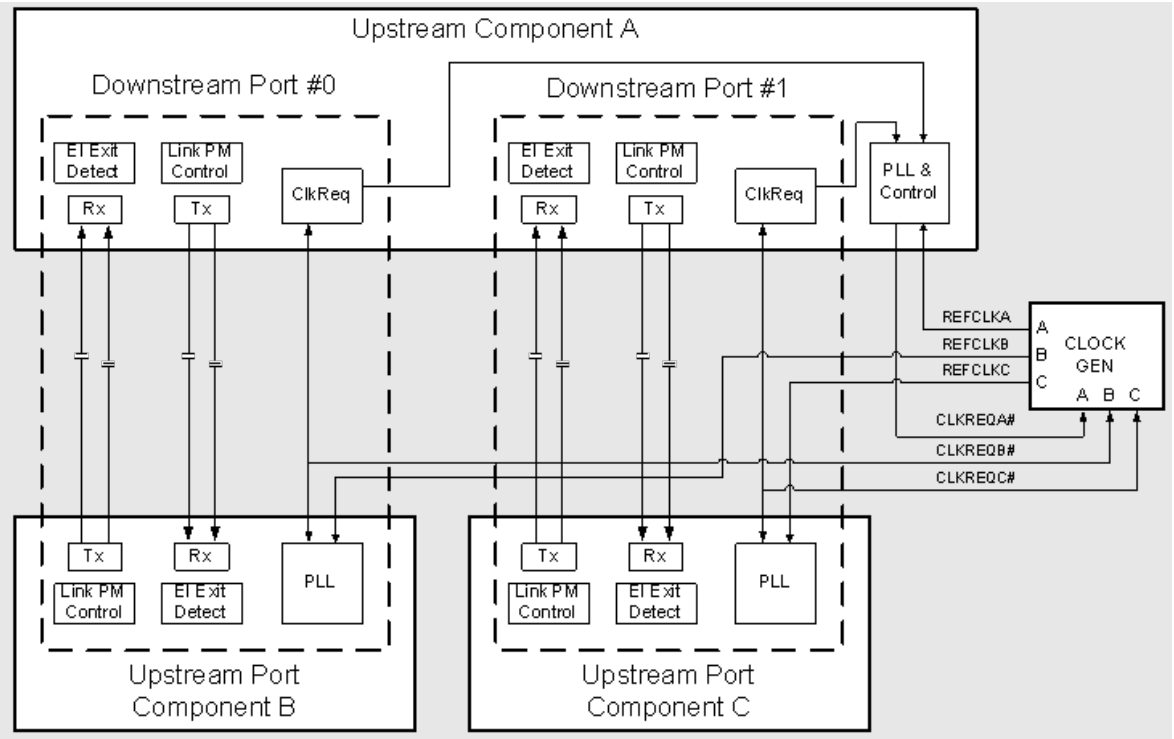

Figure 5-x3: Multiple Downstream Ports with a shared PLL

It is necessary for board implementers to consider what CLKREQ# topologies will be supported by components in order to make appropriate board level connections to support L1 PM Substates and for the reference clock generation.

IMPLEMENTATION NOTE

Avoiding Unintended Interactions Between L1 PM Substates and the LTSSM

It is often the case that implementation techniques which save power will also increase the latency to return to normal operation. When implementing L1 PM Substates, it is important for the implementer to ensure that any added delays will not negatively interact with other elements of the platform. It is particularly important to ensure that LTSSM timeout conditions are not unintentionally triggered. Although typical implementations will not approach the latencies that would cause such interactions, the responsibility lies with the implementor to ensure that correct overall operation is achieved.

5.5.1 Entry conditions for L1 PM Substates and L1.0 Requirements

The Link is considered to be in PCI-PM L1.0 when the L1 PM Substate is L1.0 and the LTSSM entered L1 through PCI-PM compatible power management. The Link is considered to be in ASPM L1.0 when the L1 PM Substate is in L1.0 and LTSSM entered L1 through ASPM.

The following rules define how the L1.1 and L1.2 substates are entered:

- Both the Upstream and Downstream Ports must monitor the logical state of the CLKREQ# signal.
- When in PCI-PM L1.0 and the PCI-PM L1.2 Enable bit is Set, the L1.2 substate must be entered when CLKREQ# is de-asserted.
- When in PCI-PM L1.0 and the PCI-PM L1.1 Enable bit is Set, the L1.1 substate must be entered when CLKREQ# is de-asserted and the PCI-PM L1.2 Enable bit is Clear.
- When in ASPM L1.0 and the ASPM L1.2 Enable bit is Set, the L1.2 substate must be entered when CLKREQ# is de-asserted and all of the following conditions are true:
  - the reported snooped LTR value is greater than or equal to the value set by the LTR_L1.2_THRESHOLD Value and Scale fields, or there is no snoop service latency requirement
  - the reported non-snooped LTR value is greater than or equal to the value set by the LTR_L1.2_THRESHOLD Value and Scale fields, or there is no non-snoop service latency requirement
- When in ASPM L1.0 and the ASPM L1.1 Enable bit is Set, the L1.1 substate must be entered when CLKREQ# is de-asserted and the conditions for entering the L1.2 substate are not satisfied.

When the entry conditions for L1.2 are satisfied, the following rules apply:

- Both the Upstream and Downstream Ports must monitor the logical state of the CLKREQ# input signal.
- An Upstream Port must not de-assert CLKREQ# until the Link has entered L1.0.
- It is permitted for either Port to assert CLKREQ# to prevent the Link from entering L1.2.
- A Downstream Port intending to block entry into L1.2 must assert CLKREQ# before the Link enters L1.
- When CLKREQ# is de-asserted the Ports enter the L1.2.Entry substate of L1.2.

If a Downstream Port is in PCI-PM L1.0 and PCI-PM L1.1 Enable and/or PCI-PM L1.2 Enable are Set, or if a Downstream Port is in ASPM L1.0 and ASPM L1.1 Enable and/or ASPM L1.2 Enable are Set, and the Downstream Port initiates an exit to Recovery without having entered L1.1 or L1.2, the Downstream Port must assert CLKREQ# until the Link exits Recovery.

5.5.2. L1.1 Requirements

Both Upstream and Downstream Ports are permitted to deactivate mechanisms for electrical idle (EI) exit detection and Refclk activity detection if implemented, however both ports must maintain common mode.

5.5.2.1. Exit from L1.1

If either the Upstream or Downstream Port needs to initiate exit from L1.1, it must assert CLKREQ# until the Link exits Recovery. The Upstream Port must assert CLKREQ# on entry to Recovery, and must continue to assert CLKREQ# until the next entry into L1, or other state allowing CLKREQ# de-assertion.

- Next state is L1.0 if CLKREQ# is asserted.
  - The Refclk will eventually be turned on as defined in the PCI Express Mini CEM spec, which may be delayed according to the LTR advertized by the Upstream Port.

Figure 5-x4 illustrates entry into L1.1 with exit driven by the Upstream Port.

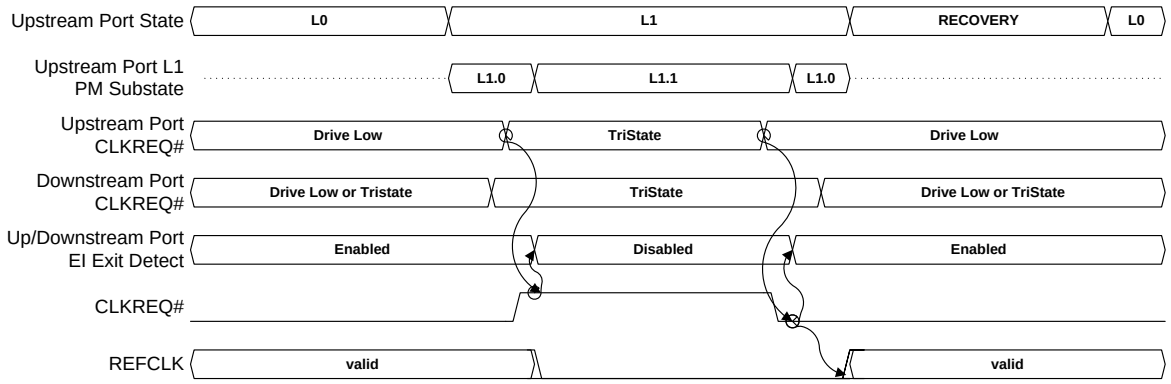

Figure 5-x4: Example: L1.1 Waveforms Illustrating Upstream Port Initiated Exit

Figure 5-x5 illustrates entry into L1.1 with exit driven by the Downstream Port.

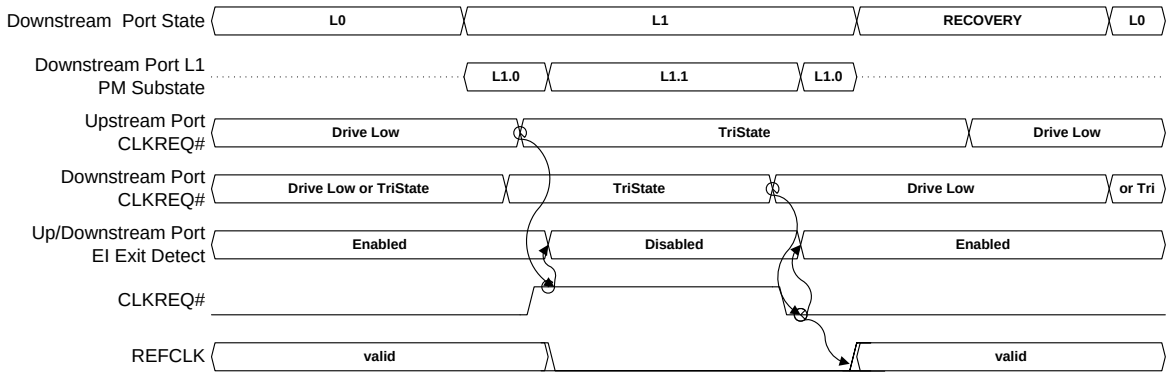

Figure 5-x5: Example: L1.1 Waveforms Illustrating Downstream Port Initiated Exit

5.5.3. L1.2 Requirements

All Link and PHY state must be maintained during L1.2, or must be restored upon exit using implementation-specific means, and the LTSSM and corresponding Port state upon exit from L1.2 must be indistinguishable from the L1.0 LTSSM and Port state.

L1.2 has additional requirements that do not apply to L1.1. These requirements are documented in this section.

L1.2 has three substates, which are defined below (see Figure 5-x6).

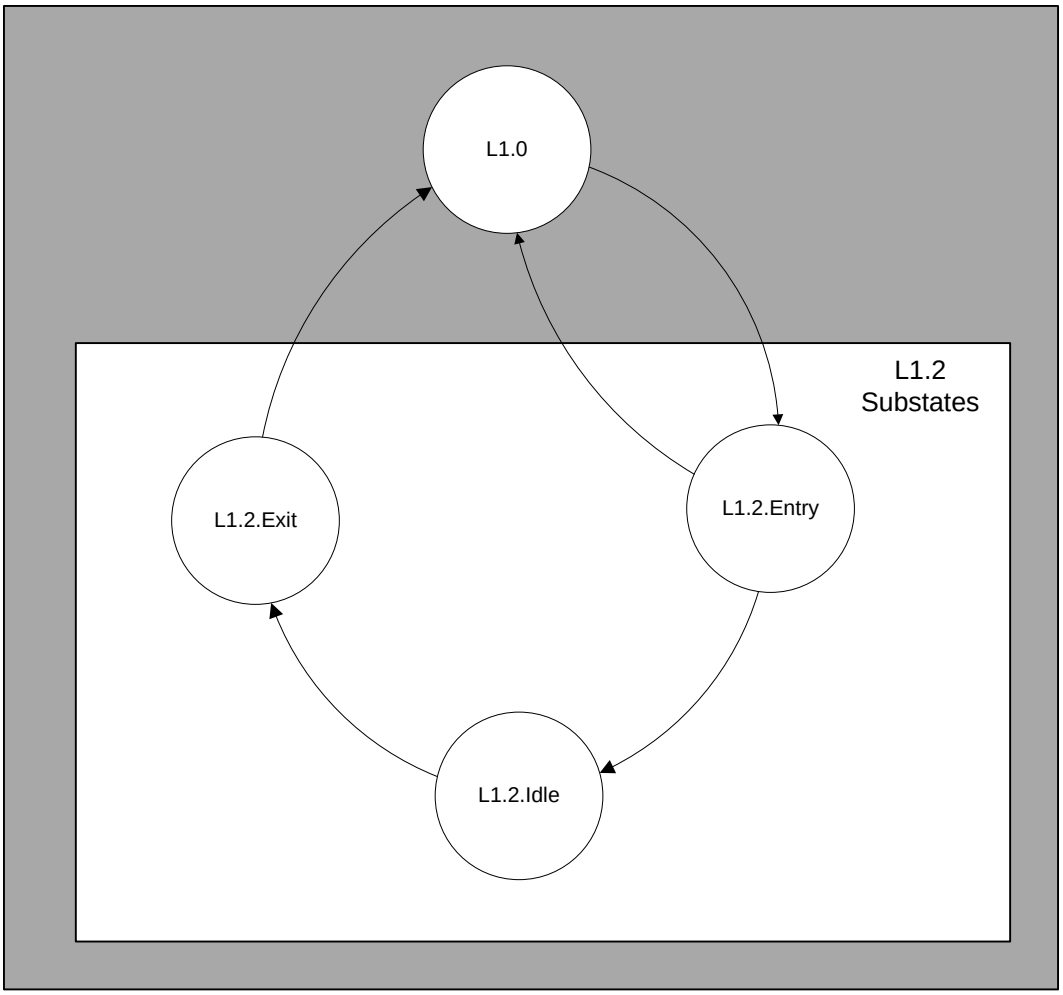

Figure 5-x6: L1.2 Substates

5.5.3.1. L1.2.Entry

L1.2.Entry is a transitional state on entry into L1.2 to allow time for Refclk to turn off and to ensure both Ports have observed CLKREQ# de-asserted. The following rules apply to L1.2.Entry:

- Both Upstream and Downstream Ports continue to maintain common mode.
- Both Upstream and Downstream Ports may turn off their electrical idle (EI) exit detect circuitry.
- The Upstream and Downstream Ports must not assert CLKREQ# in this state.
- Refclk must be turned off within $T_{L1O\_REFCLK\_OFF}$.
- Next state is L1.0 if CLKREQ# is asserted, else the next state is L1.2.Idle after waiting for T_{POWER_OFF}.

Note that there is a boundary condition which can occur when one Port asserts CLKREQ# shortly after the other Port de-asserts CLKREQ#, but before the first Port has observed

CLKREQ# de-asserted. This is an unavoidable boundary condition that implementations must handle correctly. An example of this condition is illustrated in Figure 5-x7.

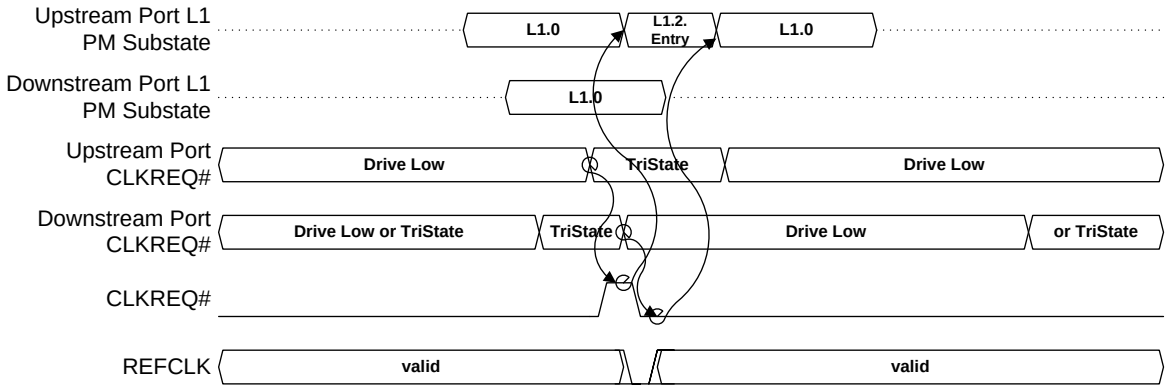

Figure 5-x7: Example: Illustration of Boundary Condition due to Different Sampling of CLKREQ#

5.5.3.2. L1.2.Idle

When requirements for the entry into L1.2.Idle state (see Section 5.5.1) have been satisfied then the Ports enter the L1.2.Idle substate. The following rules apply in L1.2.Idle:

- ❑ Both Upstream and Downstream Ports may power-down any active logic, including circuits required to maintain common mode.
- ❑ The PHY of both Upstream and Downstream Ports may have their power removed.

The following rules apply for L1.2.Idle state when using the CLKREQ#-based mechanism:

- ❑ If either the Upstream or Downstream Port needs to exit L1.2, it must assert CLKREQ# after ensuring that $T_{L1.2}$ has been met.
- ❑ If the Downstream Port is initiating exit from L1, it must assert CLKREQ# until the Link exits Recovery. The Upstream Port must assert CLKREQ# on entry to Recovery, and must continue to assert CLKREQ# until the next entry into L1, or other state allowing CLKREQ# de-assertion.
- ❑ If the Upstream Port is initiating exit from L1, it must continue to assert CLKREQ# until the next entry into L1, or other state allowing CLKREQ# de-assertion.
- ❑ Both the Upstream and Downstream Ports must monitor the logical state of the CLKREQ# input signal.
- ❑ Next state is L1.2.Exit if CLKREQ# is asserted.

5.5.3.3. L1.2.Exit

This is a transitional state on exit from L1.2 to allow time for both devices to power up. In L1.2.Exit, the following rules apply:

- The PHYs of both Upstream and Downstream Ports must be powered.
- It must not be assumed that common mode has been maintained.

5.5.3.3.1. Exit from L1.2

The following rules apply for L1.2 Exit using the CLKREQ#-based mechanism:

- Both Upstream and Downstream Ports must power up any circuits required for L1.0, including circuits required to maintain common mode.
- The Upstream and Downstream Ports must not change their driving state of CLKREQ# in this state.
- Refclk must be turned on no earlier than $T_{L1O\_REFCLK\_ON}$ minimum time, and may take up to the amount of time allowed according to the LTR advertized by the Endpoint before becoming valid.
- Next state is L1.0 after waiting for T_{POWER_ON}:
    - Common mode is permitted to be established passively during L1.0, and actively during Recovery. In order to ensure common mode has been established, the Downstream Port must maintain a timer, and the Downstream Port must not send TS2 training sequences until a minimum of $T_{COMMONMODE}$ has elapsed since the Downstream Port has started both transmitting and receiving TS1 training sequences.

Figure 5-x8 illustrates the signal relationships and timing constraints associated with L1.2 entry and Upstream Port initiated exit.

Figure 5-x9 illustrates the signal relationships and timing constraints associated with L1.2 entry and Downstream Port initiated exit.

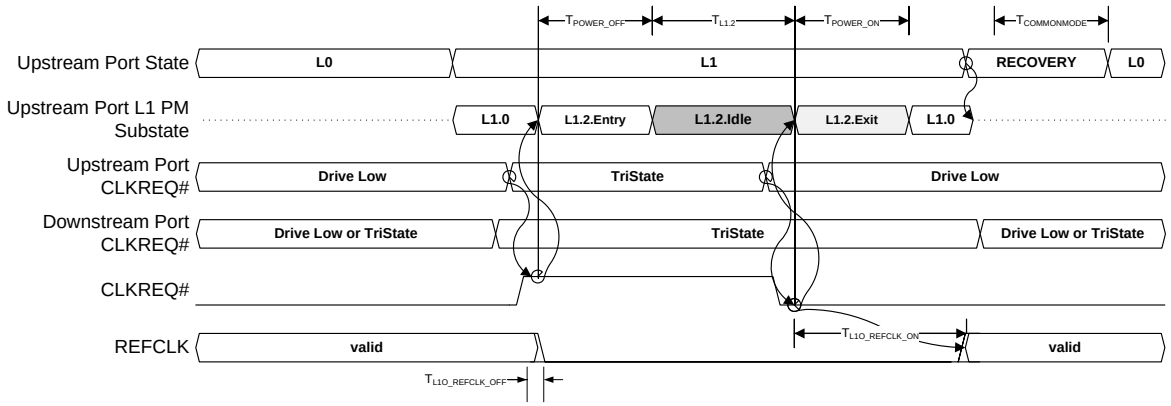

Figure 5-x8: Example: L1.2 Waveforms Illustrating Upstream Port Initiated Exit

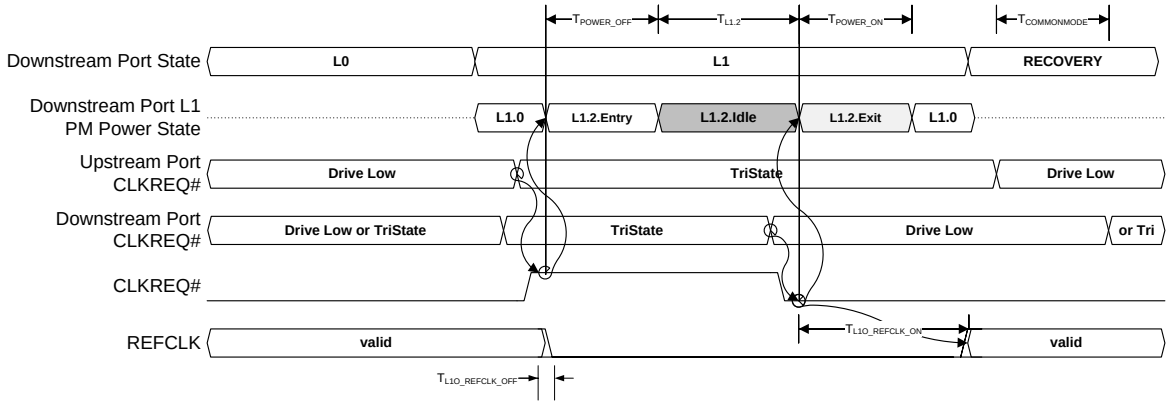

Figure 5-x9: Example: L1.2 Waveforms Illustrating Downstream Port Initiated Exit

5.5.4. L1 PM Substates Configuration

L1 PM Substates is considered enabled on a Port when any combination of the ASPM L1.1 Enable, ASPM L1.2 Enable, PCI-PM L1.1 Enable and PCI-PM L1.2 Enable bits associated with that Port are Set.

An L1 PM Substate enable bit must only be Set in the Upstream and Downstream Ports on a Link when the corresponding supported capability bit is Set by both the Upstream and Downstream Ports on that Link, otherwise the behavior is undefined.

The Setting of any enable bit must be performed at the Downstream Port before the corresponding bit is permitted to be Set at the Upstream Port. If any L1 PM Substates enable bit is at a later time to be cleared, the enable bit(s) must be cleared in the Upstream Port before the corresponding enable bit(s) are permitted to be cleared in the Downstream Port.

If setting either or both of the enable bits for ASPM L1 PM Substates, both ports must be configured as described in this section while ASPM L1 is disabled.

If setting either or both of the enable bits for PCI-PM L1 PM Substates, both ports must be configured as described in this section while in D0.

Prior to setting either or both of the enable bits for L1.2, the values for T_{POWER_ON}, Common_Mode_Restore_Time, and, if the ASPM L1.2 Enable bit is to be Set, the LTR_L1.2_THRESHOLD (both Value and Scale fields) must be programmed.

The T_{POWER_ON} and Common_Mode_Restore_Time fields must be programmed to the appropriate values based on the components and AC coupling capacitors used in the connection linking the two components. The determination of these values is design implementation specific.

When both the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are cleared, it is not required to program the T_{POWER_ON}, Common_Mode_Restore_Time, and LTR_L1.2_THRESHOLD Value and Scale fields, and hardware must not rely on these fields to have any particular values.

When programming LTR_L1.2_THRESHOLD Value and Scale fields, identical values must be programmed in both Ports.

5.5.5. L1 PM Substates Timing Parameters

The following table defines the timing parameters associated with the L1.2 substates mechanism.

Table 5-xx: Timing Parameters

Parameter	Description	Min	Max	Units
T_{POWER_OFF}	CLKREQ# de-assertion to entry into the L1.2.Idle substate		2	µs
$T_{COMMONMODE}$	Restoration of Refclk to restoration of common mode established through active transmission of TS1 training sequences (see Section 5.5.3.3.1)	Programmable in range from 0 to 255		µs
$T_{L1O\_REFCLK\_OFF}$	CLKREQ# de-assertion to Refclk reaching idle electrical state when entering L1.2	0	100	ns
$T_{L1O\_REFCLK\_ON}$	CLKREQ# assertion to Refclk valid when exiting L1.2	T_{POWER_ON}	LTR value advertized by the Endpoint	µs
T_{POWER_ON}	The minimum amount of time that each component must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface to ensure no device is ever actively driving into an unpowered component.	Set in the L1 PM Substates Control 2 Register (range from 0 to 3100)		µs
$T_{L1.2}$	Time a Port must stay in L1.2 when CLKREQ# must remain inactive	4		µs

7.8.6 Link Capabilities Register (Offset 0Ch)

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18	**Clock Power Management** – For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a multi-Function device associated with an Upstream Port, each Function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all Functions of the multi-Function device indicate a 1b in this bit. For ARI Devices, all Functions must indicate the same value in this bit. For Downstream Ports, this bit must be hardwired to 0b.	RO

…

7.8.7 Link Control Register (Offset 0Ch)

…

8	**Enable Clock Power Management** – Applicable only for Upstream Ports and with form factors that support a "Clock Request" (CLKREQ#) mechanism, this bit operates as follows: 0b Clock power management is disabled and device must hold CLKREQ# signal low. 1b When this bit is Set, the device is permitted to use CLKREQ# signal to power manage Link clock according to protocol defined in appropriate form factor specification. For a non-ARI multi-Function device, power-management-configuration software must only Set this bit if all Functions of the multi-Function device indicate a 1b in the Clock Power Management bit of the Link Capabilities register. The component is permitted to use the CLKREQ# signal to power manage Link clock only if this bit is Set for all Functions. For ARI Devices, Clock Power Management is enabled solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. The CLKREQ# signal may also be controlled via the L1 PM Substates mechanism. Such control is not affected by the setting of this bit. Downstream Ports and components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities register) must hardwire this bit to 0b. Default value of this bit is 0b, unless specified otherwise by the form factor specification.	RW

…

7.xx. L1 PM Substates Extended Capability

The PCI Express L1 PM Substates Capability is an optional Extended Capability, that is required if L1 PM Substates is implemented at a Port. The L1 PM Substates Extended Capability structure is defined as shown in Figure 7-xx.

For a multi-Function device associated with an Upstream Port implementing L1 PM Substates, this Extended Capability Structure must be implemented only in Function 0, and must control the Upstream Port's Link behavior on behalf of all the Functions of the device.

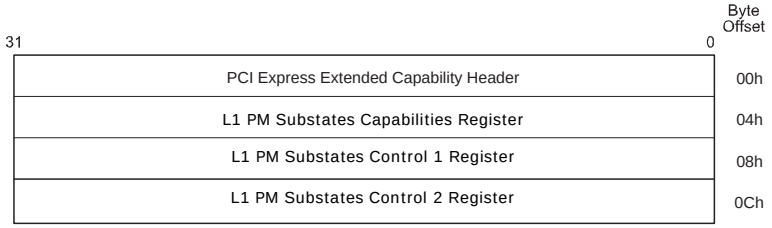

Figure 7-xx: L1 PM Substates Capability

7.xx.1. L1 PM Substates Extended Capability Header (Offset 00h)

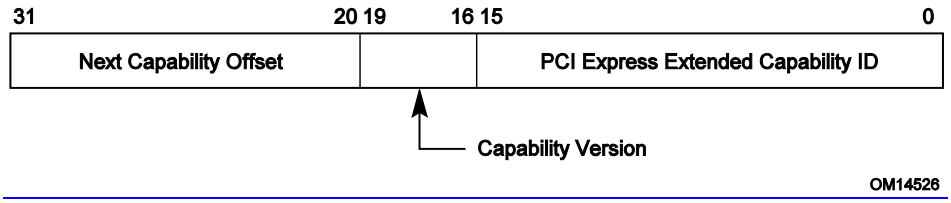

Figure 7-xx: L1 PM Substates Extended Capability Header

Table 7-xx: L1 PM Substates Extended Capability Header

Bit Location	Register Description	Attributes
15:0	**PCI Express Extended Capability ID** – This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 PM Substates is 001Eh.	RO
19:16	**Capability Version** – This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	**Next Capability Offset** – This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.	RO

7.xx.2. L1 PM Substates Capabilities Register (Offset 04h)

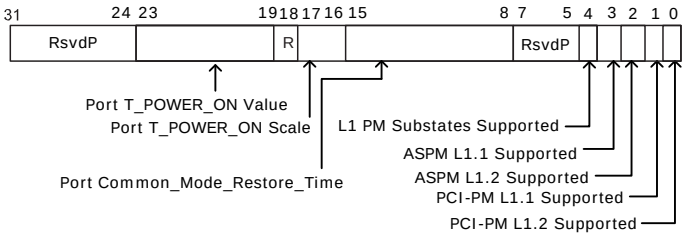

Figure 7-xx: L1 PM Substates Capabilities Register

Table 7-xx: L1 PM Substates Capabilities Register

Bit Location	Register Description	Attributes
0	**PCI-PM L1.2 Supported** – When Set this bit indicates that PCI-PM L1.2 is supported.	HwInit
1	**PCI-PM L1.1 Supported -** When Set this bit indicates that PCI-PM L1.1 is supported, and must be Set by all Ports implementing L1 PM Substates.	HwInit
2	**ASPM L1.2 Supported** – When Set this bit indicates that ASPM L1.2 is supported.	HwInit
3	**ASPM L1.1 Supported -** When Set this bit indicates that ASPM L1.1 is supported.	HwInit
4	**L1 PM Substates Supported** – When Set this bit indicates that this Port supports L1 PM Substates.	HwInit
7:5	**Reserved**	RsvdP
15:8	**Port Common_Mode_Restore_Time –** Time (in µs) required for this Port to re-establish common mode as described in table <reference 5-xx Timing Parameters>. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP.	HwInit/RsvdP (See description)
17:16	**Port T_POWER_ON_Scale –** Specifies the scale used for the Port T_POWER_ON Value field in the L1 PM Substates Capabilities register. Range of Values 00b = 2µs 01b = 10µs 10b = 100µs 11b = Reserved Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Default value is 00b	HwInit / RsvdP
18	**Reserved**	RsvdP

23:19	**Port T_POWER_ON Value –** Along with the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register sets the time (in us) that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register. Default value is 00101b Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP.	HwInit / RsvdP
31:24	**Reserved**	RsvdP

7.xx.3. L1 PM Substates Control 1 Register (Offset 08h)

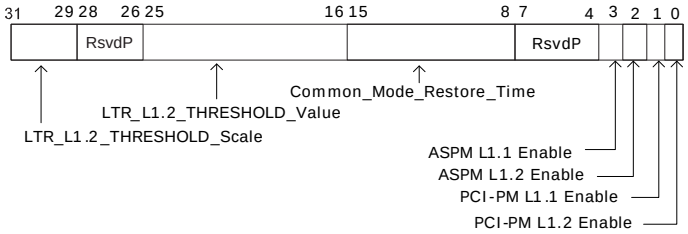

Figure 7-xx: L1 PM Substates Control 1 Register

Table 7-xx: L1 PM Substates Control 1 Register

Bit Location	Register Description	Attributes
0	**PCI-PM L1.2 Enable** – When Set this bit enables PCI-PM L1.2. Required for both Upstream and Downstream Ports. For Ports for which the PCI-PM L1.2 Supported bit is Clear this bit is permitted to be hardwired to 0. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported bit in the L1 PM Substates Capabilities Register is Set. Default value is 0b.	RW
1	**PCI-PM L1.1 Enable -** When Set this bit enables PCI-PM L1.1. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported bit in the L1 PM Substates Capabilities Register is Set. Default value is 0b.	RW
2	**ASPM L1.2 Enable** – When Set this bit enables ASPM L1.2. Required for both Upstream and Downstream Ports. For Ports for which the ASPM L1.2 Supported bit is Clear this bit is permitted to be hardwired to 0. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported bit in the L1 PM Substates Capabilities Register is Set. Default value is 0b.	RW
3	**ASPM L1.1 Enable -** When Set this bit enables ASPM L1.1. Required for both Upstream and Downstream Ports. For Ports for which the ASPM L1.1 Supported bit is Clear this bit is permitted to be hardwired to 0. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported bit in the L1 PM Substates Capabilities Register is Set. Default value is 0b.	RW
7:4	**Reserved**	RsvdP

15:8	**Common_Mode_Restore_Time –** Sets value of $T_{COMMONMODE}$ (in µs), which must be used by the Downstream Port for timing the re-establishment of common mode, as described in Table 5-xx. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are Set. Required for Downstream Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. This field is of type RsvdP for Upstream Ports. Default value is implementation specific.	RW/RsvdP (See Description)
25:16	**LTR_L1.2_THRESHOLD_Value** – Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 (if enabled) or L1.2 (if enabled). The default value for this field is 00 0000 0000b. This field must only be modified when the ASPM L1.2 Enable bit is Clear. The Port behavior is undefined if this field is modified when the ASPM L1.2 Enable bit is Set. Required for all Ports for which the ASPM L1.2 Supported bit is Set, otherwise this field is of type RsvdP.	RW/RsvdP (See Description)
28:26	**Reserved**	RsvdP
31:29	**LTR_L1.2_THRESHOLD_Scale** – This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. Encoding is the same as the LatencyScale fields in the LTR Message (see Section 6.18). The default value for this field is 000b. Hardware operation is undefined if software writes a Not-Permitted value to this field. This field must only be modified when the ASPM L1.2 Enable bit is Clear. The Port behavior is undefined if this field is modified when the ASPM L1.2 Enable bit is Set. Required for all Ports Ports for which the ASPM L1.2 Supported bit is Set, otherwise this field is of type RsvdP.	RW/RsvdP (See description)

7.xx.4. L1 PM Substates Control 2 Register (Offset 0Ch)

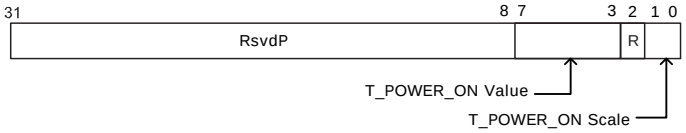

Figure 7-xx: L1 PM Substates Control 2 Register

Table 7-xx: L1 PM Substates Control 2 Register

Bit Location	Register Description	Attributes
1:0	**T_POWER_ON_Scale –** Specifies the scale used for T_POWER_ON Value. Range of Values 00b = 2µs 01b = 10µs 10b = 100µs 11b = Reserved Required for all Ports that support L1.2, otherwise this field is of type RsvdP. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are Set. Default value is 00b	RW/ RsvdP
2	**Reserved**	RsvdP
7:3	**T_POWER_ON_Value –** Along with the T_POWER_ON Scale sets the minimum amount of time (in µs) that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON Scale field. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are Set. Default value is 00101b Required for all Ports that support L1.2, otherwise this field is of type RsvdP.	RW/ RsvdP
31:8	**Reserved**	RsvdP

The following section applies to updates to the PCIe Mini-CEM Specification.

PCIe Mini CEM Specification – revise the affected portion of Table 3-1 as follows:

Table 3-1: PCI Express Mini Card System Interface Signals

Signal Group	Signal	Direction	Description
Auxiliary Signals (3.3V Compliant)	PERST#	Input	Functional reset to the card
	CLKREQ#	Input/Output	Reference clock request signal; Also used by L1 PM Substates.
	WAKE#	Input/Output	Open Drain active Low signal. When the add-in card supports wakeup, this signal is used to request that the system return from a sleep/suspended state to service a function initiated wake event. When the add-in card supports the OBFF mechanism, this signal is used by the system to indicate OBFF or CPU Active state transitions.
	SMB_DATA	Input/Output	SMBus data signal compliant to the SMBus 2.0 specification
	SMB_CLK	Input	SMBus clock signal compliant to the SMBus 2.0 specification

PCIe Mini CEM Specification – revise Section 3.2.5.2. as follows:

3.2.5.2. CLKREQ# Signal

The CLKREQ# signal is an open drain, active low signal that is driven low by the add-in card~~PCI Express Mini Card function~~ to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data. Operation of the CLKREQ# signal is determined by the state of the Enable Clock Power Management bit in the Link Control Register (offset 010h). When disabled, the CLKREQ# signal shall be asserted at all times whenever power is applied to the card, with the exception that it may be de-asserted during L1 PM Substates. When enabled, the CLKREQ# signal may be de-asserted during an L1 Link state.

The CLKREQ# signal is also used by the L1 PM Substates mechanism. In this case, CLKREQ# can be asserted by either the system or add-in card to initiate an L1 exit. See the *PCI Express Base Specification* for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.

Whenever dynamic clock management is enabled and when a card stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and module designs shall be tolerant of an active reference clock even when CLKREQ# is de-asserted by the module.

…

In PCI Express Mini Card Electromechanical Specification Revision 1.2, change Section 3.4.1. as follows:

3.4.1. Logic Signal Requirements

The 3.3V card logic levels for single-ended digital signals (WAKE#, CLKREQ#, PERST#, W_DISABLE1#, W_DISABLE2#, and MLDIR) are given in Table 3-9.

Table 3-9: DC Specification for 3.3V Logic Signaling

Symbol	Parameter	Conditions	Min	Max	Units	Notes
+3.3Vaux	Supply Voltage		3.3 – 9%	3.3 + 9%	V	3
V_{IH}	Input High Voltage		2.0	3.6	V	1
V_{IL}	Input Low Voltage		-0.5	0.8	V	1
I_{OL}	Output Low Current for open-drain signals	0.4 V	4		mA	2
I_{IN}	Input Leakage Current	0 V to 3.3 V	-10	+10	µA	1
I_{LKG}	Output Leakage Current	0 V to 3.3 V	-50	+50	µA	1
C_{IN}	Input Pin Capacitance			7	pF	1
C_{OUT}	Output Pin Capacitance			30	pF	2
$R_{PULL-UP}$	Pull-up Resistance		9	60	kΩ	4

Notes:
1. Applies to PERST#, W_DISABLE1#, W_DISABLE2#, MLDIR (when applicable), WAKE# (when used for OBFF signaling), and CLKREQ# (when used for L1 exit signaling).
2. Applies to CLKREQ# and WAKE#.
3. As measured at the card connector pad.
4. Applies to CLKREQ# pull-up on host system

The following section applies to the PCI Express Card Electromechanical Specification Revision 2.0 --

1.5 Electrical Overview

…

- ❑ PERST#, required
- ❑ CLKREQ#, optional

…

REFCLK, CLKREQ#, JTAG, SMBus,

2. Auxiliary Signals

The auxiliary signals are provided on the connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture.

…

PRSNT2# (required): add-in card presence detect pin. See Chapter 3 for a detailed description.

CLKREQ# (optional): The CLKREQ# signal is an open drain, active low signal that is driven low by the card to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data. See the PCI Express Mini-CEM Specification for details on the functional and electrical requirements for the CLKREQ# signal. The CLKREQ# signal is also used by the optional L1 PM Substates mechanism. In this case, CLKREQ# can be asserted by either the system or add-in card to initiate an L1 exit. See the *PCI Express Base Specification* for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.

2.6.1. DC Specifications

Table 2-3: Auxiliary Signal DC Specifications - PERST#, WAKE#, CLKREQ# and SMBus

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage		-0.5	0.8	V	2
V_{IH1}	Input High Voltage		2.0	V_{cc3_3} + 0.5	V	2
V_{IL2}	Input Low Voltage		-0.5	0.8	V	4
V_{IH2}	Input High Voltage		2.1	V_{ccSus3_3} + 0.5	V	4

V_{OL1}	Output Low Voltage	4.0 mA		0.2	V	1, 3
V_{HMAX}	Max High Voltage			V_{cc3_3} + 0.5	V	3
V_{OL2}	Output Low Voltage	4.0 mA		0.4	V	1, 4
I_{in}	Input Leakage Current	0 to 3.3 V	-10	+10	µA	2, 4
I_{lkg}	Output Leakage Current	0 to 3.3 V	-50	+50	µA	3, 5
C_{in}	Input Pin Capacitance			7	pF	2
C_{out}	Output (I/O) Pin Capacitance			30	pF	3,4
$R_{PULL-UP}$	Pull-up Resistance		9	60	kΩ	6

Notes:

1. Open-drain output a pull-up is required on the system board. There is no V_{OH} specification for these signals. The number given is the maximum voltage that can be applied to this pin.
2. Applies to PERST#.
3. Applies to WAKE# and CLKREQ#.
4. Applies to SMBus signals SMBDATA and SMBCLK.
5. Leakage at the pin when the output is not active (high impedance).
6. Applies to CLKREQ# pull-up on host system

5.1. Connector Pinout

Table 5-1 shows the pinout definition for the x1, x4, x8, and x16 PCI Express connectors. The auxiliary pins are identified in the shaded areas.

Pin #	Side B		Side A	
	Name	**Description**	**Name**	**Description**
Mechanical key				
12	CLKREQ#	Clock Request Signal	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK-	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
End of the x1 connector				

...