PCI-SIG ENGINEERING CHANGE NOTICATION

TITLE:	Second Wireless Disable Pin
DATE:	Updated – May 10, 2010, original request May 05, 2010
AFFECTED DOCUMENT:	PCI Express Mini CEM Revision 1.2 and applicable ECNs published as of this notification.
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Part I

1. Summary of the Functional Changes

This ECN is for the functional addition of a second wireless disable signal (W_DISABLE2#) as a new definition of Pin 51 (Reserved). When this optional second wireless disable signal is not implemented by the system, the original intent of a single wireless disable signal disabling all radios on the add-in card when asserted is still required.

2. Benefits as a Result of the Changes

For add-in cards that implement multiple radios, the ability to segment and manage the radios using two independent wireless disable signals is beneficial to meeting requirements for graceful transitions between enabled and disabled states. Specifically, radio state transitions usually involve coordination between hardware and software, and such coordination may require different sequences and timing for each radio implementation – providing multiple wireless disable signals allows for implementing different timings for each radio.

3. Assessment of the Impact

Add-in cards that are expecting to use the second wireless disable signal (W_DISABLE2#) should only be installed in platforms that are designed to support multiple wireless disable signals. If installed in a socket that doesn't support the second signal (i.e. the signal is not connected in the platform), the ability to manage the affected radio may be limited to software only controls.

4. Analysis of the Hardware Implications

As needed to support multiple radios on a single add-in card, platform hardware will have to be changed to connect and terminate multiple wireless disable signals instead of just one.

Analysis of the Software Implications

To the extent that radio device drivers currently interact with the wireless disable signaling, that software may require changes to align with the wireless disable signal associated with that software's radio.

Part II – Detailed Description of the changes

Change Table 3-1 as follows:

Table 3-1: PCI Express Mini Card System Interface Signals

Signal Group	Signal	Direction	Description
Power	+3.3Vaux (5 pins)		3.3 V source
	+1.5V (3 pins)		1.5V source
	GND (14 pins)		Return current path
PCI Express	PETp0, PETn0 PERp0, PERn0	Input/Output	PCI Express x1 data interface: one differential transmit pair and one differential receive pair
	REFCLK+, REFCLK–	Input	PCI Express differential reference clock (100 MHz)
Universal Serial Bus (USB)	USB_D+, USB_D–	Input/Output	USB serial data interface compliant to the USB 2.0 specification
Auxiliary Signals (3.3V Compliant)	PERST#	Input	Functional reset to the card
	CLKREQ#	Output	Reference clock request signal
	WAKE#	Input/Output	Open Drain active Low signal. When the add-in card supports wakeup, this signal is used to request that the system return from a sleep/suspended state to service a function initiated wake event. When the add-in card supports the OBFF mechanism, this signal is used by the system to indicate OBFF or CPU Active state transitions.
	SMB_DATA	Input/Output	SMBus data signal compliant to the SMBus 2.0 specification
	SMB_CLK	Input	SMBus clock signal compliant to the SMBus 2.0 specification
Communications Specific Signals	LED_WPAN#, LED_WLAN#, LED_WWAN#	Output	Open drain, active low signals. These signals are used to allow the PCI Express Mini Card add-in card to provide status indicators via LED devices that will be provided by the system.

Signal Group	Signal	Direction	Description
	W_DISABLE1#, W_DISABLE2#	Input	Active low signals. This These signals is are used by the system to disable radio operation on add-in cards that implement radio frequency applications. When implemented, this these signals requires a pull-up resistor on the card.
User Identity Module (UIM) Signals	UIM_PWR (1 pin)	Output	Power source for the UIM. Compliant to the ISO/IEC 7816-3 specification (VCC).
	UIM_RESET	Output	UIM reset signal. Compliant to the ISO/IEC 7816-3 specification (RST).
	UIM_CLK	Output	UIM clock signal. Compliant to the ISO/IEC 7816-3 specification (CLK).
	UIM_SPU	Input/Output	Standard or proprietary use signal. Compliant to the ISO/IEC 7816-3 specification (SPU).
	UIM_DATA	Input/Output	UIM data signal. Compliant to the ISO/IEC 7816-3 specification (I/O).
	UIM_IC_DP	Input/Output	Inter-Chip USB D+ Data line
	UIM_IC_DM	Input/Output	Inter-Chip USB D- Data line

Change Table 3-6 as follows:

Table 3-6: Simple Indicator Protocol for LED States

State	Definition	Interpretation
OFF	The LED is emitting no light.	Radio is incapable of transmitting. This state is indicated when the card is not powered, ~~the W_DISABLE#~~a wireless disable signal is asserted to disable the radio, or when the radio is disabled by software.
ON	The LED is emitting light.	Radio is capable of transmitting. The LED should remain ON even if the radio is not actually transmitting. For example, the LED remains ON during temporary radio disablements performed by the Mini Card of its own volition to do scanning, switching radios/bands, power-management, etc. If the card is in a state wherein it is possible that radio can begin transmitting without the system user performing any action, this LED should remain ON.

Change Section 3.2.6.2. as follows:

3.2.6.2. ~~W_DISABLE#~~ Wireless Disable Signals

~~The~~ W_DISABLE1# and W_DISABLE2# are wireless disable signals ~~is~~ that are provided ~~to allow~~ for wireless communications add-in cards to allow users to disable, via a system-provided switch, the add-in card's radio operation in order to meet public safety regulations or when otherwise desired. Implementation of this signal is required for systems and all add-in cards that implement radio frequency capabilities. Multiple wireless disable signals are provided to ease managing multiple radios on a single add-in card. If only one wireless disable signal is implemented by the system, asserting that single signal should be used for collectively disabling all radios on the add-in card.

The ~~W_DISABLE#~~wireless disable signals ~~is~~ are ~~an~~ active low signals that when asserted (driven low) by the system shall disable radio operation. When implemented, ~~A~~ a pull-up resistor between ~~W_DISABLE#~~each wireless disable signal and +3.3Vaux is required on the card and should be in the range of 100 kΩ to 200 kΩ. The assertion and de-assertion of ~~the W_DISABLE#~~each wireless disable signal is asynchronous to any system clock. All transients resulting from mechanical switches need to be de-bounced by system circuitry.

When ~~the W_DISABLE#~~a wireless disable signal is asserted, all of the radios associated with that signal shall be disabled. When ~~the~~ a ~~W_DISABLE#~~wireless disable signal is not asserted, the associated radios may transmit if not disabled by other means such as software. ~~This~~ These signals may be shared between multiple Mini Cards.

In normal operation, the card should disassociate with the wireless network and cease any further operations (transmit/receive) as soon as possible after the ~~W_DISABLE#~~wireless disable signal is asserted. Given that a graceful disassociation with the wireless network fails to complete in a timely manner, the Mini Card shall discontinue any communications with the network and assure that its radio operation has ceased no later than 30 seconds following the initial assertion of the ~~W_DISABLE#~~wireless disable signal. Once the disabling process is complete, the LED specific to the radio shall indicate the disabled condition to the user.

The card should initiate and indicate to the user the process of resuming normal operation within one second of de-assertion of the ~~W_DISABLE#~~wireless disable signal. Due to the potential of a software disable state, the combination of both the software state and ~~W_DISABLE#~~wireless disable signal assertion state must be determined before resuming normal operation. Table 3-7 illustrates this requirement as a function of ~~W_DISABLE#~~wireless disable signal and the software control setting such that the radio's RF operation remains disabled unless both the hardware and software are set to enable the RF features of the card.

Table 3-7: Radio Operational States

~~W_DISABLE#~~Wireless Disable Signal	SW Control Setting*	Radio Operation
De-asserted (HIGH)	Enable Radio	Enabled (RF operation allowed)
De-asserted (HIGH)	Disable Radio	Disabled (no RF operation allowed)
Asserted (LOW)	Enable Radio	Disabled (no RF operation allowed)
Asserted (LOW)	Disable Radio	Disabled (no RF operation allowed)

* This control setting is implementation specific; this column represents the collective intention of the host software to manage radio operation.

The system is required to assure that ~~W_DISABLE#~~each wireless disable signal be in a deterministic state (asserted or de-asserted) whenever power is applied to the add-in; i.e., +3.3Vaux is present.

Change Table 3-8 as follows:

Table 3-8: System Connector Pin-out

Pin #	Name	Pin #	Name
75	GND	76	MLDIR
73	ML0p	74	GND
71	ML0n	72	GND
69	GND	70	ML1p
67	GND	68	ML1n
65	ML2p	66	GND
63	ML2n	64	GND
61	GND	62	ML3p
59	GND	60	ML3n

Pin #	Name	Pin #	Name
57	AUXp	58	GND
55	AUXn	56	GND
53	DMC#	54	HPD
Mechanical Key			
51	~~Reserved~~W_DISABLE2#	52	+3.3Vaux
49	Reserved	50	GND
47	Reserved	48	+1.5V
45	Reserved	46	LED_WPAN#
43	GND	44	LED_WLAN#
41	+3.3Vaux	42	LED_WWAN#
39	+3.3Vaux	40	GND
37	GND	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3Vaux
21	GND	22	PERST#
19	UIM_IC_DP	20	W_DISABLE1#
17	UIM_IC_DM	18	GND
Mechanical Key			
15	GND	16	UIM_SPU
13	REFCLK+	14	UIM_RESET
11	REFCLK-	12	UIM_CLK
9	GND	10	UIM_DATA
7	CLKREQ#	8	UIM_PWR
5	COEX2	6	1.5V
3	COEX1	4	GND
1	WAKE#	2	3.3Vaux

Change Section 3.4.1. as follows:

3.4.1. Logic Signal Requirements

The 3.3V card logic levels for single-ended digital signals (WAKE#, CLKREQ#, PERST#, W_DISABLE1#, W_DISABLE2#, and MLDIR) are given in Table 3-9.

Table 3-9: DC Specification for 3.3V Logic Signaling

Symbol	Parameter	Conditions	Min	Max	Units	Notes
+3.3Vaux	Supply Voltage		3.3 – 9%	3.3 + 9%	V	3
V_{IH}	Input High Voltage		2.0	3.6	V	1
V_{IL}	Input Low Voltage		-0.5	0.8	V	1
I_{OL}	Output Low Current for open-drain signals	0.4 V	4		mA	2
I_{IN}	Input Leakage Current	0 V to 3.3 V	-10	+10	µA	1
I_{LKG}	Output Leakage Current	0 V to 3.3 V	-50	+50	µA	1
C_{IN}	Input Pin Capacitance			7	pF	1
C_{OUT}	Output Pin Capacitance			30	pF	2

Notes:
1. Applies to PERST#, W_DISABLE1#, W_DISABLE2#, MLDIR (when applicable), and WAKE# (when used for OBFF signaling).
2. Applies to CLKREQ# and WAKE#.
3. As measured at the card connector pad.