PCI-SIG ENGINEERING CHANGE NOTIFICATIION

TITLE:	Change Root Complex Event Collector Class Code
DATE:	Initial Submission: 17 September 2012 Updated: 20 September 2012 Approved for Member Review: 25 October 2012 Approved for Publication: 13 December 2012
AFFECTED DOCUMENT:	PCI Class Code Specification, Revision 1.3 PCI Express Base Specification, Revision 3.0
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Part I

1. Summary of the Functional Changes

Change the Sub-Class assignment for Root Complex Event Collector from 06h to 07h.

2. Benefits as a Result of the Changes

The PCI Express Base Specification assigned Sub-Class 06h to Root Complex Event Collector. This assignment was not incorporated into the PCI Code and ID Assignment Specification and was overlooked when assigning that Sub-Class to IOMMU.

This ECN changes the assignment for Root Complex Event Collectors to remove the duplication.

3. Assessment of the Impact

Some software will require changes.

Root Complex hardware may require changes.

4. Analysis of the Hardware Implications

It is strongly recommended, but not strictly required, that new designs containing a Root Complex Event Collector use the new assignment.

IOMMU designs are not affected.

No other components are affected.

5. Analysis of the Software Implications

Software that uses the Sub-Class value to locate a Root Complex Event Collector will need to change to be tolerant of either sub-Class 06h or 07h.

The Device/Port Type field can always be used to definitively identify a Root Complex Event Collector (see Section 7.8.2 of the PCI Express Base Specification).

Software that uses the Sub-Class value to identify an IOMMU is unaffected.

Software that uses Vendor ID / Device ID to identify either Function type is unaffected.

6. Analysis of the C&I Test Implications

Root Complex tests may require changes.

Part II

Detailed Description of the change

In the PCI Express Base Specification, change section 1.3.4 as follows (Page 46, Line 1):

1.3.4. Root Complex Event Collector

- A Root Complex Event Collector provides support for terminating error and PME messages from Root Complex Integrated Endpoints.
- A Root Complex Event Collector must follow all rules for a Root Complex Integrated Endpoint.
- A Root Complex Event Collector is not required to decode any memory or IO resources.
- A Root Complex Event Collector is identified by its Device/Port Type value (see section 7.8.2).
- A Root Complex Event Collector has the Base Class 08h, Sub-Class ~~06h~~ 07h and Programming Interface 00h.[1]
- A Root Complex Event Collector resides on the same Logical Bus as the Root Complex Integrated Endpoints it supports.
- Multiple Root Complex Event Collectors are permitted to reside on a single Logical Bus.
- A Root Complex Event Collector explicitly declares supported Root Complex Integrated Endpoints through the Root Complex Event Collector Endpoint Association Capability.
- Root Complex Event Collectors are optional.

[1] Since an earlier version of this specification used Sub-Class 06h for this purpose, an implementation is still permitted to use Sub-Class 06h, but this is strongly discouraged.

In the PCI Code and ID Assignment Specification, change Section 1.9 as follows (Page 14, Line 1):

1.9. Base Class 08h

This base class is defined for all types of generic system peripherals. Several sub-class values are defined, most of these having a specific well-known Programming Interface.

Base Class	Sub-Class	Programming Interface	Meaning
08h	00h	00h	Generic 8259 PIC
		01h	ISA PIC
		02h	EISA PIC
		10h	I/O APIC interrupt controller (see Note 1 below)
		20h	I/O(x) APIC interrupt controller
	01h	00h	Generic 8237 DMA controller
		01h	ISA DMA controller
		02h	EISA DMA controller
	02h	00h	Generic 8254 system timer
		01h	ISA system timer
		02h	EISA system timers (two timers)
		03h	High Performance Event Timer
	03h	00h	Generic RTC controller
		01h	ISA RTC controller
	04h	00h	Generic PCI Hot-Plug controller
	05h	00h	SD Host controller
	06h	00h	IOMMU
	07h	00h	Root Complex Event Collector (see Note 2 below)
	80h	00h	Other system peripheral

Notes:

1. For I/O APIC Interrupt Controller, the Base Address register at offset 10h is used to request a minimum of 32 bytes of non-prefetchable memory. Two registers within that space are located at Base+00h (I/O Select register) and Base+10h (I/O Window register).
2. Some versions of the PCI Express Base Specification defined Root Complex Event Collectors to use Sub-Class 06h. Implementations are permitted to use Sub-Class 06h for this purpose, but this practice is strongly discouraged. The Device/Port Type field value can be used to accurately identify all Root Complex Event Collectors.