



PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	8.0 GT/s Receiver Impedance
DATE:	Updated May 26, 2011, Final Approval August 18,2011
AFFECTED DOCUMENT:	PCI Express Base Specification, Revision 3.0
SPONSOR:	IBM Corporation

Part I

1. Summary of the Functional Changes

Receivers that operate at 8.0 GT/s with an impedance other than the range defined by the Z_{RX-DC} parameter for 2.5 GT/s (40-60 Ohms) must meet additional behavior requirements in the following LTSSM states: Polling, Rx_L0s, L1, L2, and Disabled.

2. Benefits as a Result of the Changes

The changes address Link bring-up deadlock scenarios that can occur when an 8.0 GT/s receiver is not detected in the LTSSM Detect state.

3. Assessment of the Impact

The changes affect all Ports with Receivers that operate at 8.0 GT/s with an impedance other than the range defined by the Z_{RX-DC} parameter for 2.5 GT/s (40-60 Ohms).

4. Analysis of the Hardware Implications

The changes address Link bring-up deadlock scenarios that can occur when an 8.0 GT/s receiver is not detected in the LTSSM Detect state.

5. Analysis of the Software Implications

None.

Part II

Detailed Description of the change

Change Section 4.2.6.2.2, page 254 as follows:

4.2.6.2.2 Polling.Compliance

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Subsequent entries to Polling.Compliance repeat the above sequence. For example, the state sequence which causes a Port to transmit the Compliance pattern at a data rate of 5.0 GT/s and a de-emphasis level of -6 dB is: Polling.Active, Polling.Compliance (2.5 GT/s and -3.5 dB), Polling.Active, Polling.Compliance (5.0 GT/s and -3.5 dB), Polling.Active, Polling.Compliance (5.0 GT/s and -6 dB).

The sequence must be set to Setting #1 in the Polling.Configuration state if the Port's Receivers do not meet the Z_{RX-DC} specification for 2.5 GT/s when they are operating at 8.0 GT/s or higher data rates (see Table 4-24). All Ports are permitted to set the sequence to Setting #1 in the Polling.Configuration state.

Change Section 4.2.6.2.3, page 258 as follows:

4.2.6.2.3 Polling.Configuration

- Receiver must invert polarity if necessary (see Section 4.2.4.4).
- The Transmit Margin field of the Link Control 2 register must be reset to 000b on entry to this substate.
- The Transmitter's Polling.Compliance sequence setting is updated, if required, as described in Section 4.2.6.2.2.
- Transmitter sends TS2 Ordered Sets with Link and Lane numbers set to PAD on all Lanes that detected a Receiver during Detect.
 - The Data Rate Identifier Symbol of the TS2 Ordered Sets must advertise all data rates that the Port supports, including those that it does not intend to use.
- The next state is Configuration after eight consecutive TS2 Ordered Sets, with Link and Lane numbers set to PAD, are received on any Lanes that detected a Receiver during Detect, and 16 TS2 Ordered Sets are transmitted after receiving one TS2 Ordered Set.
- Otherwise, next state is Detect after a 48 ms timeout.

Change Section 4.2.6.6.1.2, page 300 as follows:

4.2.6.6.1.2. Rx_L0s.Idle

- Next state is Rx_L0s.FTS if the Receiver detects an exit from Electrical Idle on any Lane of the configured Link.
- Next state is Rx_L0s.FTS after a 100 ms timeout if the current data rate is 8.0 GT/s or higher and the Port's Receivers do not meet the Z_{RX-DC} specification for 2.5 GT/s (see Table 4-24). All Ports are permitted to implement the timeout and transition to Rx_L0s.FTS when the data rate is 8.0 GT/s or higher.

Change Section 4.2.6.7.2, page 304 as follows:

4.2.6.7.2 L1.Idle

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- Next state is Recovery if any Receiver detects exit from Electrical Idle or directed after remaining in this substate for a minimum of 40 ns in speeds other than 2.5 GT/s.
 - Note: A minimum stay of 40 ns is required in this substate in speeds other than 2.5 GT/s to account for the delay in the logic levels to arm the Electrical Idle detection circuitry in case the Link enters L1 and immediately exits the L1 state.
 - A Port is allowed to set the directed_speed_change variable to 1b following identical rules described in L0 for setting this variable. When making such a transition, the changed_speed_recovery variable must be reset to 0b. A Port may also go through Recovery back to L0 and then set the directed_speed_change variable to 1b on the transition from L0 to Recovery.
 - A Port is also allowed to enter Recovery from L1 if directed to change the Link width. The Port must follow identical rules for changing the Link width as described in the L0 state.
- Next state is Recovery after a 100 ms timeout if the current data rate is 8.0 GT/s or higher and the Port's Receivers do not meet the Z_{RX-DC} specification for 2.5 GT/s (see Table 4-24). All Ports are permitted, but not encouraged, to implement the timeout and transition to Recovery when the data rate is 8.0 GT/s or higher.



IMPLEMENTATION NOTE

100 ms Timeout in L1

Ports that meet the Z_{RX-DC} specification for 2.5 GT/s while in the L1.Idle state and are therefore not required to implement the 100 ms timeout and transition to Recovery should avoid implementing it, since it will reduce the power savings expected from the L1 state.

Change Section 4.2.6.7.2, page 305 as follows:

4.2.6.8.1 L2.Idle

- ~~☐ All Rx termination must remain enabled in low impedance.~~
- ☐ All Receivers must meet the Z_{RX-DC} specification for 2.5 GT/s within 1 ms (see Table 4-24).

Change Section 4.2.6.9, page 307 as follows:

4.2.6.9 Disabled

- ☐ All Lanes transmit 16 to 32 TS1 Ordered Sets with the Disable Link bit asserted and then transition to Electrical Idle.
 - The EIOS (one EIOS if the current Link speed is 2.5 GT/s or 8.0 GT/s and two consecutive EIOSs if the current Link speed is 5.0 GT/s) must be sent prior to entering Electrical Idle.
 - The DC common mode voltage does not have to be within specification.
- ☐ If an EIOS was transmitted (one if the current Link speed is 2.5 GT/s or 8.0 GT/s and two consecutive ones if the current Link speed is 5.0 GT/s) and an EIOS was received on any Lane (even while transmitting TS1 with the Disable Link bit asserted), then:
 - LinkUp = 0b (False)
 - ◆ At this point, the Lanes are considered Disabled.
 - For Upstream Ports: All Receivers must meet the Z_{RX-DC} specification for 2.5 GT/s within 1 ms (see Table 4-24).
 - For Upstream Ports: The next state is Detect when Electrical Idle Exit is detected at the Receiver.