PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	PCIe Link Activation
DATE:	Introduced: 17 May 2017 Updated: 7 December 2017 Final Approval: 7 December 2017
AFFECTED DOCUMENT:	PCI Express Base Specification, Revision 4.0
SPONSOR:	Intel Corp.

Part I

1. Summary of the Functional Changes

Link Activation allows software to temporarily disable Link power management, enabling the avoidance of the architecturally mandated stall for software-initiated L1 Substate exits.

2. Benefits as a Result of the Changes

This ECN improves PCIe as noted in item 1.

3. Assessment of the Impact

Link Activation is an optional feature that has no effect on existing implementations. It requires both new hardware and new software to be used.

4. Analysis of the Hardware Implications

Link Activation is optional and disabled by default. Hardware changes are required on Downstream Ports to support **Link Activation**. Upstream Ports are not affected.

5. Analysis of the Software Implications

System Software changes are required on systems that wish to support **Link Activation**.

6. Analysis of the C&I Test Implications

This ECN allocates previously reserved bits and requires the creation of new tests for the new register fields. New C & I tests would be required if it is desirable to extend C & I coverage to explicitly evaluate these new features.

Part II

Detailed Description of the change

Add a Section, 5.5.6:

5.5.6 Link Activation

Link Activation is an optional mechanism to temporarily disable L1 Substates. Link Activation is used to bring a Link out of L1.1/L1.2, avoiding potential stalls. An example of one such stall is the stall associated with a Configuration Write to perform a $D3_{hot}$ to D0 transition. Link Activation can also be used to indirectly indicate to a Device that it should avoid long-latency internal power management during latency-sensitive or time critical operations.

The following rules apply to Link Activation:

- A Downstream Port is permitted to support Link Activation, as indicated by the Link Activation Supported bit in the L1 PM Substates Capabilities register being Set.
- The Link Activation Control bit must have no effect on Port behavior unless one or more of the following bits are Set:
  - PCI-PM L1.2 Enable
  - PCI-PM L1.1 Enable
- When the Link Activation Control bit is Set, the Port that is about to enter L1 must assert, and while in L1 maintain as asserted, the CLKREQ# signal.
- If the Link Activation Control bit is Clear, the Link Activation mechanism does not impose any additional requirements on the state of the CLKREQ# signal.
- If the Port is enabled for edge-triggered interrupt signaling using MSI or MSI-X, an interrupt message must be sent every time the logical AND of the following conditions transitions from FALSE to TRUE:
  - The associated vector is unmasked (not applicable if MSI does not support PVM)
  - The Link Activation Interrupt Enable bit is Set
  - The Link Activation Control bit is Set
  - The Link Activation Status bit is Set. Note that Link Activation interrupts always use the MSI or MSI-X vector indicated by the Interrupt Message Number field in the PCI Express Capabilities register.
- If the Port is enabled for level-triggered interrupt signaling using the INTx messages, the virtual INTx wire must be asserted whenever and as long as the following conditions are satisfied:
  - The Interrupt Disable bit in the Command register is Clear.
  - The Link Activation Interrupt Enable bit is Set
  - The Link Activation Control bit is Set
  - The Link Activation Status bit is Set
- The Link Activation Status bit must be Set every time the logical AND of the following conditions transitions from FALSE to TRUE:

- Either the PCI-PM L1.2 Enable bit or the PCI-PM L1.1 Enable bit (or both) are Set
- The Link Activation Control bit is Set
- The Link is not in an L1 Substate

Make the following changes to Section 7.8.3:

7.8.3 L1 PM Substates Extended Capability

The PCI Express L1 PM Substates Capability is an optional Extended Capability, that is required if L1 PM Substates is implemented at a Port. The L1 PM Substates Extended Capability structure is defined as shown in Figure 7-102.

For a Multi-Function Device associated with an Upstream Port implementing L1 PM Substates, this Extended Capability Structure must be implemented only in Function 0, and must control the Upstream Port's Link behavior on behalf of all the Functions of the device.

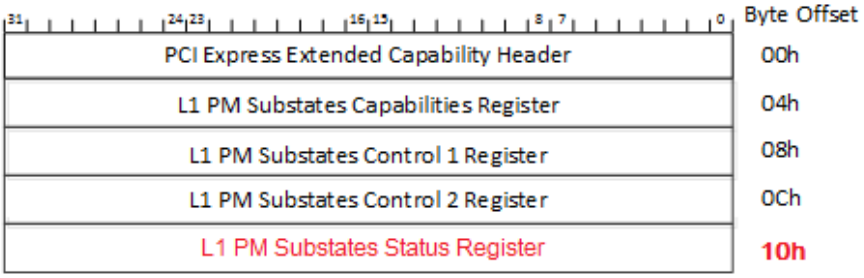

Figure 7-102: L1 PM Substates Capability

In Table 7-82, edit as shown:

…

Table 7-82: L1 PM Substates Extended Capability Header

Location	Register Description	Attributes
…	…	…
19:16	**Capability Version** – This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. ~~Must be 1h for this version of the specification.~~ This field must be 2h if the L1 PM Substates Status Register is implemented and must be 1h otherwise.	HwInit
…	…	…

In Section 7.8.3.2, edit as shown:

…

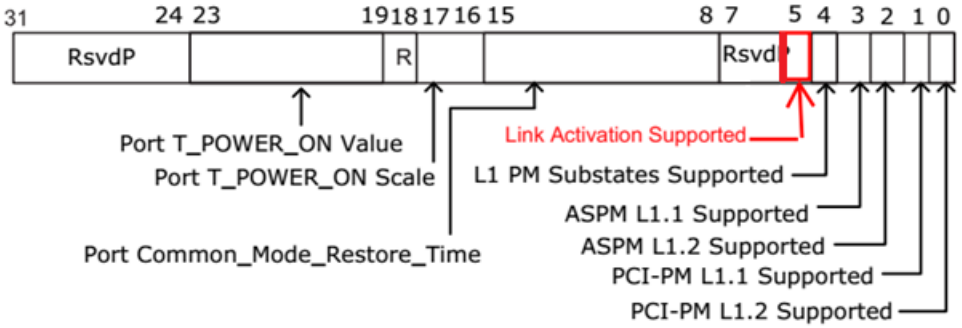

Figure 7-103: L1 PM Substates Capabilities Register

Table 7-83: L1 PM Substates Capabilities Register

Location	Register Description	Attributes
…	…	…
5	**Link Activation Supported –** For Downstream Ports, when Set, this bit indicates that this Port supports Link Activation. This bit is of type RsvdP for Upstream Ports.	HwInit/RsvdP
7:6~~:5~~	**Reserved**	RsvdP

….

In Section 7.8.3.3, edit as shown:

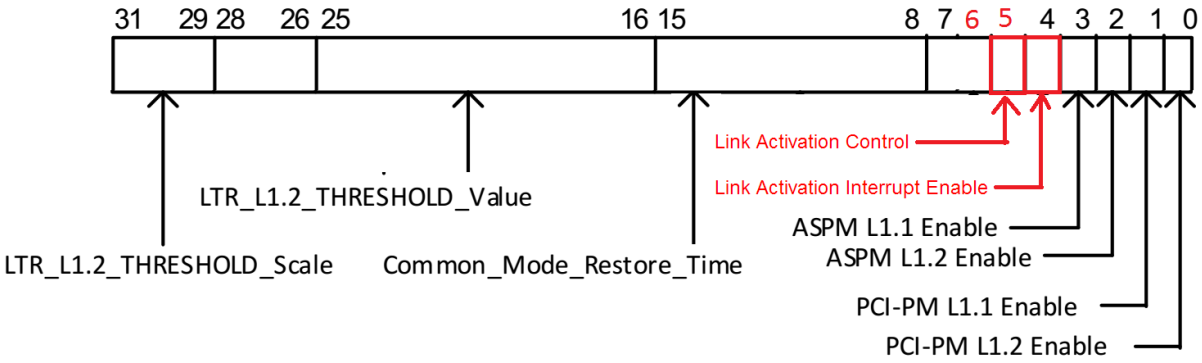

Figure 7-104: L1 PM Substates Control 1 Register

Table 7-84: L1 PM Substates Control 1 Register

Location	Register Description	Attributes
…	…	…
4	**Link Activation Interrupt Enable** – When set this bit enables the generation of an interrupt to indicate the completion of the Link Activation process. See Section 5.5.6 for details. Required for Downstream Ports when the Link Activation Supported bit is Set, otherwise it is permitted to be hardwired to 0b. Must be RsvdP for Upstream Ports. Default value is 0b.	RW/RsvdP
5	**Link Activation Control –** When this bit is Set, the Port must initiate the Link Activation process. See section 5.5.6 for details Required for Downstream Ports when the Link Activation Supported bit is Set, otherwise it is permitted to be hardwired to 0b. Must be RsvdP for Upstream Ports. Default value is 0b.	RW/RsvdP
7:6	**Reserved**	RsvdP
…	…	…

Add Section 7.8.3.5, as shown:

7.8.3.5 L1 PM Substates Status Register (Offset 10h)

Hardware must implement this register if the Capability Version in the L1 PM Substates is 2h or greater. This register is not present if the Capability Version is 1h.

Figure 7-XXX: L1 PM Substates Status Register

Table 7-YYY: L1 PM Substates Status Register

Location	Register Description	Attributes
0	**Link Activation Status –** Indicates the status of Link Activation. See section 5.5.6 for details. Required for Downstream Ports when the Link Activation Supported bit is Set, otherwise it is hardwired to 0b. Must be RsvdZ for Upstream Ports. Default value is 0b.	RW1C/RsvdZ
31:1	**Reserved**	RsvdZ