PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Extended Message Data for MSI
DATE:	May 10, 2016
AFFECTED DOCUMENTS:	PCI Local Bus Specification Revision 3.0 PCI Express® Base Specification Revision 3.1 Single Root I/O Virtualization and Sharing Specification Revision 1.1
SPONSORS:	Jim Panian, Qualcomm Technologies Inc. Joe Cowan, Hewlett Packard Enterprise

Part I

1. Summary of the Functional Changes

MSI is enhanced to include an Extended Message Data Field for the function generating the interrupt. The MSI Capability Structure is modified to enable the new feature to be enabled/disabled; and a new Extended Message Data Field to be configured.

This change only applies to MSI and not MSI-X.

2. Benefits as a Result of the Changes

Enables the MSI to pass an additional 16-bit Extended Message Data value in addition to the 16-bit Message Data value already specified. This provides MSI with a similar capability to MSI-X which passes 32-bits of Message Data.

3. Assessment of the Impact

This feature is optional. It will have no impact on existing implementations.

4. Analysis of the Hardware Implications

Hardware changes are required to take advantage of this new optional capability.

5. Analysis of the Software Implications

Software must be modified to query for support of the feature, enable the feature, and to configure the Extended Message Data field.

6. Analysis of the C&I Test Implications

It is expected that HW implementing this optional capability will pass existing C & I tests. New C & I tests would be required in order to evaluate the implementation of this capability.

Part II

Detailed Description of the change to the PCI Local Bus Specification Revision 3.0

Change Section 6.8.1, MSI Capability Structure, page 232 as follows:

6.8.1. MSI Capability Structure

The capabilities mechanism (refer to Section 6.7) is used to identify and configure an MSI or MSI-X capable device. The MSI capability structure is described in the current section. The MSI-X capability structure is described in Section 6.8.2.

The MSI capability structure is illustrated in Figure 6-9. Each device function that supports MSI (in a multi-function device) must implement its own MSI capability structure. More than one MSI capability structure per function is prohibited, but a function is permitted to have both an MSI and an MSI-X capability structure.

Capability Structure for 32-bit Message Address

31 — 16	15 — 8	7 — 0	
Message Control	Next Pointer	Capability ID	Capability Pointer
Message Address			Capability Pointer + 04h
Extended Message Data (if implemented)	Message Data		Capability Pointer + 08h

Capability Structure for 64-bit Message Address

31 — 16	15 — 8	7 — 0	
Message Control	Next Pointer	Capability ID	Capability Pointer
Message Address			Capability Pointer + 04h
Message Upper Address			Capability Pointer + 08h
Extended Message Data (if implemented)	Message Data		Capability Pointer + 0Ch

Capability Structure for 32-bit Message Address and Per-vector Masking

31 — 16	15 — 8	7 — 0	
Message Control	Next Pointer	Capability ID	Capability Pointer
Message Address			Capability Pointer + 04h
Extended Message Data (or Reserved)	Message Data		Capability Pointer + 08h
Mask Bits			Capability Pointer + 0Ch
Pending Bits			Capability Pointer + 10h

Capability Structure for 64-bit Message Address and Per-vector Masking

31 — 16	15 — 8	7 — 0	
Message Control	Next Pointer	Capability ID	Capability Pointer
Message Address			Capability Pointer + 04h
Message Upper Address			Capability Pointer + 08h
Extended Message Data (or Reserved)	Message Data		Capability Pointer + 0Ch
Mask Bits			Capability Pointer + 10h
Pending Bits			Capability Pointer + 14h

Figure 6-9: MSI Capability Structures

To request service, an MSI function writes the contents of the Message Data register, and if enabled, the Extended Message Data register, to the address specified by the contents of the Message Address register (and, optionally, the Message Upper Address register for a 64-bit message address). A read of the address specified by the contents of the Message Address register produces undefined results.

A function supporting MSI implements one of four MSI Capability Structure layouts illustrated in Figure 6-9, depending upon which optional features are supported. If a function supports 64-bit addressing (DAC) when acting as a master, the function is required to implement 64-bit addressing.

The message control register indicates the function's capabilities and provides system software control over MSI.

Each field is further described in the following sections. Reserved registers and bits always return 0 when read and write operations have no effect. Read-only registers return valid data when read and write operations have no effect.

Change Section 6.8.1.3, MSI Capability Structure, page 234 as follows:

6.8.1.3. Message Control for MSI

This register provides system software control over MSI. After reset, MSI is disabled. If MSI and MSI-X are both disabled, the function requests servicing via its INTx# pin (if supported). System software can enable MSI by setting bit 0 of this register. System software is permitted to modify the Message Control register's read/write bits and fields. A device driver is not permitted to modify the Message Control register's read/write bits and fields.

Bits	Field	Description
15::~~09~~ 11	Reserved	Always returns 0 on a read, and a write operation has no effect.
10	Extended Message Data Enable	If 1, the function is enabled to provide Extended Message Data. If 0, the function is not enabled to provide Extended Message Data. This bit's state after reset is 0 (Extended Message Data is disabled). This bit must be read/write if the Extended Message Data Capable bit is 1; otherwise it must be hardwired to 0.
9	Extended Message Data Capable	If 1, the function is capable of providing Extended Message Data. If 0, the function does not support providing Extended Message Data. This bit is read only.
…	…	…

Change Section 6.8.1.6, page 234 as follows:

6.8.1.6. Message Data for MSI

Bits	Field	Description
15::00	Message Data	System-specified message data. If the Message Enable bit (bit 0 of the Message Control register) is set, the message data is driven onto the lower word (AD[15::00]) of the memory write transaction's data phase. ~~AD[31::16] are driven to zero during the memory write transaction's data phase.~~ C/BE[3::0]# are asserted during the data phase of the memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of "010" indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is "000", the function is not permitted to modify the message data. This field is read/write.

Add Section 6.8.1.7, page 234 as follows. Move all other lower sections down:

6.8.1.7. Extended Message Data for MSI (Optional)

Bits	Field	Description
15::00	Extended Message Data	System-specified message data. This register is optional. For the MSI Capability structures without Per-vector Masking, it must be implemented if the Extended Message Data Capable bit is 1; otherwise, it is outside the MSI Capability structure and undefined. For the MSI Capability structures with Per-vector Masking, it must be implemented if the Extended Message Data Capable bit is 1; otherwise, it is Reserved. If Extended Message Data Enable bit (bit 10 of the Message Control register) is set, AD[31::16] are driven during the memory write transaction's data phase to the Extended Message Data field value; otherwise, AD[31::16] are driven to zero. The state of these bits after reset must be 0. If implemented, this field must be read/write.

Change Section 6.8.3.1, page 247 as follows:

System software initializes the MSI capability structure's Message Data register with the lower 16 bits of a system specified data value. When Extended Message Data Capable bit is 0, ~~Care~~ care must be taken to initialize only the Message Data register (i.e., a 2-byte value) and not modify the upper two bytes of that DWORD location.

If the Extended Message Data Capable bit is set and system software supports 32-bit vector values, system software may initialize the MSI capability structure's Extended Message Data register with the upper 16 bits of a system specified data value, and then set the Extended Message Data Enable bit to 1.

Change Section 6.8.3.4, page 249 as follows:

For MSI when Extended Message Data Enable bit is 0, the DWORD that is written is made up of the value in the MSI Message Data register in the lower two bytes and zeroes in the upper two bytes. For MSI when Extended Message Data Enable bit is 1, the DWORD that is written is made up of the value in the MSI Message Data register in the lower two bytes and the value in the MSI Extended Message Data register in the upper two bytes.

Detailed Description of the change to the PCI Express® Base Specification Revision 3.1

Change Section 6.1, page 499 as follows:

6.1. Interrupt and PME Support

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In addition to PCI INTx compatible interrupt emulation, PCI Express requires support of MSI or MSI-X or both. The PCI Express MSI and MSI-X mechanisms are compatible with those defined in the *PCI Local Bus Specification* and the *Extended Message Data for MSI ECN*.

Change Section 7.7, page 681 as follows:

7.7. MSI and MSI-X Capability Structures

All PCI Express device Functions that are capable of generating interrupts must implement MSI or MSI-X or both. MSI, MSI-X, and their Capability structures are defined in the *PCI Local Bus Specification* and the *Extended Message Data for MSI ECN*. The functionality associated with these structures defined by conventional PCI is also required for PCI Express. Only added requirements associated with PCI Express are described here.

Detailed Description of the change to the Single Root I/O Virtualization and Sharing Specification Revision 1.1

Change Section 5.1.1, page 83 as follows:

5.1.1. MSI Interrupts

MSI Capability is defined in the *PCI Local Bus Specification* and the *Extended Message Data for MSI ECN*.