PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Separate Refclk Independent SSC Architecture (SRIS) JTOL and SSC Profile Requirements
DATE:	Updated 31 March 2014
AFFECTED DOCUMENT:	Separate Refclk Independent SSC Architecture (SRIS) ECN, PCI Express Base Spec. Rev 3.1
SPONSOR:	Intel

Part I

1. Summary of the Functional Changes

Modifies specifications to provide revised JTOL curve for SRIS mode and provides additional frequency domain constraint of SSC profile jitter on reference clocks.

2. Benefits as a Result of the Changes

Allows more flexibility in CDR design for SRIS mode.

3. Assessment of the Impact

4. Analysis of the Hardware Implications

1. Reference clocks may have to change to meet SSC jitter profile requirements. However – it is believed that most (if not all) current reference clocks with SSC already meet the requirements.

2. SRIS CDR designs may be optimized to improve high frequency jitter tolerance.

5. Analysis of the Software Implications

None.

6. Analysis of the C&I Test Implications

None.

Part II

Detailed Description of the change

Additions are noted in blue.

Modify Section 4.3.4.4.6 as follows:

4.3.4.4.6. Separate Refclk with Independent SSC (SRIS) RX Architecture

The testing of the Separate Refclk with Independent SSC RX Architecture is the same as the Common clock architecture with the following modifications:

- ❑ The DUT shall be driven with an independent SSC modulated reference clock for all testing. SSC shall meet the frequency limits and maximum deviation range defined in table 4-34.
- ❑ The generator shall be driven with an independent SSC modulated reference clock for the stressed voltage test. SSC shall have a triangular profile and meet the frequency limits and maximum deviation range defined in table 4-34.
- ❑ The generator shall provide a 33 kHz Sj tone with 25 ns peak to peak amplitude during the stressed eye test.
- ❑ The generator shall transmit with a nominal unit interval of 125.3125 ps during the stressed eye test.
- ❑ Sj shall be swept over the range given by equation 4-x0 and shown in Figure 4-x0 during the stressed eye test:

$$\text{Sj in Unit Intervals} = \begin{cases} \dfrac{5713941}{F^{1.1262}} & (400\ \text{KHz} \le F < 1\ \text{MHz}) \\ \dfrac{10^6}{F} & (1\ \text{MHz} \le F < 10\ \text{MHz}) \\ 0.1 & (F \ge 10\ \text{MHz}) \end{cases}$$

where F is frequency in Hz

Equation 4-x0 SRIS JTOL Curve

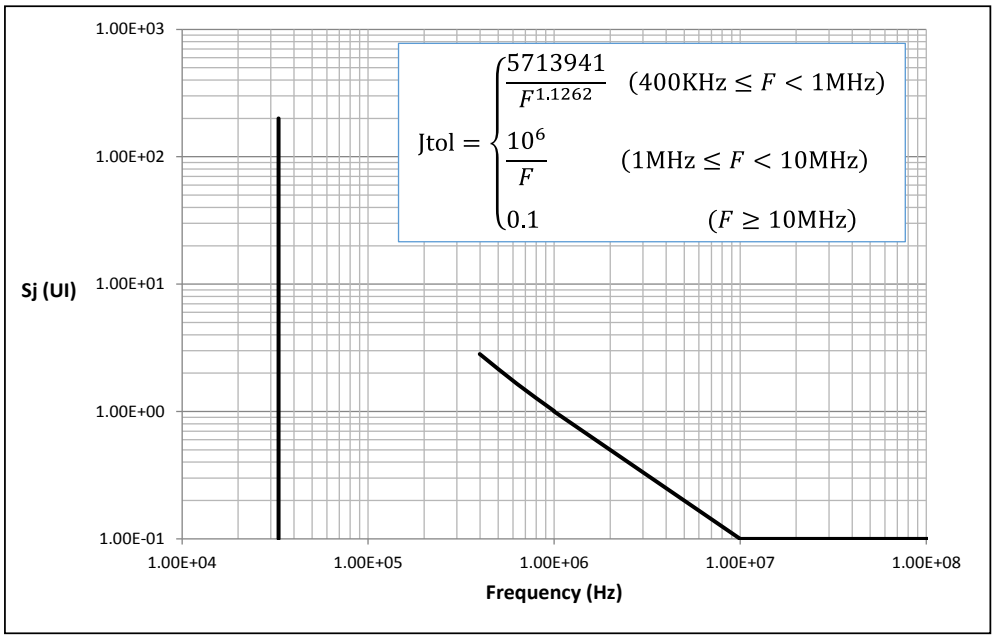

Figure 4-x0: Swept Sj Mask

Change Section 4.3.7.3, page 401 as follows:

4.3.7.3. Bit Rate Tolerance and Spread Spectrum Clocking

The tolerance for the Refclk is 100 MHz ±300 ppm, where this number is defined with spread spectrum clocking (SSC) turned off. SSC may be implemented as a method of reducing EMI. The Refclk rate for a single source may be modulated from +0 to -5000 ppm of the nominal data rate frequency, at a modulation rate lying within a 30 kHz – 33 kHz range. The maximum rate of change of the frequency on a reference clock with SSC active is 1250 ppm/us. Refclks that operate with SSC need to meet an additional frequency dependent phase jitter limit at low frequency. The data points in Table 0-x1 are used to construct a piece-wise linear graph from 30 kHz to 500 kHz and the unfiltered phase jitter of the reference clock in the frequency domain must fall below this graph as shown in Figure 4-x1.

Table 0-x1: Limits for phase jitter from the reference clock

Frequency	Maximum Peak to Peak Phase Jitter (ps)
30 kHz - 33 kHz	25000
100 kHz	1000
500 kHz	25

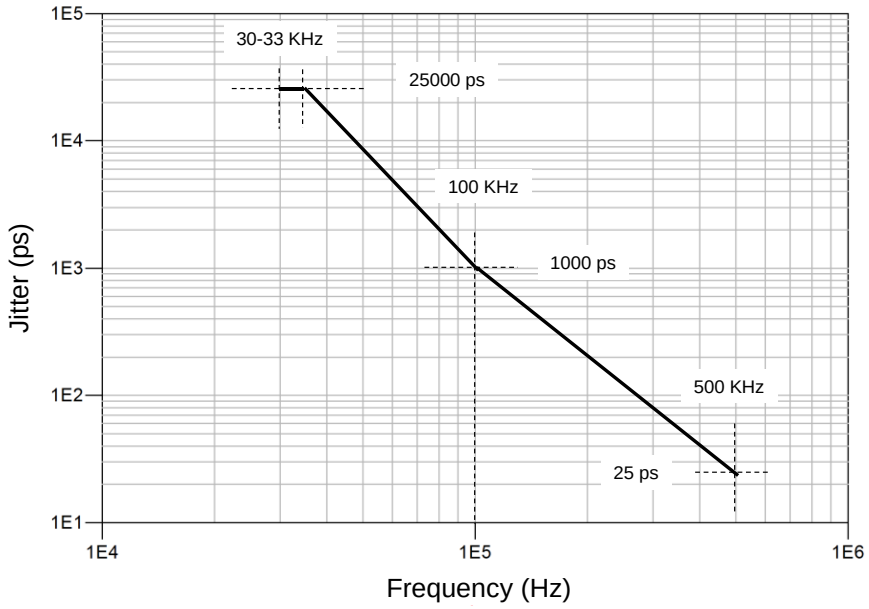

Figure 4-x1: Limits for phase jitter from the Reference Clock

Change Section 4.3.8.5 as follows:

4.3.8.5. Separate Refclk With Independent SSC (SRIS) Architecture

It is possible to architect an 8.0 GT/s PCI Express implementation with separate Refclk sources with independent SSC for the Tx and Rx. Figure 4-92a shows a high level block diagram of the separate Refclk architecture. Since this architecture employs two independent clock sources, the Receiver must be able to track and reject the phase drift due to the two independent SSC clocks. Changes in the logical sub-block are also required for the separate Refclk architecture; please refer to the logical sub-block section for all relevant information concerning SRIS (see Sections 4.2.5.6, 4.2.7, 4.2.7.3 and 4.2.7.4).

For the common Refclk architecture, the 8.0 GT/s specification contains a behavioral CDR model shown in Figure 4-67; it is a first order high-pass function with the -3 dB corner frequency at 10 MHz. Furthermore, during the receiver stressed jitter test (section 4.3.4.4), the receiver's CDR bandwidth and its low frequency jitter tracking capability are required to

pass the jitter mask (Figure 4-74). For the separate Refclk with independent SSC architecture, the CDR needs to have increased rejection at low frequency to handle the extra phase drift due to independent SSC. The new behavioral CDR jitter transfer function is shown in Figure 4-9x2 and Equation 4.3.8. The model CDR jitter transfer function is a continuous approximation of the inverse of the jitter tolerance curve for SRIS mode. The stressed jitter test is also modified to account for the requirement that the CDR can reject jitter from two separate reference clocks with SSC. Other test parameters and requirements such as transmitter jitters (Table 4-19) and the receive stressed voltage eye (Table 4-22) remain unchanged.

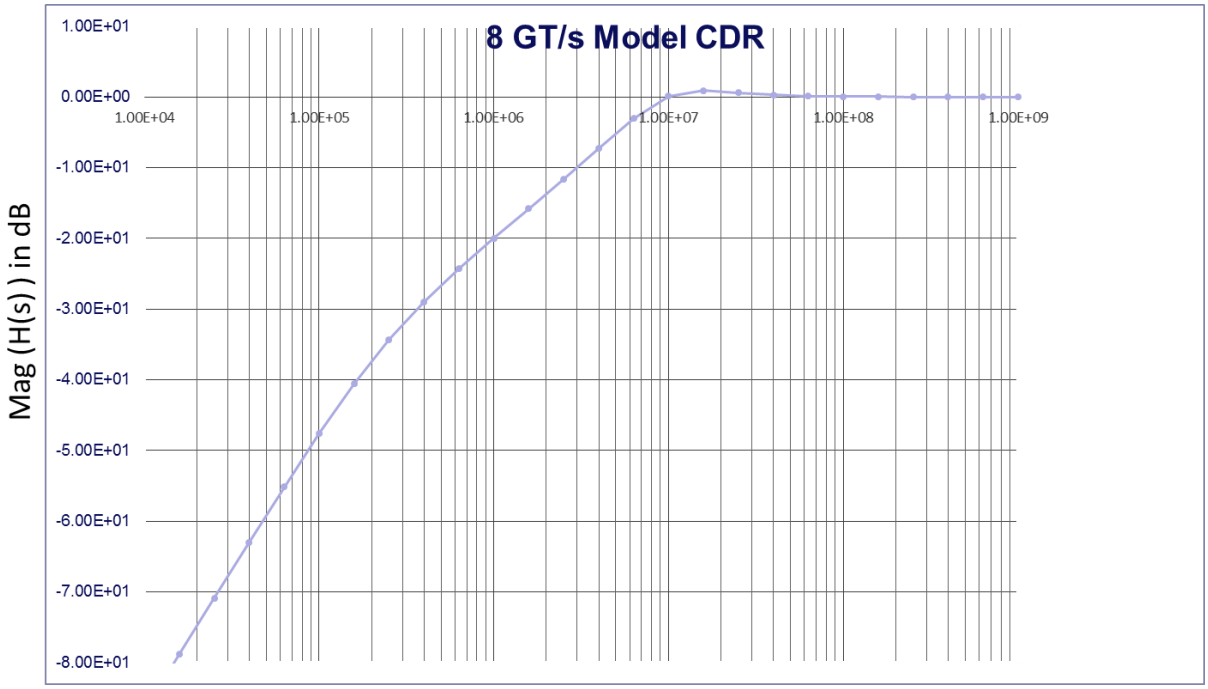

Figure 4-9x2: Informative CDR Jitter Transfer Function for the Separate Refclk With Independent SSC (SRIS) Architecture at 8.0 GT/s

$$H(s) = \frac{s^2}{s^2 + sA + B} \cdot \frac{s^2 + 2\zeta_2\omega_0 s + \omega_0^2}{s^2 + 2\zeta_1\omega_0 s + \omega_0^2}$$

Equation 4.3.8

$$\zeta_1 = \frac{1}{\sqrt{2}};\ \zeta_2 = 1;\ \omega_0 = 10^7 \times 2\pi$$

$$A = 10^7 \times 2\pi; B = 2.2 \times 10^{12} \times (2\pi)^2$$

The new CDR jitter transfer function impacts the Refclk jitter specification. This Refclk jitter number is captured as $T_{REFCLK\text{-}RMS\text{-}SRIS}$ in Table 4-9x2.

Table 4-9x2: Parameters for Separate Refclk With Independent SSC (SRIS) Architecture at 8.0 GT/s

Symbol	Description	Limits		Units
		Min	Max	
F_{REFCLK}	Refclk frequency	99.97	100.03	MHz
$T_{REFCLK\text{-}RMS\text{-}SRIS}$	RMS Refclk jitter for separate Refclk independent SSC architecture[1]		0.5	ps RMS
F_{SSC}	SSC frequency range	30	33	kHz
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation		+0.0/-0.5	%

Notes:
1. The Refclk jitter is measured after applying PLL transfer function (4 MHz, 2 dB) and CDR jitter transfer function defined in Figure 4-9x2.
2. The maximum rate of change of the clock frequency is 1250 ppm/us.
3. The maximum rate of change of the clock phase is 3 ns/us.