PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	SMBus interface for SSD Socket 2 and Socket 3
DATE:	August 11, 2014
AFFECTED DOCUMENT:	PCI Express M.2 Specification, Revision 1.0
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Part I

1. Summary of the Functional Changes

SMBus interface signals are included in sections 3.2 and 3.3 and related minor clarifications added to sections 1.2, 1.3, 2.2, 4.1, 4.2, 5.2.2, and 5.3.

2. Benefits as a Result of the Changes

This proposal adds SMBus interface for the use of SSD applications on M.2 Socket 2 and Socket 3. SMBus is a three pin low power and low bandwith interface. It is a side band mechanism that can be used to perform tasks related to drive management. Those tasks include discovery, configuration, and monitoring of the SSDs. It can be used for periodic drive health check, statistics gathering, and monitor temp sensor. It is a non-intrusive transport mechanism to carry management protocol for above purposes that does not interfere with SSD PCIe or SATA links.

3. Assessment of the Impact

The proposed pins are currently N/C for SSD Socket 2 and Socket 3. Hence there is no impact to existing modules.

4. Analysis of the Hardware Implications

Current N/C pins are used for SMBus interface. New designs can make use of this interface, existing SSD Socket 2 and Socket 3 hardware should have no impact.

5. Analysis of the Software Implications

New feature, no impact to existing software.

6. Analysis of the C&I Test Implications

New interface for test and compliance, no impact to existing test suites.

Part II

Detailed Description of the change

1.2 Targeted Application

The M.2 family of form factors is intended to support multiple function add-in cards/modules that include the following:

- WiFi
- Bluetooth
- Global Navigation Satellite Systems (GNSS)
- Near Field Communication (NFC)
- WiGig
- WWAN (2G, 3G and 4G)
- Solid-State Storage Devices
- Other & Future Solutions (e.g. Hybrid Digital Radio (HDR))

The M.2 Specification will cover multiple Host Interface solutions including:

- PCIe, PCIe LP
- HSIC
- SSIC
- USB
- SDIO
- UART
- PCM/ I2S
- I^2C
- SMBus
- SATA
- Display Port
- And future variants of the above

1.3 Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

- PCI Express Mini Card Electromechanical Specification, Revision 2.0
- PCI Express Specification Revision 3.0
- SDIO3.0
- SSIC – SuperSpeed USB Inter-Chip Supplement to the USB 3.0 Specification, Revision 1.0 as of May 3, 2012
- HSIC - High-Speed Inter-Chip USB Electrical Specification, Version 1.0 (September 23, 2007), plus HSIC ECN Disconnect Supplement to High Speed Inter Chip Specification Revision 0.94 (Sep 20, 2012)
- USB2.0 - Universal Serial Bus Specification, Revision 2.0, plus ECN and Errata, July 14, 2011, available from usb.org
- USB3.0 - Universal Serial Bus 3.0 Specification, Revision 1 plus ECN and Errata, July 29 2011, available from usb.org
- DisplayPort Standard Specifications, version 1.2
- *Serial ATA* Revision 3.1 Gold or later, available from sata-io.org
- *I^2C BUS Specifications*, Version 2.1, January 2000
- System Management Bus (SMBus) Specification, Version 2.0, August 3, 2000
- EIA-364 Electrical Connector/Socket Test Procedures including Environmental Classifications
- EIA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications

2.2. Card Type Naming Convention

Because there are various types of M.2 solutions and configurations, a standard naming convention will be employed to define the main features of a specific solution.

The naming convention will identify the following:

- The module size (width & length)
- The component assembly maximum Z-height for the top and bottom sides of the module
- The Mechanical Connector Key/Module key location/assignment or multiple locations/assignments

These naming conventions will clearly define the module functionality, what connector it coincides with, and what Z-heights are met. Figure 3 diagrams the naming convention.

The board width options are: 12 mm, 16.5 mm, the generic 22 mm, and the widest 30 mm board width.

The board length can scale to various lengths to support the content and expand as the content increases. The lengths supported are: 16 mm, 26 mm, 30 mm, 42 mm, 60 mm, 80 mm, and 110 mm.

Together these two dimensions make up the first part of the module type definition portion of the module name.

The next part of the name describes whether the module is single-sided or dual-sided and a secondary definition of what are the maximum Z-heights of the components on the top and bottom side of the module. Here we have specific Z-height limits that are either 1.5 mm, 1.35 mm, or 1.2 mm on the top side and 1.5mm, 1.35 mm, 0.7 mm and 0 mm on the bottom side. The letter S will designate Single-sided and the letter D will designate Dual-sided. This will be complimented with a number that designates the specific Z-height combination option.

The last section of the name will designate the mechanical connector key/module key name and the coinciding pin location. These will be designated by a letter from A to M. In cases where the module will have a dual key scheme to enable insertion of the module into two different keyed sockets, a second letter will be added to designate the second mechanical connector key/module key.

Key ID assignment must be approved by the PCI-SIG. Unauthorized Key IDs would render the modules incompatible with the M.2 specification.

Figure 4 on the following page shows an example of module Type 2242 – D2 – B – M.

Module Nomenclature
Sample Type 2242-D2-B-M

Type XX XX - XX - X - X*

Width (mm)
12
16
22
30

Length (mm)
16
26
30
42
60
80
110

Lable**	Component Max Ht (mm)	
	Top Max	Bottom Max
S1	1.2	0****
S2	1.35	0****
S3	1.5	0****
D1	1.2	1.35
D2	1.35	1.35
D3	1.5	1.35
D4	1.5	0.7
D5	1.5	1.5

Key ID	Pin	Interface
A	8-15	2x PCIe x1 / USB 2.0 / I2C / DP x4
B	12-19	PCIe x2/SATA/USB 2.0/USB 3.0/HSIC/SSIC/Audio/UIM/I2C/SMBus
C	16-23	Reserved for Future Use
D	20-27	Reserved for Future Use
E	24-31	2x PCIe x1 / USB 2.0 / I2C / SDIO / UART / PCM
F	28-35	Future Memory Interface (FMI)
G	39-46	Generic (Not used for M.2)***
H	43-50	Reserved for Future Use
J	47-54	Reserved for Future Use
K	51-58	Reserved for Future Use
L	55-62	Reserved for Future Use
M	59-66	PCIe x4 / SATA / SMBus

* Use ONLY when a double slot is being specified
** Label included in height dimension
*** Key G is intended for custom use. Devices with this key will not be M.2-compliant. Use at your own risk!
**** Insulating label allowed on connector-based designs

Figure 3. M.2 Naming Nomenclature

3.2. WWAN/SSD/Other Socket 2 Module Interface Signals

The socket 2 module interface signals are listed in Table 25.

Table 25. Socket 2 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Ground	+3.3 V (5 pins)	I	3.3 V source	3.3 V
	GND (11 pins)		Return current path	0 V
Communication Specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module. SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. 200 ppm.	3.3 V
	W_DISABLE1#	I	Active low, debounced signal when applied by the system it will disable radio operation on the add-in cards that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the card.	3.3 V
	W_DISABLE2#	I		1.8 V
	LED_1#	O	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.	3.3 V
	COEX[1..3]	I/O	Coexistence between WWAN and WiFi+BT on Socket 1	1.8 V
Supplemental Communication Specific Signals	FULL_CARD_POWER_OFF#	I	A single control to turn Off the WWAN solution. It is Active Low. This is only required on Tablet devices working directly off VBAT	1.8 V
	RESET#	I	A single control to Reset the WWAN solution. Active Low. This is needed when working in systems/platforms running directly off VBAT	1.8 V
	GPIO[0..11][1]	I/O	These signals form a block of programmable signals which can be used to perform various functions. See Table 33 for specific functions performed.	1.8 V
Supplemental Communication Specific Signal **continued…**	ANTCTL[0..3]	O	These signals are used for Antenna Control and should be routed to the appropriate Antenna Control Circuitry on the platform	1.8 V Nominal/ 2.8 V Max
	IPC_[0..7]	I/O	Pins to facilitate IPC signals exchanged between the host and the card. Functions are BTO/CTO.	1.8 V
	AUDIO[0..3]	I/O	Pins for the use of audio. Some examples of	1.8 V

[1] GPIO[9] may be defined as LED_1#, IPC_5, or SATA DAS/DSS. Host systems should use the CONFIG pins (see **Error! Reference source not found.**), or other mechanisms, to ensure that these signals are fully electrically compatible, or that no electrically incompatible signals are driven onto these pins of an M.2 module prior to discovery of the module type,

Interface	Signal Name	I/O	Function	Voltage
			audio interfaces are SLIMBus, I2S and PCM. Functions are BTO/CTO	
	WAKE_ON_WWAN#	O	Used to wake the platform by the WWAN device	1.8 V
	DPR	I	This signal is an input directly to the WWAN module from a suitable SAR sensor. The specific implementation will be determined by the module vendor and their customer	1.8 V
PCI-e	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1	I/O	PCIe TX/RX Differential signals defined by the PCIe 3.0 specification	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification	
	PERST#	I	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification	3.3 V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Substates	3.3 V
	PEWAKE#/OBFF	I/O	PCIe PME Wake. Open Drain with pull up on platform; Active Low	3.3 V
USB	USB D+, USB D-	I/O	USB Data ± Differential defined in the USB 2.0 Specification	
USB3.0	USB3.0-Rx+, USB3.0-Rx- USB3.0-Tx+, USB3.0-Tx-	I/O	USB3.0 TX/RX Differential signals defined by the USB 3.0 specification	
HSIC	HSIC-DATA, HSIC-STROBE	I/O	HSIC Data and Strobe signals as functionally defined by the HSIC Electrical Specification.	1.2 V
SSIC	SSIC-RxP, SSIC-RxN SSIC-TxP, SSIC-TxN	I/O	SSIC Tx/Rx Differential signals defined in the SSIC specification	
SATA	SATA-A+, SATA-A-/ SATA-B+, SATA-B-	I/O	Refer to Serial ATA rev. 3.1 Gold, or later	
	DEVSLP	I		
	DAS/DSS#	I/O		
SSD Specific Signals	Reserved for MFG_DATA/Reserved for MFG_CLOCK		Dedicated Data and Clock pins for SSD Manufacturing. Not to be connected to in the platform system	
	ALERT#	O	Alert notification to master; Open Drain with pull up on platform; Active Low	1.8 V
	SMB_CLK	I/O	SMBus clock; Open Drain with pull up on platform	1.8 V

Interface	Signal Name	I/O	Function	Voltage
	SMB_DATA	I/O	SMBus data; Open Drain with pull up on platform	1.8 V
User Identity Module (UIM) Signals	SIM_DETECT	I	This is an indication to the modem to detect the SIM insertion/removal. It is usually connected to the SIM reader SW pin and is card type dependent	1.8 V
	UIM_RESET	O	UIM reset signal. Compliant to the ISO/IEC 7816-3 specification (RST).	
	UIM_PWR	O	Power source for the UIM. Compliant to the ISO/IEC 7816-3 specification (VCC).	
	UIM_CLK	O	UIM clock signal. Compliant to the ISO/IEC 7816-3 specification (CLK).	
	UIM_DATA	I/O	UIM data signal. Compliant to the ISO/IEC 7816-3 specification (I/O).	
Module Configuration Pins	CONFIG[0..3]	O	These signals provide the means to indicate the specific configuration of the module as well as indication of whether a module is present or not. The meaning of each of the 16 possible decodes is shown in Table 27 These signals should either be grounded or left No Connect to build the decode required for a given module type. The host must provide a pull up resistor for each of these signals.	0 V (GND) /NC

Add following section after 3.2.11.1 (description of interface signals for Socket 2):

3.2.11.2 SMBus Interface

The SMBus interface supported in SSD Socket 2 is intended as optional side band management interface for SSD applications. SMBus is a three wire interface (ALERT# signal is optional) through which various system component chips can communicate with each other and with rest of the system. It is based on the principles of operation of I^2C. Refer to the SMBus specification for details of the operation.

3.2.11.2.1 ALERT# Signal

The ALERT# signal is intended to indicate to the platform/system that the SMBus device requires attention. This GPIO can be used to establish specific communication/signaling to the host from the device. This signal is Active Low.

3.2.11.2.2 SMB_DATA Signal

The SMB_DATA signal is used to transfer the data packets between the host and the device according to the SMBus protocol. The speed supported on this line depends on the host SMB_CLK signal speeds and the device processing capability.

3.2.11.2.3 SMB_CLK Signal

The SMB_CLK signal provides the clock signaling from the SMBus master to the SMBus slave device to be able to decode the data on the SMB_DATA line.

Modify table 31, and table 32 as shown below:

Table 31. Socket 2 SATA-based SSD Module Pinout

74	3.3V	CONFIG_2 = GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 = GND	69
	Module Key	N/C	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
		Module Key	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	N/C	55
54	N/C	N/C	53
52	N/C	GND	51
50	N/C	SATA-A+	49
48	N/C	SATA-A-	47
46	N/C	GND	45
44	ALERT# (O) ~~N/C~~	SATA-B-	43
42	SMB_DATA (I/O) ~~N/C~~	SATA-B+	41
40	SMB_CLK (I/O) ~~N/C~~	GND	39
38	DEVSLP (I)(0/3.3V)	N/C	37
36	N/C	N/C	35
34	N/C	GND	33
32	N/C	N/C	31
30	N/C	N/C	29
28	N/C	GND	27
26	N/C	N/C	25
24	N/C	N/C	23
22	N/C	CONFIG_0 = GND	21
20	N/C	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
		N/C	11
10	DAS/DSS# (I/O)	N/C	9
8	N/C	N/C	7
6	N/C	N/C	5
4	3.3V	GND	3
2	3.3V	CONFIG_3 = GND	1

Table 32. Socket 2 PCIe-based SSD Module Pinout

74	3.3V	CONFIG_2 = GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 = NC	69
	Module Key	N/C	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
		Module Key	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V)	GND	51
50	PERST# (I)(0/3.3V)	PERp0	49
48	N/C	PERn0	47
46	N/C	GND	45
44	ALERT# (O) ~~N/C~~	PETp0	43
42	SMB_DATA (I/O) ~~N/C~~	PETn0	41
40	SMB_CLK (I/O) ~~N/C~~	GND	39
38	N/C	PERp1	37
36	N/C	PERn1	35
34	N/C	GND	33
32	N/C	PETp1	31
30	N/C	PETn1	29
28	N/C	GND	27
26	N/C	N/C	25
24	N/C	N/C	23
22	N/C	CONFIG_0 = GND	21
20	N/C	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key		
10	LED1#	N/C	11
8	N/C	N/C	9
6	N/C	N/C	7
4	3.3V	N/C	5
2	3.3V	GND	3
		CONFIG_3 = GND	1

3.3 SSD Socket 3 Module Interface Signals

Table 33 contains a list of the Socket 3 module interface signals.

Table 33. Socket 3 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Grounds	+3.3 V (9 pins)	I	3.3 V source	3.3 V
	GND (14 pins)		Return current path	0 V
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the PCIe 3.0 specification	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification	
	PERST#	I	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification	3.3 V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Substates	3.3 V
	PEWAKE#/OBFF	I/O	PCIe PME Wake. Open Drain with pull up on platform; Active Low	3.3 V
SATA	SATA-A+, SATA-A-/SATA-B+, SATA-B-	I/O	Refer to Serial ATA rev. 3.1 Gold, or later	
	DEVSLP	I		
	DAS/DSS#	I/O		
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module. SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. 200 ppm.	3.3 V
	PEDET	O	Host I/F Indication; To be grounded for SATA, No Connect for PCIe	0 V/N C
	Reserved for MFG_DATA		Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation Pins should be left N/C in platform Socket	
	Reserved for MFG_CLOCK		Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation Pins should be left N/C in platform Socket	
	ALERT#	O	Alert notification to master; Open Drain with pull up on platform; Active Low	1.8 V
	SMB_CLK	I/O	SMBus clock; Open Drain with pull up on platform	1.8 V
	SMB_DATA	I/O	SMBus data; Open Drain with pull up on platform	1.8 V

Add following section after 3.3.4.3 (description of interface signals for Socket 3):

3.3.4.4 SMBus Interface

The SMBus interface supported in SSD Socket 3 is intended as optional side band management interface for SSD applications. See section 3.2.11.2, SMBus Interface, in this specification for more information.

Modify table 34, and table 35 as shown below:

3.3.5. Socket 3 Connector Pin-out Definitions

All pinout tables in this section are written from the module point of view when referencing signal directions**.**

Table 34 and Table 35 list the signal pin-outs for the module edge card connector. Table 34 lists the SATA based solution pinout. Table 35 lists the PCIe Multi-Lane based solution pinout.

Table 34. Socket 3 SATA-based Module Pinout

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	PEDET (GND-SATA)	69
	Module Key	N/C	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	N/C	55
54	N/C	N/C	53
52	N/C	GND	51
50	N/C	SATA-A+	49
48	N/C	SATA-A-	47
46	N/C	GND	45
44	ALERT# (O) ~~N/C~~	SATA-B-	43
42	SMB_DATA (I/O) ~~N/C~~	SATA-B+	41
40	SMB_CLK (I/O) ~~N/C~~	GND	39
38	DEVSLP (I)	N/C	37
36	N/C	N/C	35
34	N/C	GND	33
32	N/C	N/C	31
30	N/C	N/C	29
28	N/C	GND	27
26	N/C	N/C	25
24	N/C	N/C	23
22	N/C	GND	21
20	N/C	N/C	19
18	3.3V	N/C	17
16	3.3V	GND	15
14	3.3V	N/C	13
12	3.3V	N/C	11
10	DAS/DSS# (I/O)	GND	9
8	N/C	N/C	7
6	N/C	N/C	5
4	3.3V	GND	3
2	3.3V	GND	1

Table 35. Socket 3 PCIe-based Module Pinout

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	PEDET (NC-PCIe)	69
	Module Key	N/C	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V)	GND	51
50	PERST# (I)(0/3.3V)	PERp0	49
48	N/C	PERn0	47
46	N/C	GND	45
44	ALERT# (O) ~~N/C~~	PETp0	43
42	SMB_DATA (I/O) ~~N/C~~	PETn0	41
40	SMB_CLK (I/O) ~~N/C~~	GND	39
38	N/C	PERp1	37
36	N/C	PERn1	35
34	N/C	GND	33
32	N/C	PETp1	31
30	N/C	PETn1	29
28	N/C	GND	27
26	N/C	PERp2	25
24	N/C	PERn2	23
22	N/C	GND	21
20	N/C	PETp2	19
18	3.3V	PETn2	17
16	3.3V	GND	15
14	3.3V	PERp3	13
12	3.3V	PERn3	11
10	LED1# (O)	GND	9
8	N/C	PETp3	7
6	N/C	PETn3	5
4	3.3V	GND	3
2	3.3V	GND	1

4.2 1.8 V Logic Signal Requirements

The 1.8 V card logic levels for single-ended digital signals (SDIO, UART, PCM/I2S, SMBus etc.) are given in Table 37.

Table 37. DC Specification for 1.8 V Logic Signaling

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{DD18}	Supply Voltage		1.7	1.9	V	
V_{IH}	Input High Voltage		0.7*V_{DD18}	V_{DD18}+0.3	V	
V_{IL}	Input Low Voltage		-0.3	0.3*V_{DD18}	V	
V_{OH}	Output High Voltage	I_{OH} = -1mA V_{DD18} Min	V_{DD18}-0.45		V	
V_{OL}	Output Low Voltage	I_{OL} = 1mA V_{DD18} Min		0.45	V	
I_{IN}	Input Leakage Current	0 V to V_{DD18}	-10	+10	µA	
I_{LKG}	Output Leakage Current	0 V to V_{DD18}	-50	+50	µA	
C_{IN}	Input Pin Capacitance			10	pF	

Update SSD bullet in section 5.2.2 as shown below:

5.2.2. Socket 2 Pin-Out (Mechanical Key B) On Platform

- Socket 2 pinout is intended to support WWAN+GNSS, SSD, and Other types of Add-In solutions with the defined and configurable Host I/Fs.
- WWAN can make use of USB2.0, USB3.0, PCIe (up to two Lanes), or SSIC host I/Fs. The actual implemented I/F is identified through the Configuration pins state (1 of 16 states) on the Module side. LED1# and W_DISABLE1# are intended for use with the WWAN solution. There are additional WWAN and GNSS related pins including W_DISABLE2#, DPR, and WAKE_ON_WWAN#
- The UIM and SIM Detect pin are used in conjunction with a SIM device in support of the WWAN solution.
- The COEX and ANTCTL pins are placeholders for future expansion and definition of these functions.
- The GPIO0..11 pins are configurable with four different variants. These variants can be in support of the GNSS interface, second UIM/SIM, Audio interfaces, HSIC and IPC

sidebands. The exact definition is determined by which configuration was identified by decoding the four Configuration pins.

- The FULL_CARD_POWER_OFF# and the RESET# pins are unique and intended to be used when the WWAN solution is plugged into platforms that provide a direct connection to V_{BATT} (and not a regulated 3.3 V) such as Tablet platforms. They are not used in NB and Very thin notebooks type platforms that provide a regulated 3.3 V power rail. But the FULL_CARD_POWER_OFF# signals should be tied to the 3.3 V power rail on the NB/very thin platform.
- The SSD can make use of the PCIe two Lanes or overlaid SATA host I/F. The actual implemented I/F is identified through the CONFIG_1 pin state (1 or 0) in conjunction with the other three Configuration pin states that are all 0. DAS/DSS# (overlaid on the LED1#) and DEVSLP are intended for use with the SATA SSD solution. The SMBus interface may be used by host as side band management interface for SSD configuration, monitoring SSD status, and other diagnostic purposes.
- The SUSCLK pin provides a Slow Clock signal of 32 kHz to enable Low Power States.
- Pins labeled N/C should Not Be Connected.

Table 47 lists the pinout for Socket 2 (mechanical key B).

Table 47. Socket 2 Pinout Diagram (Mechanical Key B)

74	3.3V	CONFIG_2	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	CONFIG_1	69
66	SIM DETECT (O)	RESET# (O)(0/1.8V)	67
64	COEX1 (I/O)(0/1.8V)	ANTCTL3 (I)(0/1.8V)	65
62	COEX2(I/O)(0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
60	COEX3(I/O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
58	N/C	ANTCTL0 (I)(0/1.8V)	59
56	N/C	GND	57
54	PEWAKE# (I/O)(0/3.3V)	REFCLKp	55
52	CLKREQ# (I/O)(0/3.3V)	REFCLKn	53
50	PERST# (O)(0/3.3V)	GND	51
48	GPIO_4 (I/O)(0/1.8V*)	PETp0/SATA-A+	49
46	GPIO_3 (I/O)(0/1.8V*)	PETn0/SATA-A-	47
44	GPIO_2 (I/O)/ALERT# (I) (0/1.8V*)	GND	45
42	GPIO_1 (I/O)/SMB_DATA (I/O) (0/1.8V*)	PERp0/SATA-B-	43
40	GPIO_0 (I/O)/SMB_CLK (I/O) (0/1.8V*)	PERn0/SATA-B+	41
38	DEVSLP (O)	GND	39
36	UIM-PWR (I)	PETp1/USB3.0-Tx+/SSIC-TxP	37
34	UIM-DATA (I/O)	PETn1/USB3.0-Tx-/SSIC-TxN	35
32	UIM-CLK (I)	GND	33
30	UIM-RESET (I)	PERp1/USB3.0-Rx+/SSIC-RxP	31
28	GPIO_8 (I/O) (0/1.8V)	PERn1/USB3.0-Rx-/SSIC-RxN	29
26	GPIO_10 (I/O) (0/1.8V)	GND	27
24	GPIO_7 (I/O) (0/1.8V)	DPR (O) (0/1.8V)	25
22	GPIO_6 (I/O)(0/1.8V)	GPIO_11 (I/O) (0/1.8V)	23
20	GPIO_5 (I/O)(0/1.8V)	CONFIG_0	21
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
10	GPIO_9/DAS/DSS# (I/O)/LED1#(I)(0/3.3V)	GND	11
8	W_DISABLE1# (O)(0/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (O)(0/1.8V or 3.3V)	USB_D+	7
4	3.3V	GND	5
2	3.3V	GND	3
		CONFIG_3	1

5.3. SSD Socket; Socket 3 (Mechanical Key M)

This Socket pinout and key are only intended for SSD devices. The Host I/Fs supported are PCIe with up to four lanes or SATA. The state of the PEDET pin (69) will indicate to the platform which I/F of these two is actually connected.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
		N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	ALERT# (I) ~~N/C~~	PERp0/SATA-B-	43
42	SMB_DATA (I/O) ~~N/C~~	PERn0/SATA-B+	41
40	SMB_CLK (I/O) ~~N/C~~	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

- Although the pinout in Table 48 allocates four additional 3.3 V power pins, it is not intended to increase the current sinking capability of the Module. The intention is to

further reduce the IR drop of the power under extreme high current cases and increase the robustness of the SSD devices. The maximum power consumption of this socket remains as identified in section 3.3, *SSD Socket 3 System Interface Signals*. This Socket will also accept SSD devices that employ a Dual Module key on Module scheme. The SMBus interface available on Socket 3 may be used by host as side band management interface for SSD configuration, monitoring SSD status, and other diagnostic purposes.