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PCI-SIG® Publishes PCI Express® 4.0, Revision 0.9 Specification

New specification is feature complete, offers 16GT/s performance

News Highlights

- Key functional enhancements future-proof the evolution of the PCIe 4.0 architecture
- Unprecedented pre-publication testing offered for 16GT/s solutions

PCI-SIG Developers Conference 2017, Santa Clara, CA. – June 7, 2017 - PCI-SIG®, the organization responsible for the widely adopted PCI Express® (PCIe®) industry-standard input/output (I/O) technology, today announced the release of the PCI Express 4.0, Revision 0.9 Specification, supporting 16GT/s data rates, flexible lane width configurations and speeds for high-performance, low-power applications. The ubiquitous PCIe I/O architecture continues to outpace other interconnect technologies in terms of market share, capacity and bandwidth – doubling per-pin bandwidth while maintaining full backwards compatibility.

"I'm pleased to say that the PCIe 4.0 specification is feature complete and going through final IP review," said Al Yanes, PCI-SIG Chairman and President. "We extended the original timeline to adhere to our meticulous specification review process that has made PCIe technology so successful. We are confident that the PCIe architecture is sound for the foreseeable future and ready for the next generation of high-performance bandwidth."

Originating as the cornerstone for I/O connectivity in personal computing, the PCIe architecture has become the interconnect of choice for the expansive server and storage market. More recently, the PCIe architecture has also evolved into the backbone for the proliferating cloud ecosystem and served as the I/O attach point in mobile, IoT, networking and external I/O connectors.

The PCIe 4.0 architecture is poised to continue its evolution in delivering power-efficient performance. New functional enhancements include, extended tags and credits for service devices, reduced system latency, lane margining, superior RAS capabilities, scalability for added lanes and bandwidth, as well as improved I/O virtualization and platform integration.

"PCI technology has proven to be one of the most enduring and versatile I/O standards in the history of the computer industry. Its architects have successfully increased its performance and capabilities as they evolved its design from the original wide, parallel multi-point connective medium to the multi-lane, point-to-point arrangement we have today, while maintaining the APIs and semantics that preserve software investments. The release of the Revision 0.9 specification is a key milestone that demonstrates PCI Express is well positioned to meet the market's never-ending requirements for lower power and higher performance operation," observed Nathan Brookwood, research fellow at Insight 64.

As part of the I/O interconnect end-to-end solution, PCI-SIG offers a robust compliance program spanning across different form-factors and platforms to ensure plug-and-play capabilities with seamless interoperability. For the first time, PCI-SIG offered pre-publication compliance testing to its members leveraging the PCIe 4.0, Revision 0.9 specification.

"We've seen unprecedented interest in our PCIe 4.0 compliance testing and early adopters have already tested a dozen 16GT/s solutions," said Yanes.

To learn more about the PCIe 4.0, Rev. 0.9 specification, visit www.pcisig.com.

About PCI-SIG
PCI-SIG is the consortium that owns and manages PCI specifications as open industry standards. The organization defines industry standard I/O (input/output) specifications consistent with the needs of its members. Currently, PCI-SIG is comprised of over 700 industry-leading member companies. To join PCI-SIG, and for a list of the Board of Directors, visit www.pcisig.com.

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