PCI-SIG® DevCon 2019 Update

Al Yanes
President and Board Chair

PCI-SIG Snapshot

Organization that **defines the PCI Express® (PCIe®) I/O bus specifications and related form factors.**

800+ member companies located worldwide.

Creating specifications and mechanisms to **support compliance** and **interoperability.**

PCI-SIG member companies support the following industries:
- ○ Virtual reality
- ○ Automotive
- ○ Artificial intelligence
- ○ Telecommunications
- ○ Storage
- ○ Consumer
- ○ Mobile

**Board of Directors
2019 – 2020**

One Interconnect – Infinite Applications

Artificial Intelligence
- High-performance
- High-bandwidth

Automotive
- High-performance
- Reliability
- Availability
- Serviceability

Cloud
- Scalable architecture
- Increased performance
- Reduced TCO

Enterprise Servers
- Redundancy/failover
- Ubiquity
- Power savings

PC/Mobile/IoT
- Faster performance
- Power efficiency
- Low latency

Storage
- Faster data transfer
- Better user experience
- Ubiquity

PCI Express® 4.0 Specification & Status

Adoption is Well Under Way

- **Key Features:**
  - Delivers 16 GT/s
  - Maintains backward compatibility with PCIe 3.x, 2.x, and 1.x
  - Implements:
    - Extended tags and credits
    - Reduced system latency
    - Lane margining
  - Superior RAS capabilities
  - Scalability for added lanes and bandwidth
  - Improved I/O virtualization and platform integration
  - dB loss is 28dB

- **Compliance Status:**
  - PCI-SIG Launched Official FYI Testing for PCIe 4.0 in December 2018
  - Formal Compliance testing targeted for Q3 2019
- **Adoption:**
  - Numerous vendors with 16GT/s PHYs and controllers in silicon
  - Test equipment from multiple vendors available
  - Several member companies have publicly announced & exhibited PCIe 4.0 products

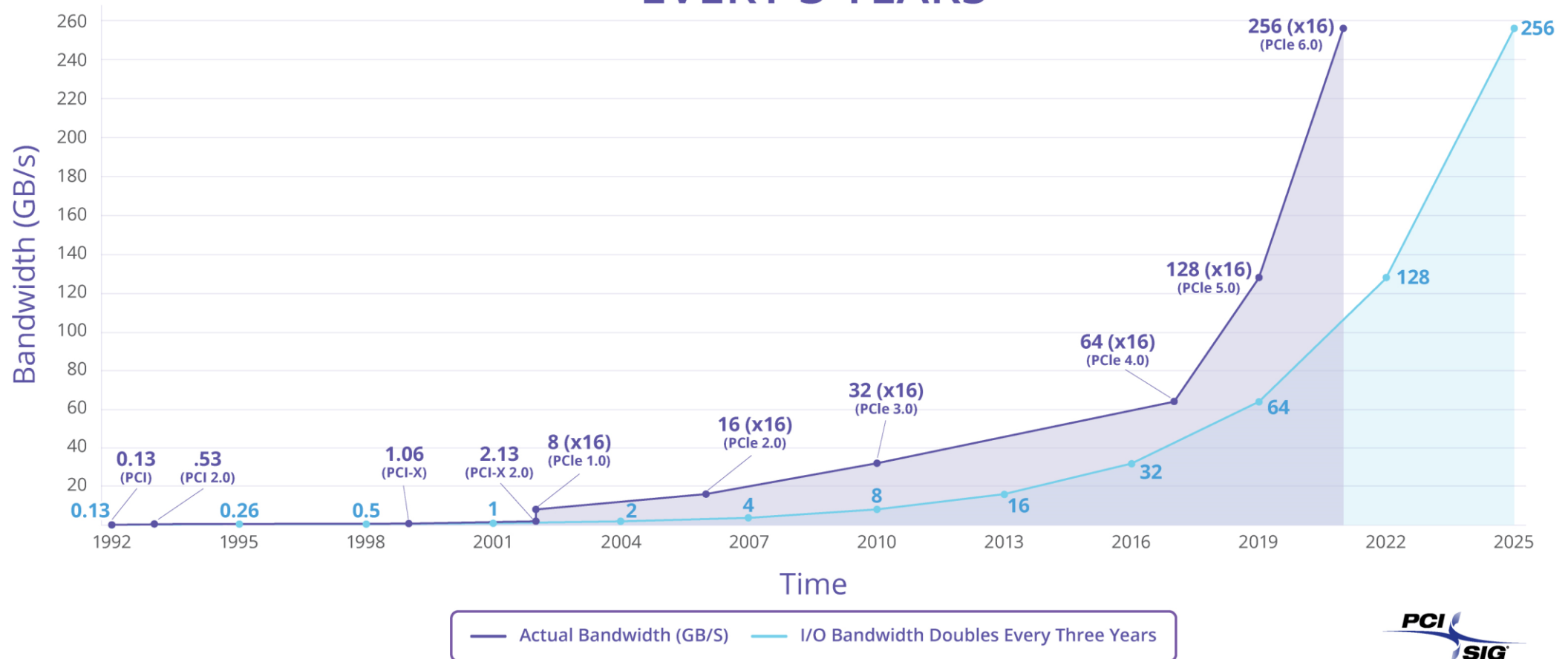# PCI Express® 5.0 Specification & Status

Published in May 2019

- **Key Features:**
  - Delivers 32 GT/s
  - Maintains backward compatibility with PCIe 4.0, 3.x, 2.x, and 1.x
  - dB loss is 36dB
  - Electrical changes to improve signal integrity and mechanical performance of connectors

- **Compliance Status:**
  - PCIe 5.0 compliance testing is under development
- **Adoption**
  - Several member companies have publicly announced and are showcasing PCIe 5.0 solutions
  - Adoption expected to grow in the next 18-24 months due to demand from high performance applications

I/O BANDWIDTH DOUBLES EVERY 3 YEARS

PCI Express® 6.0 Specification Details

Targeting completion in 2021; Designed to meet the evolving capacity needs of industry

- **Key Features:**
  - Doubles bandwidth to 64 GT/s (PCIe 6.0) from 32 GT/s (PCIe 5.0)
  - Implements PAM4 signaling (PCIe 6.0) rather than NRZ (PCIe 5.0)
    - Pulse Amplitude Modulation (PAM) allows PCIe 6.0 technology to pack more bits into the same amount of time on a serial channel
  - Includes low-latency Forward Error Correction (FEC) with additional mechanisms to improve bandwidth efficiency
  - Maintains backward compatibility with all previous generations of PCIe technology
  - Delivers similar channel reach as PCIe 5.0
  - More than two dozen member companies of the PCI-SIG Electrical Work Group attended a Face-to-Face Meeting in May

PCIe Technology Showcase

Summary

o PCIe® technology delivers one interconnect for infinite applications

  • PCIe 4.0 formal compliance testing targeted for August 2019 and adoption is accelerating and the ecosystem is complete and robust

  • PCIe 5.0 specification published in May 2019 and compliance testing is under development

  • PCIe 6.0 doubles bandwidth again to 64 GT/s; targeted for publication in 2021

o Meets performance and user requirements for current and future applications in performance demanding markets like IoT, AI/ML and automotive

o PCI-SIG continues to maintain its leadership position in delivering high-performance, low power I/O

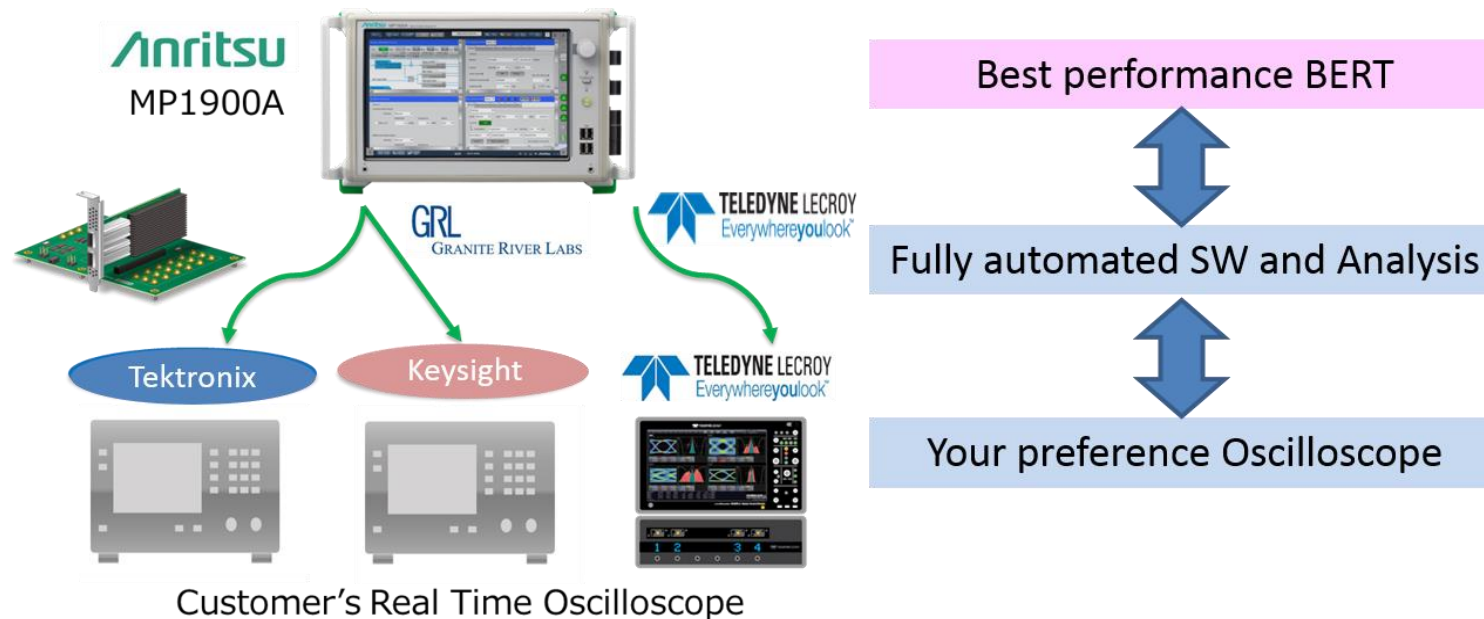# Engage with PCI-SIG on Social Media

@PCI_SIG

https://www.linkedin.com/company/pcisig/

PCI-SIG

PCI-SIG 2010 DevCon Sponsors

Combination of best performance BERT MP1900A and your preference oscilloscope

Shortening your test time and reducing your investment cost

- ➢ Supports combination with LeCroy/Tektronix/Keysight Real Time Oscilloscope
- ➢ Automated Rx CEM and Base tests : Calibration, Link EQ and Automated Tx test
- ➢ Protocol Aware : Link training/Equalization and LTSSM analysis
- ➢ Excellent expandable 32G multi-channel BERT for PCIe-G1 to G6


Anritsu Booth #615

For more information, please go to: https://www.anritsu.com/en-US/test-measurement/solutions/hssd/index?prod-page=mp1900a

Cadence Design Systems, Inc.

Join us to learn about our latest developments in PCI Express® (PCIe®) technology and see demonstrations of our verification IP, PHY, and controllers for PCIe Gen 5.

In our booth (#7) we will demonstrate:

o High-Performance SerDes PHY for PCIe

o PCIe Gen 5 Controller

o PCIe 5.0 Compliance with TripleCheck™ technology
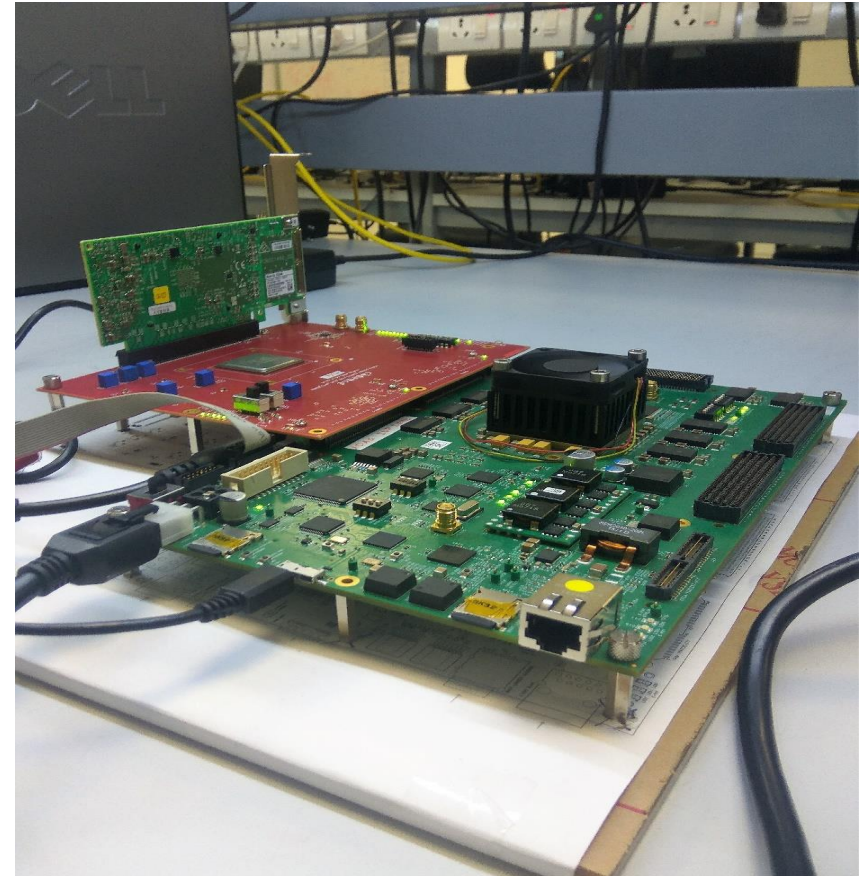
Cadence PCIe 4.0 Lane Margining Interop Demo

Keysight Technology

PCI Express® Physical Layer Test Solutions to 64GT/s   **Booth #9**

Featuring:

UXR-Series Oscilloscopes
- Models from 13GHz-110GHz
- Best in class Sample Rates
- 10bit ADC
- Best signal integrity
- Upgradeable bandwidth

Physical layer – interconnect design

ADS design software

86100D DCA-X/TDR

N5227B PNA w/ PLTS

Verify PCIe 5.0 Compliant Channels
Verify Return Loss Compliance
Capture break-out channel S-Params

Physical layer-transmitter test

UXR-Series, Z-Series Real-Time Oscilloscopes

D9050PCIC PCI Express 5.0 TX Electrical compliance software

86100CU-400 PLL and Jitter Spectrum Measurement SW

DSA UXR-Series & Z-Series Real-Time Oscilloscopes
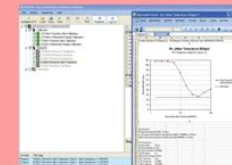
Physical layer-receiver test

M8046A J-BERT High Performance BERT w/ integrated CDR + M80454A Interference Source

M8049A-1 Substitute PCIe 5 BASE Channel board

N5991PB5A PCIe 5.0 32GT/s RX Test software

Automated RX Test software
- Accurate, Efficient
- Comprehensive RX Testing

Featuring:

M8040A 64GBaud BERT
- RX test 400G, PCIe
- Upgrade path Gen5-Gen6
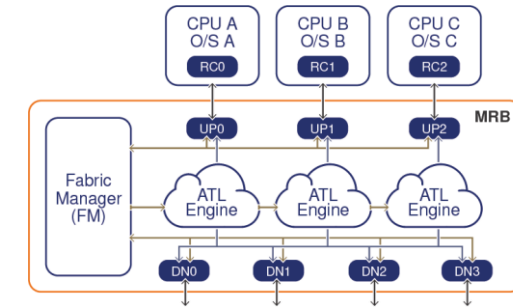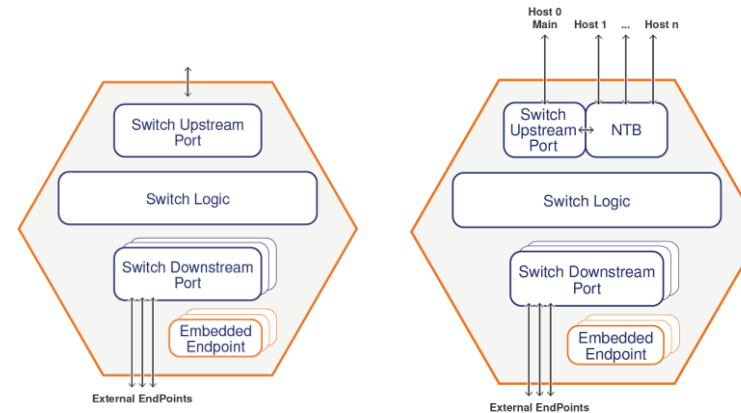- Most complete test automation
- NRZ and PAM4 capable

PLDA (Booth #1) – What's New

Enabling PCI Express® fabric composition with comprehensive PCIe® 5.0 Switch IP portfolio

o   PCIe Fanout Switch

o   PCIe Switch with NTB

o   PCIe Multi-Root Bridge

Enabling PCIe 4.0 add-in card bring-up and debug with Inspector interposer

o   Link and interface monitoring/diagnostic

o   Traffic/performance analysis

o   Interface testing (width/speed change, low power, loopback, equalization, etc.)

* "Featured at PCI-SIG® Compliance workshops for PCIe 4.0 FYI host interoperability tests - since 2017"

Synopsys

Complete DesignWare® IP Solutions for PCI Express® (PCIe®)
Lowest-Risk, Silicon-Proven, Shipping in Volume

SYNOPSYS®

Customer Success

- Dozens of early PCIe 5.0 adopters, several successful tape-outs, multiple designs in silicon
- In > 160 PCIe 4.0 designs
- Licensed > 1700 times, in billions of units
- E.g.: Habana Labs first-pass silicon success for AI processor SoC

Ecosystem Success

- Successful PCIe 4.0 & 5.0 interoperability with ecosystem: Teledyne LeCroy, Anritsu, Mellanox, Samtec, Keysight, Tektronix, Intel, Marvell
- World's first & most interoperated PCIe 4.0 host
- Most interoperability testing & PCI-SIG certifications
- On PCI-SIG board, developing and driving adoption of spec

Product Success

- Controller, PHY, verification IP
- Support for full 5.0, 4.0,3.1, 2.1, 1.1 specs
- Optimizable for highest performance, lowest power & latency
- Silicon-proven 32GT/s PHYs in FinFET processes through 7-nm
- ASIL B Ready ISO 26262 certified IP

Visit Synopsys Booth #8 to See DesignWare IP for PCIe 5.0 Demos

1. End-to-End System with DesignWare IP for PCIe 5.0 spec at 32GT/s
2. PCIe 5.0 Interoperability Success with DesignWare IP and Intel Test Chip
3. Best PPA with DesignWare PHY IP for PCIe 5.0 Rev. 1.0 spec @ 32GT/s

4. Accelerate Verification Closure with PCIe 5.0 IP/VIP and Test Suites
5. PCIe 5.0 Interoperability Success with DesignWare IP and Marvell Test Chip

Also see Synopsys IP demos in our partner booths

Customers Achieving Silicon Success with DesignWare IP for PCI Express

habana · AMD · STARBLAZE · KYOCERA Document Solutions · SOLARFLARE® · GUC · .....

Teledyne LeCroy – Booth #14

New Protocol Analyzer

- Summit T54 PCI Express® 5.0 Protocol Analyzer
- New Interposers and Adapters
    - PCIe® 4.0 x4 EDSSF Interposer
    - PCIe 4.0 EDSFF Adapters for E1.S, E1.L, and E3 devices
    - PCIe 4.0 U.2/ U.3 Interposer
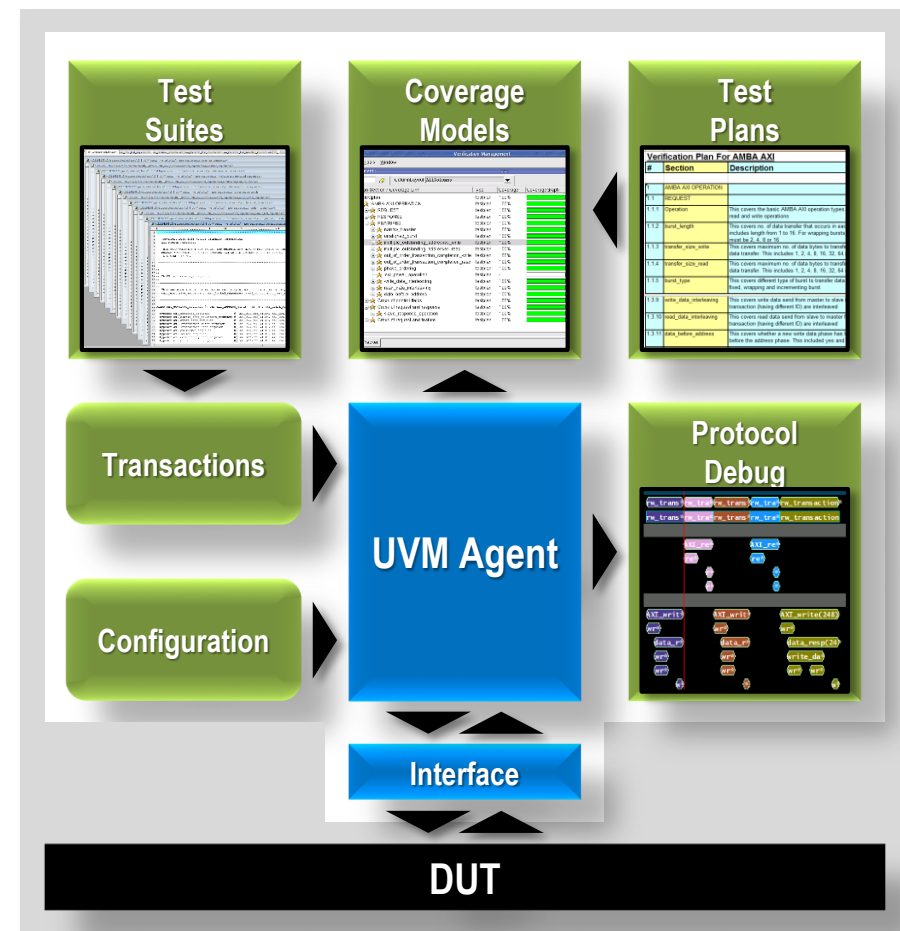   - PCIe 4.0 M.2 Interposer

Mentor, A Siemens Business BOOTH #3

o **Industry leading Verification IP for PCI Express® & NVMe**
  - Complete support for PCIe® 5.0 specification, NVMe 1.3c with advanced verification capabilities

o **Part of a complete Verification IP solution**
  - Protocols: AMBA®, Display, Ethernet, MIPI®, PCIe, USB, etc
  - Memory models: DDR family, LPDDR family, DIMM, HBM, WideIO, SD, ONFI, etc

o **Architected for rapid productivity**
  - Standards based SV UVM support
  - EZ-VIP™ API
  - Quick starter kits for commonly used IP

o **Complete protocol assurance**
  - Comprehensive sequence library, checking & coverage

o **High performance verification**
  - Optimized simulation models
  - Synthesizable transactors for testbench acceleration
  - Virtual models for Acceleration and ICE and completely virtual environment in emulation

o **Presentation:**
  - PCIe 5.0 Specification Precoding Requirements and Verification Challenges
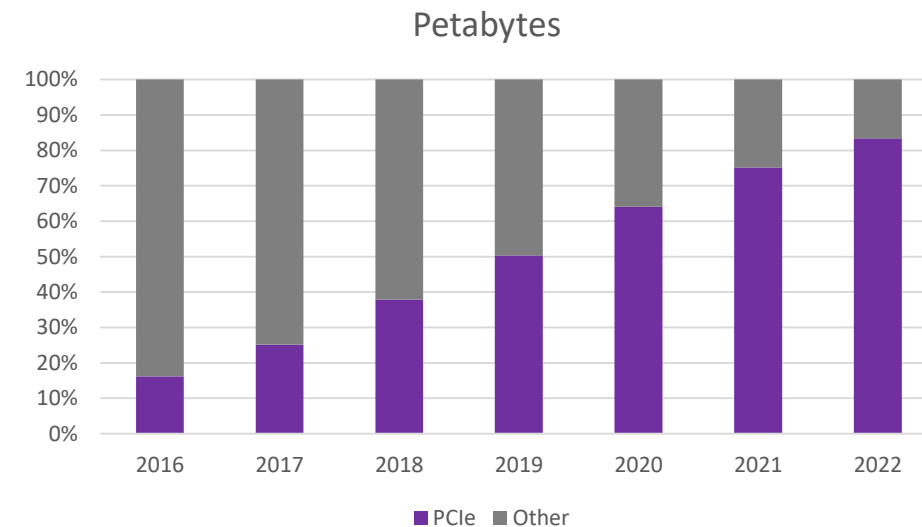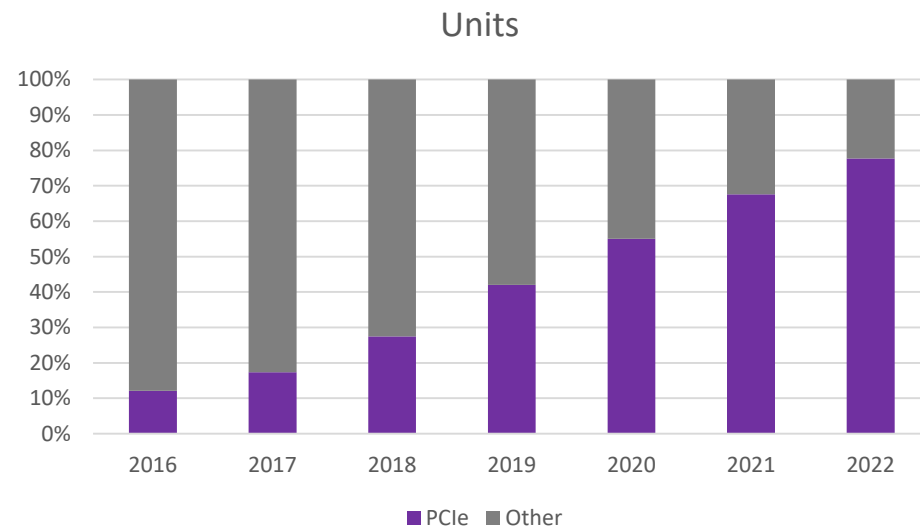 - Presenter: Gyanaranjan Khuntia
  - Wednesday @ 2:30pm

Back-Up Slides

NVM Express™ Driving PCIe® SSDs in the Data Center

- Data explosion is driving SSD adoption
  - SSD market CAGR of 14.8% during 2016-2021 *Source*: IDC
  - PCIe SSD market to surpass a CAGR of 33% during 2016-2020 *Source*: Technavio
- PCIe adoption is accelerating

Source: SSD Insights Q1/18, Forward Insights

Design for a Range of Objectives

Low Power	Server Performance	High Performance
M.2	**U.2**	**CEM Add-in-card**
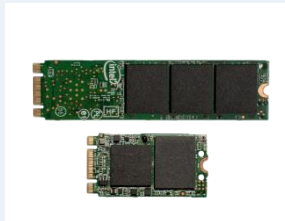
PCIe
Form Factors

42, 80, and 110mm lengths, smallest footprint of PCIe connector form factors, use for boot, for max storage density, for PXI/AXIe ecosystem

2.5in makes up the majority of SSDs sold today because of ease of deployment, hotplug, serviceability, and small form factor
Single-Port x4 or Dual-Port x2

Add-in-card (AIC) has maximum system compatibility with existing servers and most reliable compliance program. Higher power envelope, and options for height and length
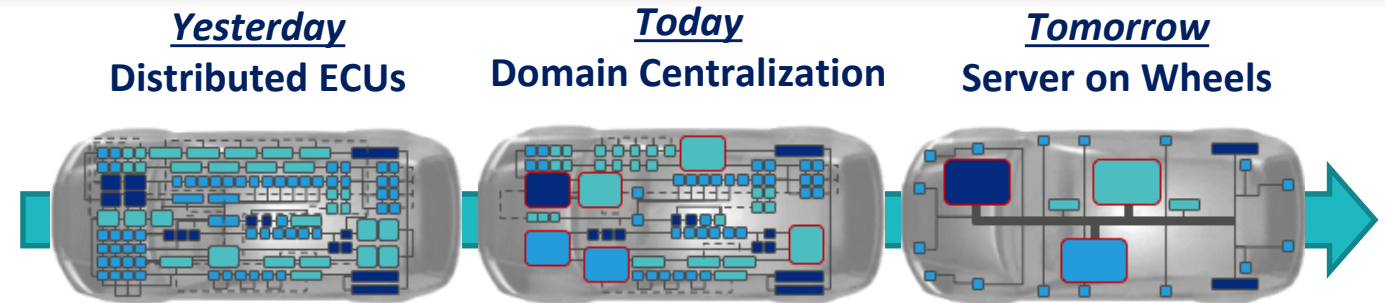
PCIe® in Automotive

- Distributed ECUs with point-to-point links transitioning to centralized compute architectures
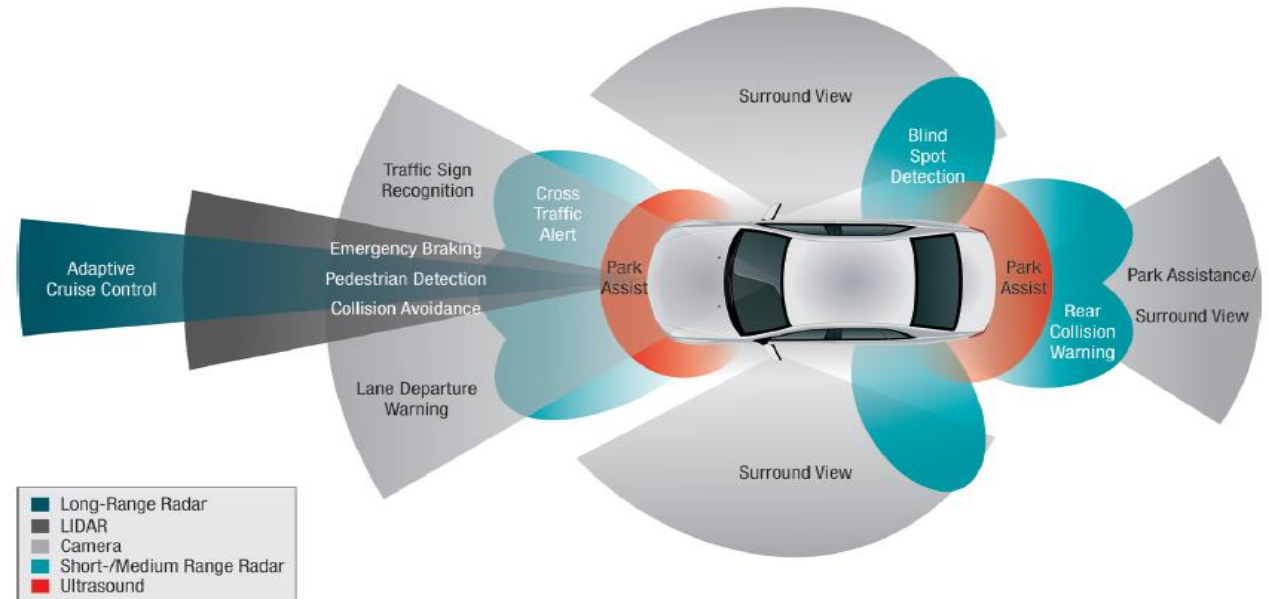
- Exploding bandwidth requirement
  - Video resolution: From 720p to 4K+
  - Displays: From 3 to 8+
  - Sensor nodes: From 4 to 12+
  - RADAR (RAdio Detection and Ranging) / LIDAR (LIght Detection And Ranging)

- PCIe as Multi-Gigabit connectivity bus
  - SoC-to-SoC : ADAS (Advanced Driver Assistance Systems), IVI (In-vehicle Infotainment)
  - SoC-to-sensor, SoC-to-I/O connectivity

Yesterday
Distributed ECUs

Today
Domain Centralization

Tomorrow
Server on Wheels

Source: Delphi, Astera Labs

Surround View
Blind Spot Detection
Traffic Sign Recognition
Cross Traffic Alert
Emergency Braking
Pedestrian Detection
Collision Avoidance
Adaptive Cruise Control
Park Assist
Park Assist
Park Assistance/ Surround View
Rear Collision Warning
Lane Departure Warning
Surround View

- Long-Range Radar
- LIDAR
- Camera
- Short-/Medium Range Radar
- Ultrasound

Source: TI Whitepaper Vision Enabled Automotive Technologies

PCIe® in IoT

o **Data deluge from IoT driving intelligence and processing to the *Edge***

  - 45% of IoT data processed at edge* by 2020

o **Industrial PCs or COM (Computer-on-Module) Express module form-factor**

  - COM express Type 7 : 32 lanes, PCIe Gen 3.0
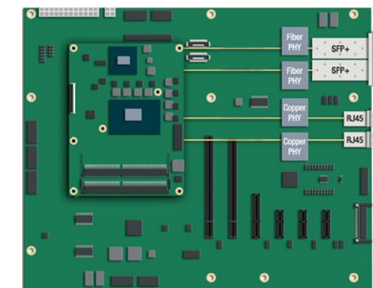 - Proposed COM-HD : 64 lanes, PCIe Gen 5.0

o **PCIe as Multi-Gigabit connectivity bus**

  - IO expansion for CPUs
  - Interconnect between data processors (CPU/FPGA/Accelerators/SoC)
  - Storage (NVMe) connectivity

*IDC

Source: : ESG Research 2016
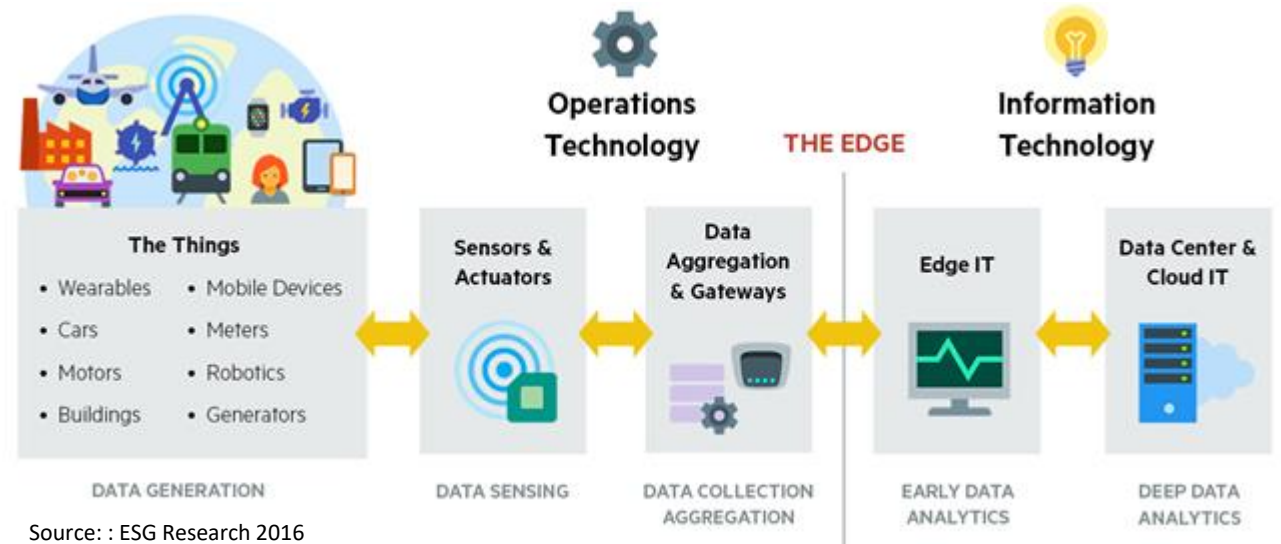
Industrial PCs

COM (Computer-on-Module) Express

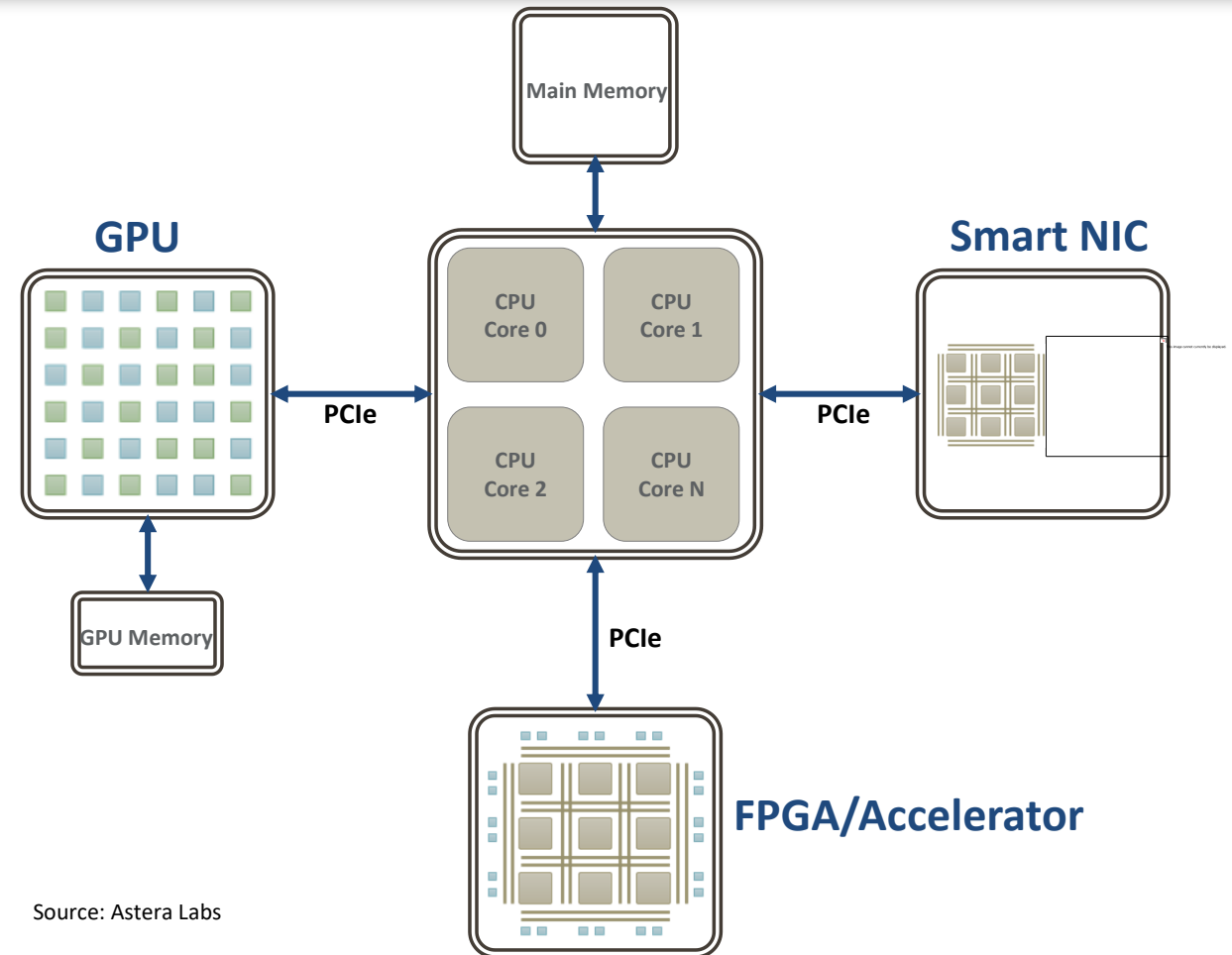o **Computation-intensive workloads demand data-centric system design**
  - Big data analytics growing at 11.9% CAGR[*]
  - AI and ML key drivers

o **Heterogeneous computing and workload-optimized platforms redefining connectivity backbone in servers**
  - PCIe 5.0 delivers 32 GT/sec bandwidth
  - Alternate protocol support included in PCIe 5.0

o **PCIe as Multi-Gigabit connectivity bus**
  - Processor-to-Processor interconnect
  - Processor I/O expansion
  - Storage (NVMe) connectivity

*[IDC](#)

Main Memory

GPU

Smart NIC

CPU Core 0
CPU Core 1
PCIe
CPU Core 2
CPU Core N

PCIe

GPU Memory

PCIe

FPGA/Accelerator

Source: Astera Labs