



# PCI-SIG® DevCon 2017 UPDATE

**AL YANES**  
President and Chairman

# PCI-SIG® Snapshot



Organization that **defines the PCI Express I/O bus specifications and related form factors.**

- **730+** member companies located worldwide

Creating specifications and mechanisms to **support compliance and interoperability.**

- 
- Australia
  - Austria
  - Belgium
  - Brazil
  - Bulgaria
  - Canada
  - China
  - Czech Republic
  - Denmark
  - Finland
  - France
  - Germany
  - Hong Kong
  - Hungary
  - India
  - Ireland
  - Israel
  - Italy
  - Japan
  - Malaysia
  - Norway
  - Russia
  - Singapore
  - Slovak Republic
  - South Korea
  - Sri Lanka
  - Sweden
  - Switzerland
  - Taiwan
  - The Netherlands
  - Turkey
  - United Kingdom
  - United States

## BOARD OF DIRECTORS 2017-2018



PCI-SIG continues its solid reputation of delivering **low cost, high-performance, low-power specifications** for **multiple applications and markets.**

- **PCI Express 4.0 Specification – (16GT/s)**
  - Feature complete Revision 0.9 released for final IP review
  - Includes new performance enhancements
  - Maintains position as the interconnect of choice for the expansive storage market and the backbone for the fast growing cloud ecosystem

- **PCIe 4.0 Key Functional Enhancements**

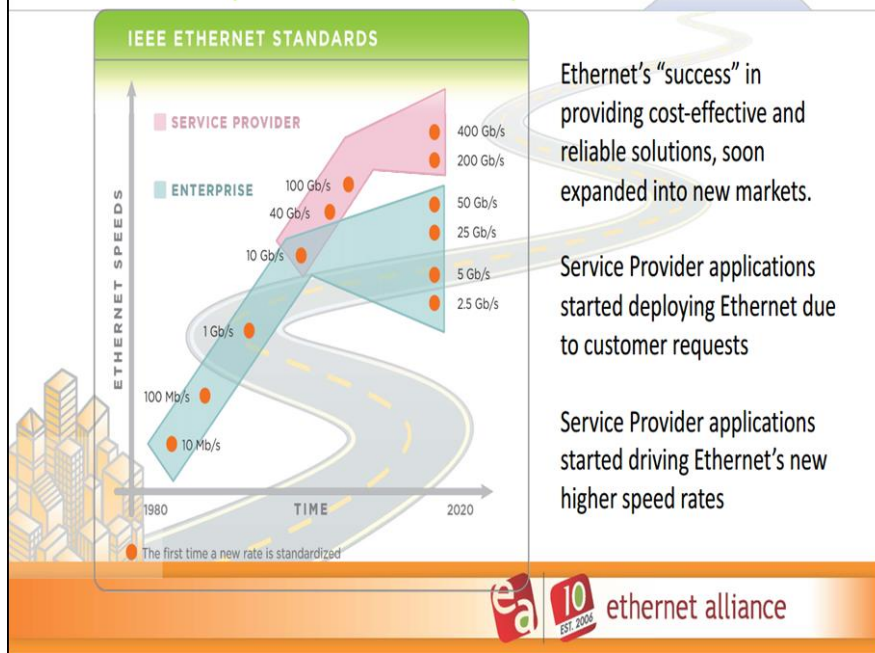
- Lane Margining at the Receiver
  - Allows the system to determine how close to “the edge” each lane is operating under real conditions
- Expanded Tag and Credits
  - Allows both tags and credits to expand to service devices well into the foreseeable future

- **PCIe 4.0 Adoption**

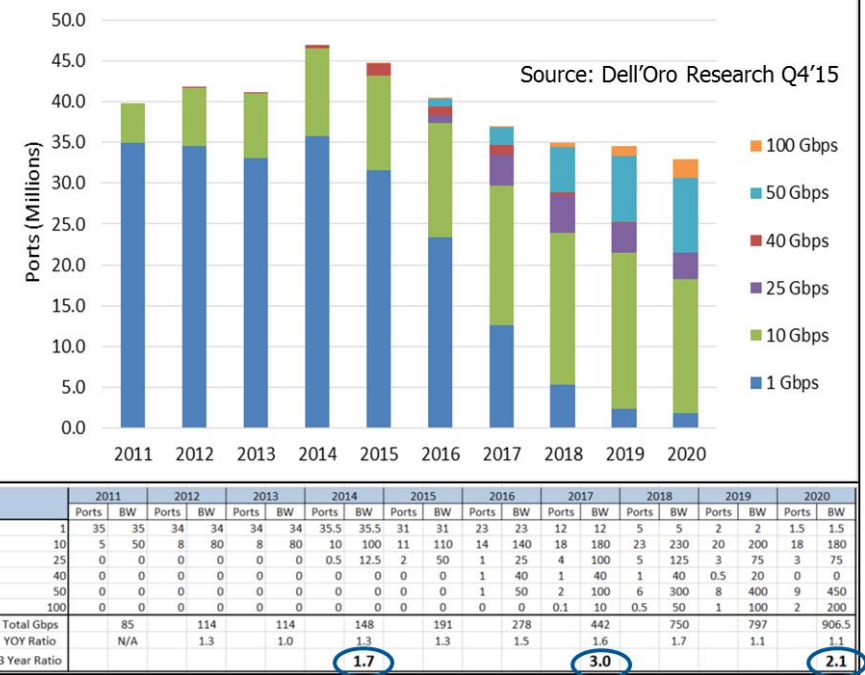
- Numerous vendors confirmed with 16GT/s PHYs in silicon
- Major IP vendors offering 16GT/s controllers
- Dozen 16GT/s solutions at a recent PCI-SIG Compliance Workshop
- Several DevCon exhibitors with 16GT/s demos

# Ethernet Evolution

## Market Adoption of Ethernet Speeds



## Controller and Adapter Market Port Forecast



- **PCI Express 5.0 Specification with 32GT/s Bandwidth**
  - Revision 0.3 has already been delivered to PCI-SIG members
  - Ideal for:
    - Applications such as artificial intelligence, machine learning, gaming, visual computing, storage and networking
    - High-end networking solutions (i.e. 400Gb Ethernet and dual 200Gb/s InfiniBand solutions)
    - Accelerator and GPU attachments for high-bandwidth solutions
    - Constricted form factor applications that cannot increase width and need higher frequency to achieve performance

# PCIe 5.0 Delivering 32GT/s



- ✓ **Supports 400Gb Ethernet Solutions**

- 400Gb = 50GB
- 50GB in both directions

- ✓ **Full Duplex**

- 128/130 bit encoding with 1.5% overhead
- x16 ~64GB/s sufficient to support 400Gb Ethernet solutions (64GB > 50 GB)
- Total Full Duplex = ~128GB

- CEM connector targeted to be backwards compatible for add-in cards
- **Targeted Release in 2019**

	RAW BIT RATE	LINK BW	BW/ LANE/WAY	TOTAL BW X16
PCIe 1.x	2.5GT/s	2Gb/s	250MB/s	8GB/s
PCIe 2.x	5.0GT/s	4Gb/s	500MB/s	16GB/s
PCIe 3.x	8.0GT/s	8Gb/s	~1GB/s	~32GB/s
PCIe 4.0	16GT/s	16Gb/s	~2GB/s	~64GB/s
PCIe 5.0	32GT/s	32Gb/s	~4GB/s	~128GB/s

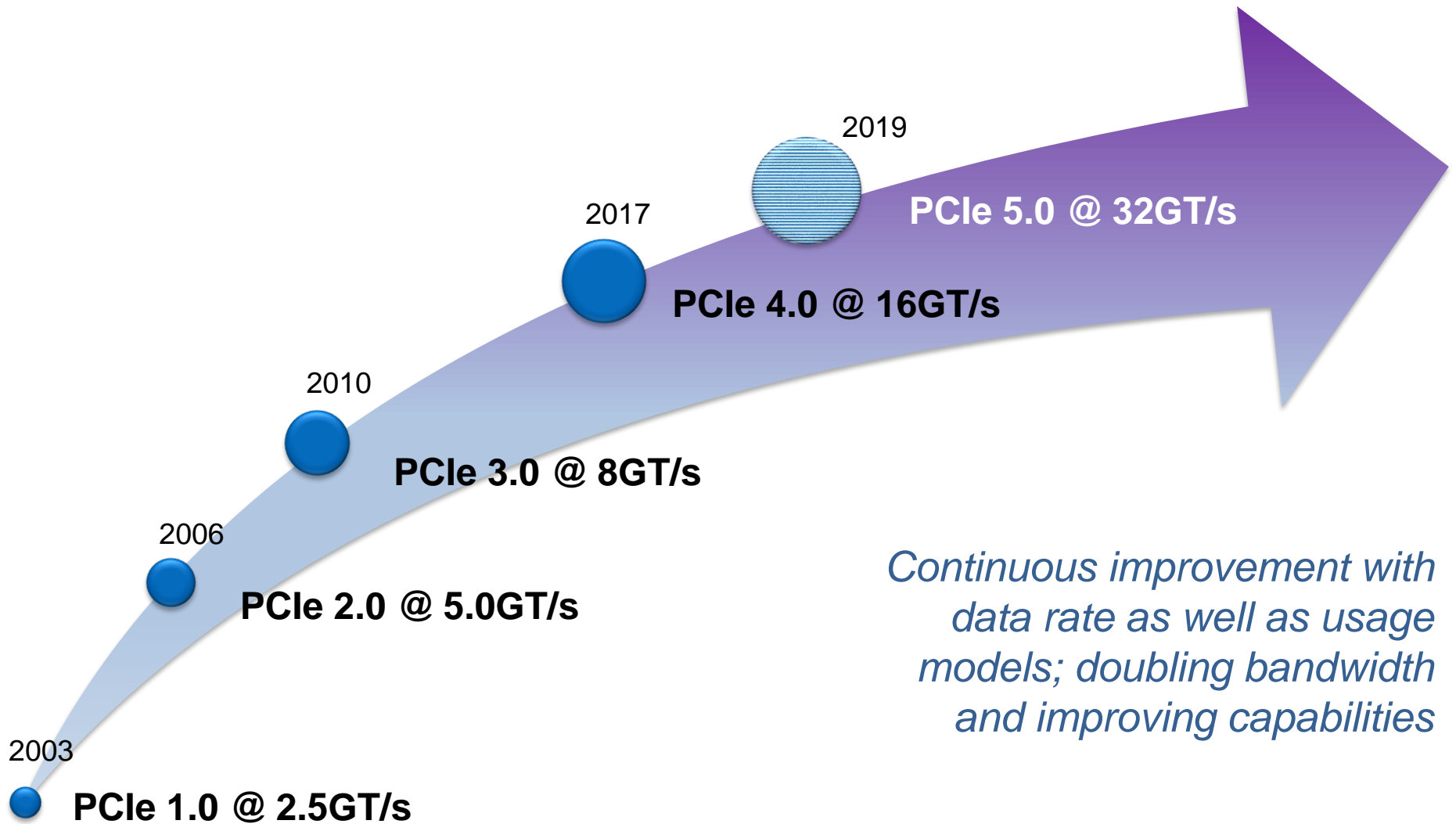
# PCIe Bandwidth & Frequency



Year	Bandwidth	Frequency/Speed
1992	133MB/s (32 bit simplex)	33 Mhz (PCI)
1993	533MB/s (64 bit simplex)	66 Mhz (PCI 2.0)
1999	1.06GB/s (64 bit simplex)	133 Mhz (PCI-X)
2002	2.13GB/s (64 bit simplex)	266 Mhz (PCI-X 2.0)
2002	8GB/s (x16 duplex)	2.5 GHz (PCIe 1.x)
2006	16GB/s (x16 duplex)	5.0 GHz (PCIe 2.x)
2010	32GB/s (x16 duplex)	8.0 GHz (PCIe 3.x)
2017	64GB/s (x16 duplex)	16.0 GHz (PCIe 4.0)
2019	128GB/s (x16 duplex)	32.0 GHz (PCIe 5.0)



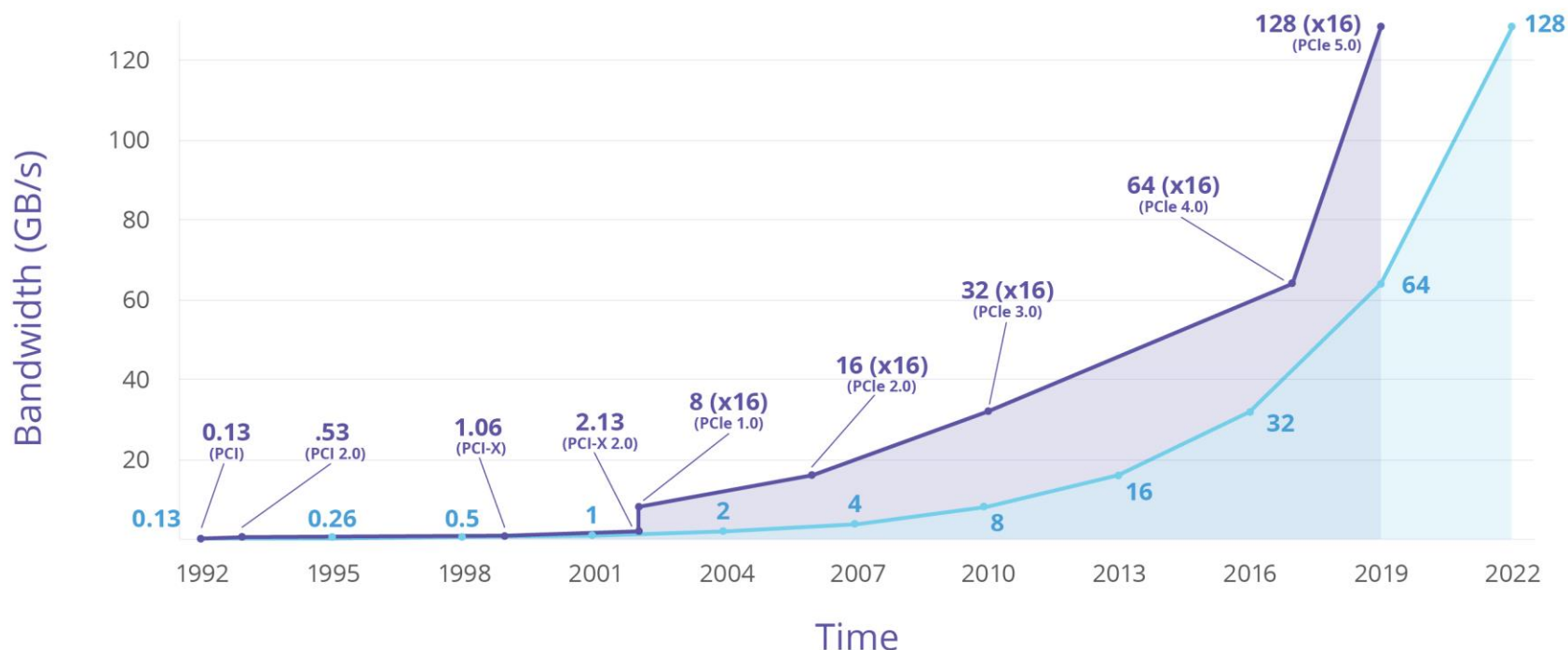
# PCIe® Roadmap



# PCI-SIG History



## I/O BANDWIDTH DOUBLES Every 3 Years



PCI-SIG BANDWIDTH 1992-2019

— Actual Bandwidth (GB/S)    — I/O Bandwidth Doubles Every Three Years



2017 PCI-SIG® DevCon  
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Companies

# Company Presenters



## Platinum

**cādence**<sup>™</sup>

**Booth 3** – Sachin Dhingra, Senior Product Marketing Manager

**SYNOPSYS**<sup>®</sup>  
*Silicon to Software*<sup>™</sup>

**Booth 2** – Scott Knowlton, Senior Product Marketing Manager



**Booth 4** – John Wiedemeier, Senior Product Marketing Manager

## Gold



**Booth 8** – Rick Eads, Principal PCI Express Solutions Planner



**Booth 9** – Jason Polychronopoulos, Mgr. Verification IP Solutions



**Booth 12** – Stephane Hauradou, Co-founder



**Booth 5** – Rob Venzina, Senior Application Engineer

## Exhibitor



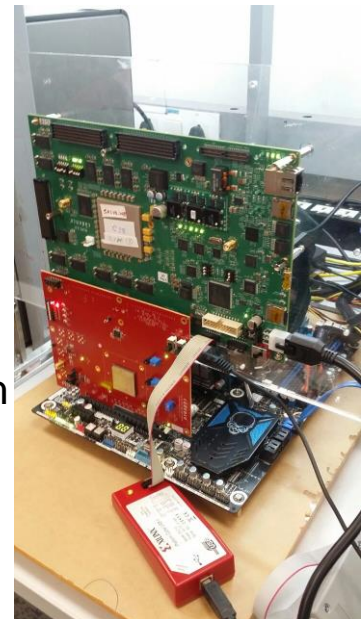
**Booth 1** – Kay Annamalai, Senior Marketing Director



**Booth 7** – Gursimranjit Singh, Senior Systems Engineer

## *Cadence IP Solution for PCI Express® 4.0 Architecture*

- **Complete, integrated, pre-verified Cadence® IP solution**
  - High-performance, low-latency controller
  - Multi-link, multi-protocol PHY
  - Verification IP with extensive test suite and debug utilities
- **Application-optimized solutions**
  - Enterprise
    - Multi-packet design allows >95% link utilization
    - Flexible PHY configurations to maximize utilization of bandwidth
  - Mobile
    - Lowest active power with L0 state power
    - Lowest area and flexible placement for smallest overall SoC
  - Automotive
    - First PCIe® 4.0 PHY audited by SGS-TÜV and deemed ASIL-B ready
    - Solution supports comprehensive automotive safety features
- **Technical presentation**
  - *Challenges and Techniques for Implementing Lane Margining – Gopi K, Architect*



## Finish First with DesignWare IP Solutions for PCIe® Technology

*Validated in Over 1500 Designs & Shipping Billions of Units*



### ○ PCIe® 4.0 Architecture Ready

- PHYs, controllers, verification IP & IP prototyping kits conforming to the 0.7 revision of the PCIe 4.0 specification
- Validated PCIe 4.0 testing and interoperability with ecosystem partners: Mellanox, Teledyne LeCroy and more
  - Demos: Full system PCIe 4.0 interoperability @ 16GT/s with Mellanox; DesignWare® PHY IP; verification IP

News

### ○ Automotive Ready

- Certified PHY and controller IP solutions meet automotive functional safety, reliability and temperature requirements
  - Demo: Reliability, debug, error injection features

News

In position to lead the industry in powering next-gen products beyond 16GT/s

**SYNOPSYS**  
Silicon to Software™

Booth #2

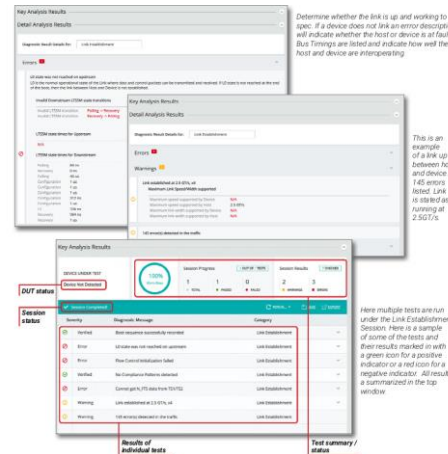
## PCIe® 4.0 Protocol Test Equipment



Summit T416  
Protocol Analyzer

Summit Z416  
Protocol Exerciser

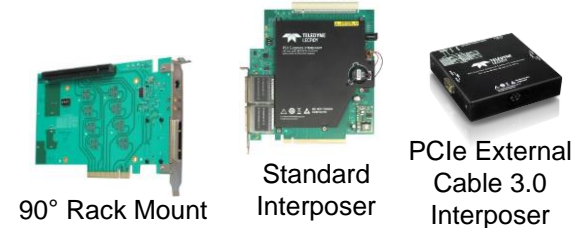
## Link Expert



## Makes Protocol Analysis Easy



## PCIe technology with SMBus Support



90° Rack Mount



Standard Interposer



PCIe External Cable 3.0 Interposer



M.2 Interposer



U.2(SFF-8639) 5"



SFF-8639 Dual12" Interposer

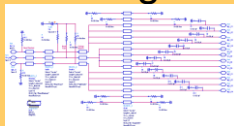


# Keysight Technologies



## PCI Express® 4.0 Technology – Keysight Total Solution

### Physical layer – interconnect design



ADS design software



86100D DCA-X/TDR



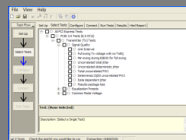
E5071C ENA option TDR

Verify PCIe 4.0 Compliant  
Channels  
Verify Return Loss Compliance

### Physical layer- transmitter test



V-Series, Z-Series Real-  
Time Oscilloscopes



N5393F PCI Express 4.0  
TX Electrical compliance  
software



86100CU-400 PLL and  
Jitter Spectrum  
Measurement SW

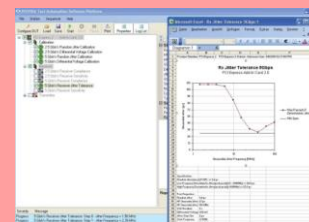
DSA V-series & Z-Series  
Real-Time Oscilloscopes

### Physical layer- receiver test



M8020A J-BERT High  
Performance, Protocol  
Aware BERT

N5990A automated  
compliance and device  
characterization test  
software



Automated RX Test software  
- Accurate, Efficient  
- Comprehensive RX Testing

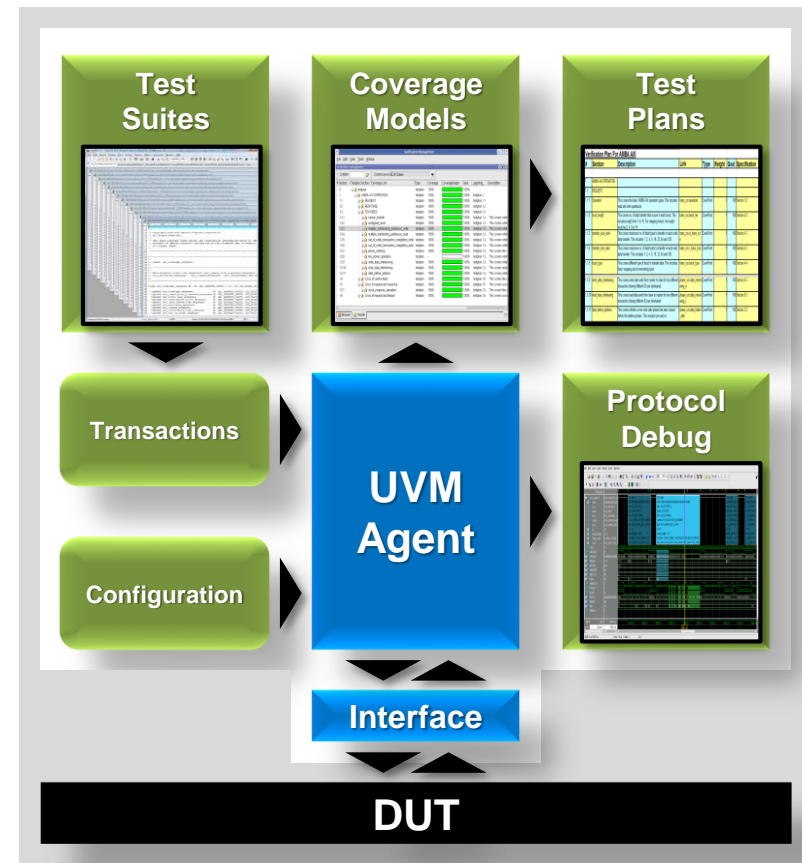
PCIe 4.0 16GT/s  
TX/RX/Testing



Booth #8



- **Industry leading support for PCIe® Technology & NVMe®**
  - PCIe 4.0 specification, NVMe, AHCI, SRIOV, MRIOV, etc
- **Part of a complete Verification IP solution**
  - Protocols: AMBA®, Display, Ethernet, MIPI®, PCIe architecture, USB, etc.
  - Memory models: DDR, HBM, WideIO, SD, ONFI, etc
- **Architected for rapid productivity**
  - Standards based SV UVM support
  - **New** configuration GUI
  - **New** sequence library
- **Complete protocol assurance**
  - Comprehensive test suite, checking & coverage
- **High performance verification**
  - Optimized simulation models
  - Synthesizable transactors for testbench acceleration
  - Virtual models for Acceleration and ICE



PLDA launches Inspector for PCIe technology, a Plug & Play **PCIe 4.0 16GT/s host platform** with built-in PCIe traffic monitoring, ideal for:

- Interoperability validation of PCIe endpoints (up to PCIe 4.0 architecture)
- Real-time benchmarking and performance monitoring
- Applications performance optimization
- Early PCIe 4.0 software development
- Performance validation of PCIe 4.0 PoCs



## Viavi Solutions Storage Network Test Solutions

- Gold Sponsor
- Viavi provides storage network testing solutions for PCIe® technology, NVMe, Fibre Channel and ethernet
- Viavi announces Xgig 4K16 PCI Express 4.0 Protocol Analyzer/Jammer
- Single platform offers simultaneous protocol analysis and error injection for PCIe 4.0 technology traffic at all layers of the stack



VI.VI

Booth #5

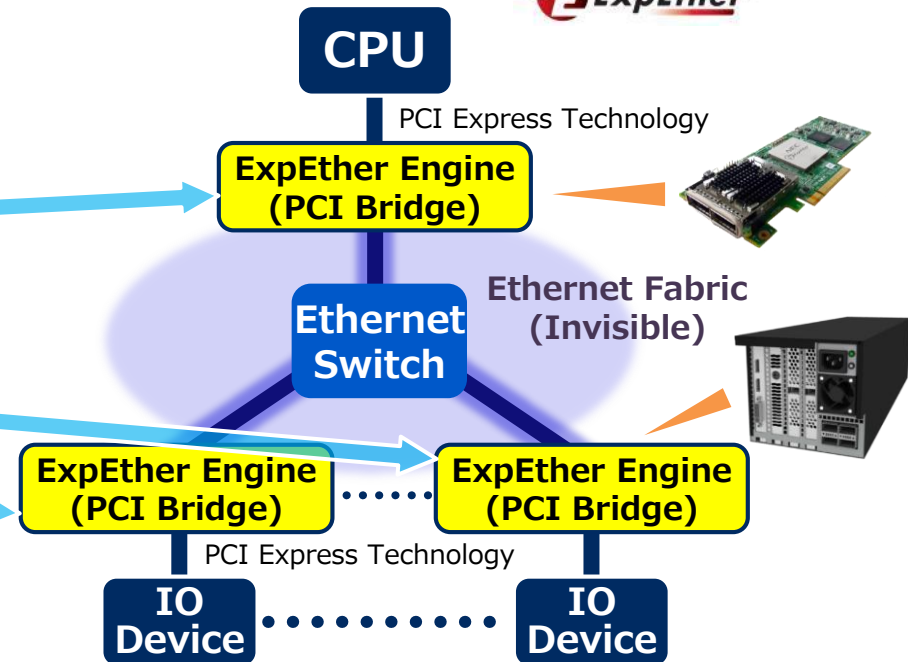
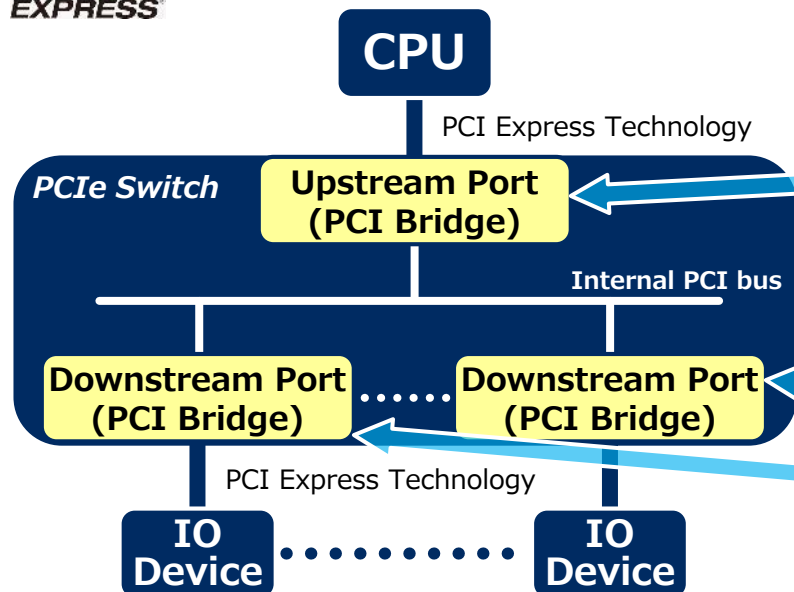
## PCI Express® Technology Solution

- Broad portfolio of PCI Express (PCIe) products in the industry including timing, switching, muxing and signal conditioning to support up to 16Gbps.
- [Timing ICs](#) (PCIe 2.0 and PCIe 3.0-based architectures) minimize clock jitter that can degrade signal integrity at the source
- [ReDrivers / Repeaters](#) (PCIe 2.0 and PCIe 3.0-based architectures) compensate for known channel losses at the transmitter and restore signal integrity at the receiver
- [Signal Switches / Multiplexers](#) (PCIe 2.0, PCIe 3.0 and PCIe 4.0-based solutions) provide efficient and clear signal routing
- [Packet Switches](#) (PCIe 2.0-based architecture) efficiently aggregate multiple I/O devices without compromising signal integrity
- [Bridges](#) (PCIe to UART/USB/PCI/PCI-X) enable reliable, turn-key connectivity between PCIe hosts and legacy peripherals

## ExpEther – Expansion of PCIe® Switch over Ethernet

ExpEther Engine is seen as PCIe Switch from CPU

- Ethernet region is invisible from the CPU



ExpEther is fully compatible with PCIe Specification

NEC

Booth #7

# PCI-SIG® Exhibiting Member Companies



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**SYNOPSYS**®  
*Silicon to Software™*

 **TELEDYNE LECROY**  
Everywhere you look™

## Gold Sponsors

**avery**  
design systems

 **KEYSIGHT**  
TECHNOLOGIES

**Mentor**  
**Graphics**®

  
**VIavi**

## Exhibitors

**DIODES**  
INCORPORATED

**NEC**

**Tektronix**®

# PCI-SIG® DevCon Schedule



## Lunch and Exhibit

11:30 a.m. – 1:00 p.m.



## Conference Sessions

1:00 p.m. – 3:00 p.m.



## Afternoon Break and Exhibit

3:00 p.m. – 3:30 p.m.



## Conference Sessions

3:30 p.m. – 4:30 p.m.



## PCI-SIG 25<sup>th</sup> Anniversary Party

5:30 p.m. – 8:00 p.m.

# Conference Sessions



**The following sessions are open for press attendance:**

**Wednesday, June 7**

## **Track 2: PCI-SIG Architecture**

- 1:00-2:00 p.m. – PCI Express Basics
- 3:30-4:30 p.m. – M.2 Updates

## **Track 3: Member Implementation**

- 2:00-3:00 p.m. – In-system Debugging of PCIe Devices
- 3:30-4:30 p.m. – Performance Tuning PCIe Systems

*Note: Thursday, June 8 is closed to press*