PCI-SIG® DevCon 2017 UPDATE

AL YANES

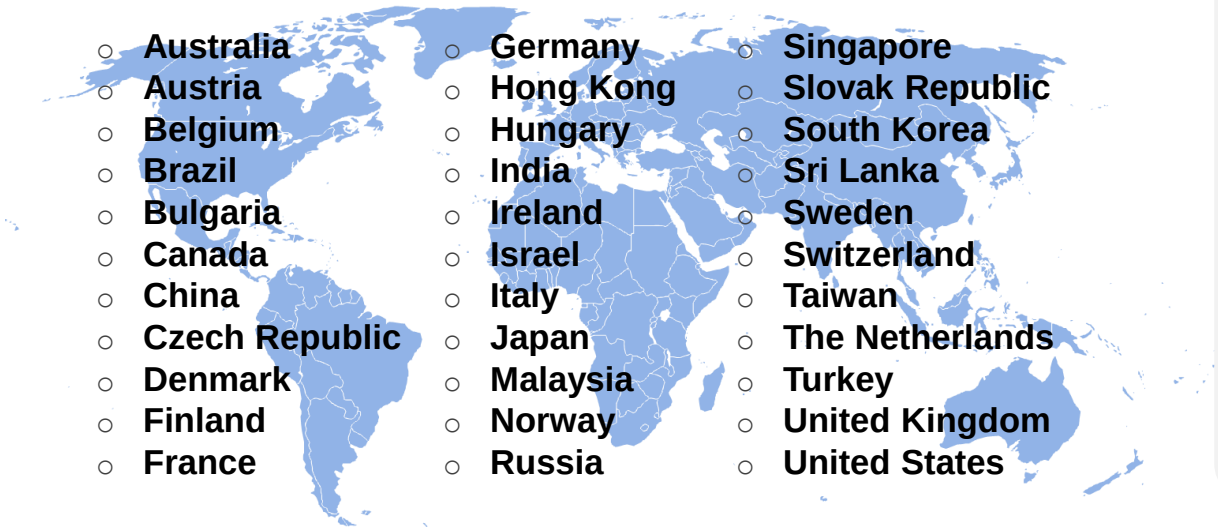
President and Chairman

PCI-SIG® Snapshot

Organization that **defines the PCI Express I/O bus specifications and related form factors.**

- **730+** member companies located worldwide

Creating specifications and mechanisms to **support compliance** and **interoperability.**



- Australia
- Austria
- Belgium
- Brazil
- Bulgaria
- Canada
- China
- Czech Republic
- Denmark
- Finland
- France
- Germany
- Hong Kong
- Hungary
- India
- Ireland
- Israel
- Italy
- Japan
- Malaysia
- Norway
- Russia
- Singapore
- Slovak Republic
- South Korea
- Sri Lanka
- Sweden
- Switzerland
- Taiwan
- The Netherlands
- Turkey
- United Kingdom
- United States

BOARD OF DIRECTORS 2017-2018

AMD
DELL
Hewlett Packard Enterprise
IBM
intel
lenovo
NVIDIA
QUALCOMM®
SYNOPSYS®
Silicon to Software™

PCI Express 4.0

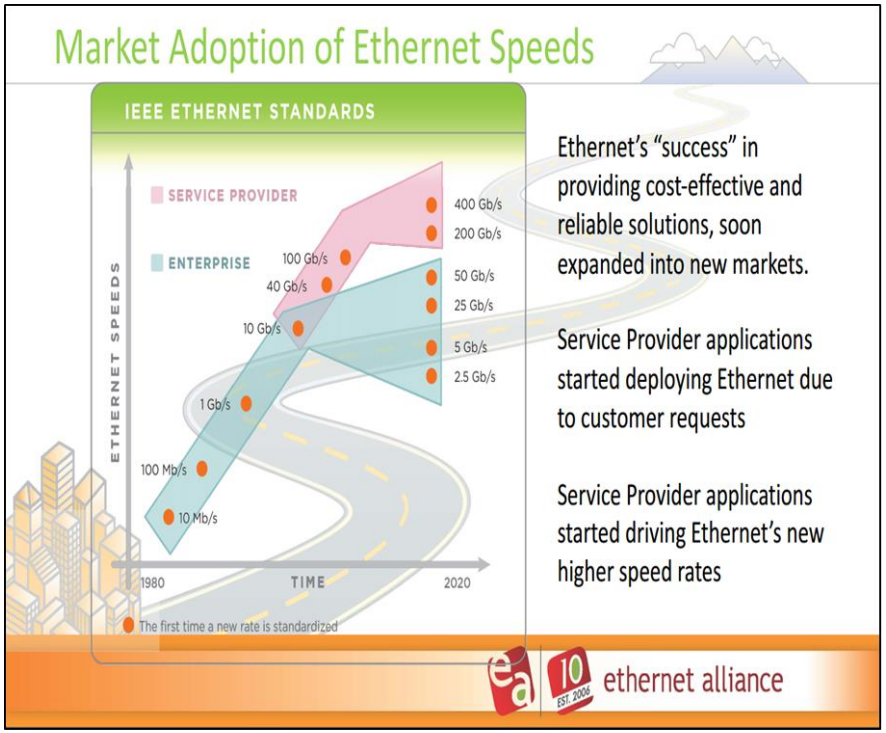
PCI-SIG continues its solid reputation of delivering **low cost, high-performance, low-power specifications** for **multiple applications** and **markets.**

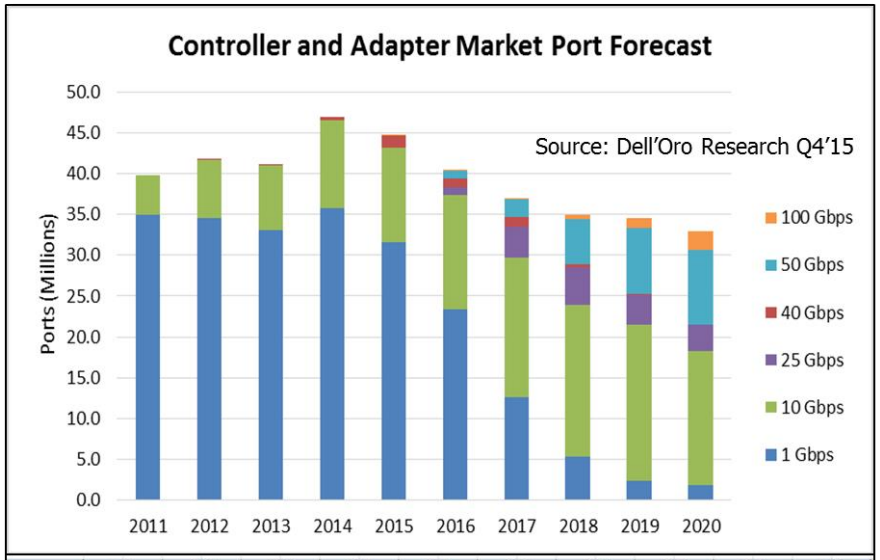
- **PCI Express 4.0 Specification – (16GT/s)**
  - Feature complete Revision 0.9 released for final IP review
  - Includes new performance enhancements
  - Maintains position as the interconnect of choice for the expansive storage market and the backbone for the fast growing cloud ecosystem

PCI Express 4.0

- **PCIe 4.0 Key Functional Enhancements**
  - Lane Margining at the Receiver
    - Allows the system to determine how close to “the edge” each lane is operating under real conditions
  - Expanded Tag and Credits
    - Allows both tags and credits to expand to service devices well into the foreseeable future
- **PCIe 4.0 Adoption**
  - Numerous vendors confirmed with 16GT/s PHYs in silicon
  - Major IP vendors offering 16GT/s controllers
  - Dozen 16GT/s solutions at a recent PCI-SIG Compliance Workshop
  - Several DevCon exhibitors with 16GT/s demos

Ethernet Evolution





	2011		2012		2013		2014		2015		2016		2017		2018		2019		2020	
	Ports	BW	Ports	BW	Ports	BW	Ports	BW	Ports	BW	Ports	BW	Ports	BW	Ports	BW	Ports	BW	Ports	BW
1	35	35	34	34	34	34	35.5	35.5	31	31	23	23	12	12	5	5	2	2	1.5	1.5
10	5	50	8	80	8	80	10	100	11	110	14	140	18	180	23	230	20	200	18	180
25	0	0	0	0	0	0	0.5	12.5	2	50	1	25	4	100	5	125	3	75	3	75
40	0	0	0	0	0	0	0	0	0	0	1	40	1	40	1	40	0.5	20	0	0
50	0	0	0	0	0	0	0	0	0	0	1	50	2	100	6	300	8	400	9	450
100	0	0	0	0	0	0	0	0	0	0	0	0	0.1	10	0.5	50	1	100	2	200
Total Gbps		85		114		114		148		191		278		442		750		797		906.5
YOY Ratio		N/A		1.3		1.0		1.3		1.3		1.5		1.6		1.7		1.1		1.1
3 Year Ratio								**1.7**						**3.0**						**2.1**

PCI Express – Future

- **PCI Express 5.0 Specification with 32GT/s Bandwidth**
  - Revision 0.3 has already been delivered to PCI-SIG members
  - Ideal for:
    - Applications such as artificial intelligence, machine learning, gaming, visual computing, storage and networking
    - High-end networking solutions (i.e. 400Gb Ethernet and dual 200Gb/s InfiniBand solutions)
    - Accelerator and GPU attachments for high-bandwidth solutions
    - Constricted form factor applications that cannot increase width and need higher frequency to achieve performance

PCIe 5.0 Delivering 32GT/s

✓ **Supports 400Gb Ethernet Solutions**

- 400Gb = 50GB
- 50GB in both directions

✓ **Full Duplex**

- 128/130 bit encoding with 1.5% overhead
- x16 ~64GB/s sufficient to support 400Gb Ethernet solutions (64GB > 50 GB)
- Total Full Duplex = ~128GB

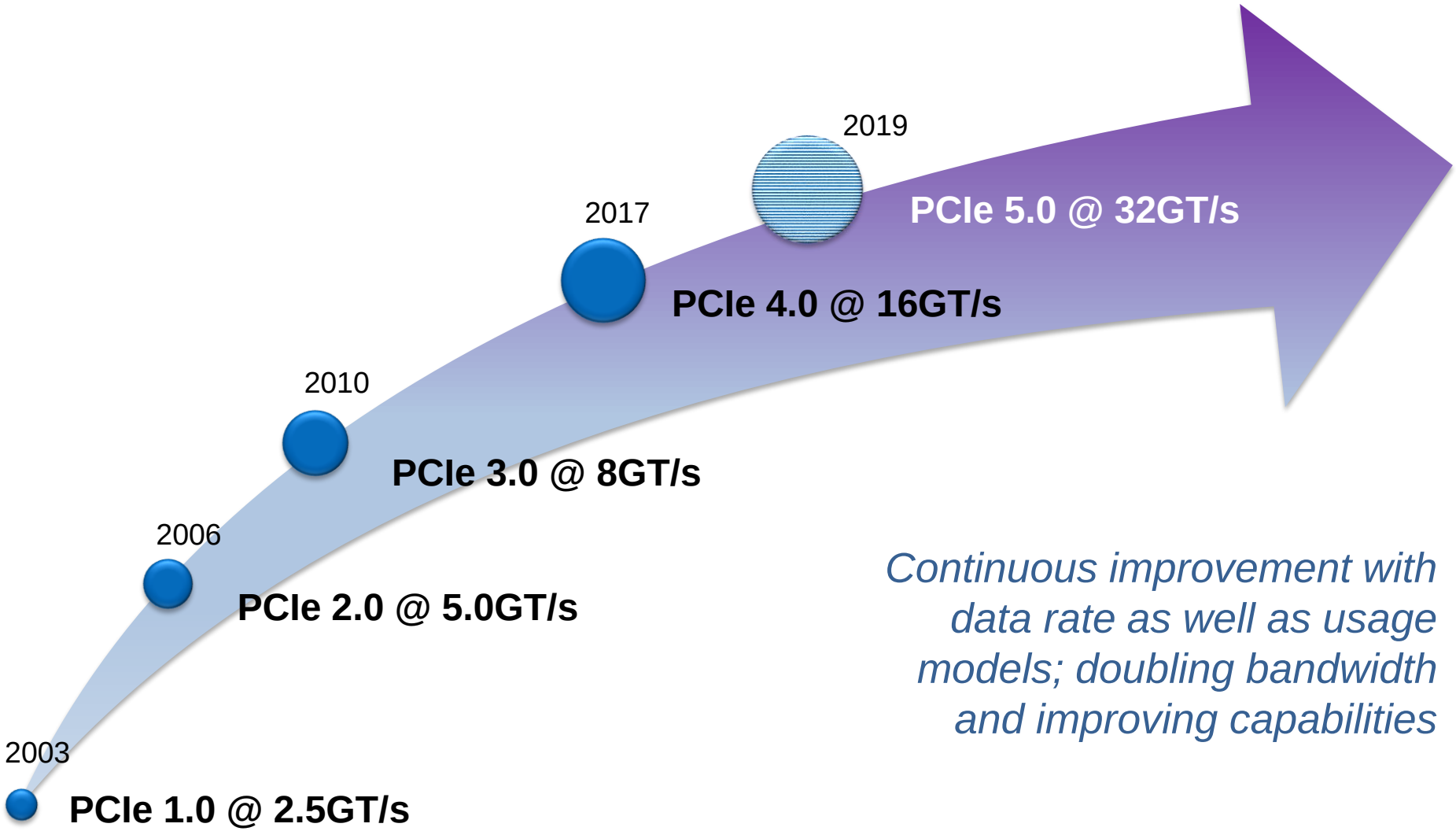
- CEM connector targeted to be backwards compatible for add-in cards
- **Targeted Release in 2019**

	RAW BIT RATE	LINK BW	BW/ LANE/WAY	TOTAL BW X16
PCIe 1.x	2.5GT/s	2Gb/s	250MB/s	8GB/s
PCIe 2.x	5.0GT/s	4Gb/s	500MB/s	16GB/s
PCIe 3.x	8.0GT/s	8Gb/s	~1GB/s	~32GB/s
PCIe 4.0	16GT/s	16Gb/s	~2GB/s	~64GB/s
PCIe 5.0	32GT/s	32Gb/s	~4GB/s	~128GB/s

PCIe Bandwidth & Frequency

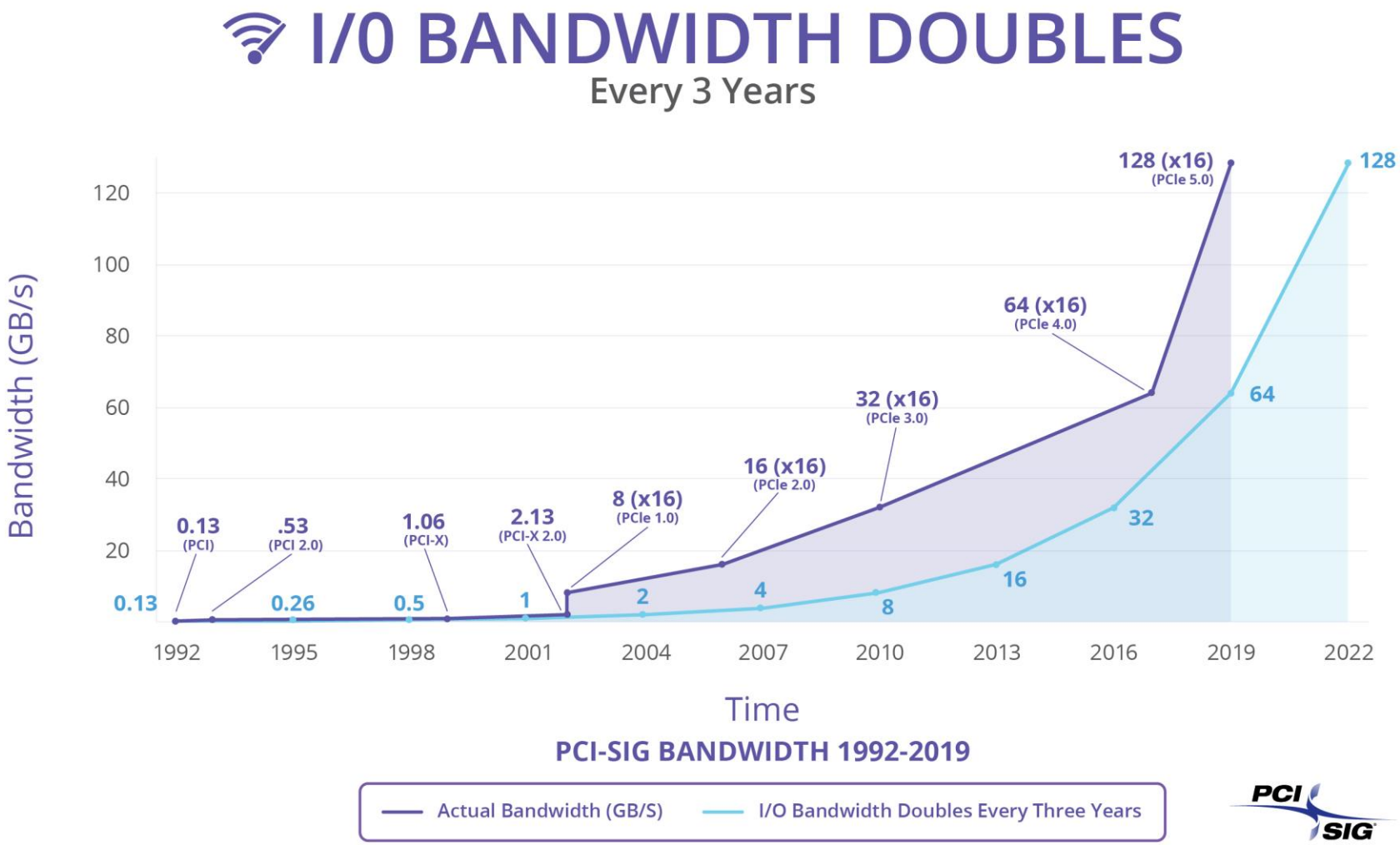
Year	Bandwidth	Frequency/Speed
1992	133MB/s (32 bit simplex)	33 Mhz (PCI)
1993	533MB/s (64 bit simplex)	66 Mhz (PCI 2.0)
1999	1.06GB/s (64 bit simplex)	133 Mhz (PCI-X)
2002	2.13GB/s (64 bit simplex)	266 Mhz (PCI-X 2.0)
2002	8GB/s (x16 duplex)	2.5 GHz (PCIe 1.x)
2006	16GB/s (x16 duplex)	5.0 GHz (PCIe 2.x)
2010	32GB/s (x16 duplex)	8.0 GHz (PCIe 3.x)
2017	64GB/s (x16 duplex)	16.0 GHz (PCIe 4.0)
2019	128GB/s (x16 duplex)	32.0 GHz (PCIe 5.0)

PCIe® Roadmap



Continuous improvement with data rate as well as usage models; doubling bandwidth and improving capabilities

PCI-SIG History



2017 PCI-SIG® DevCon Sponsor & Exhibiting Companies

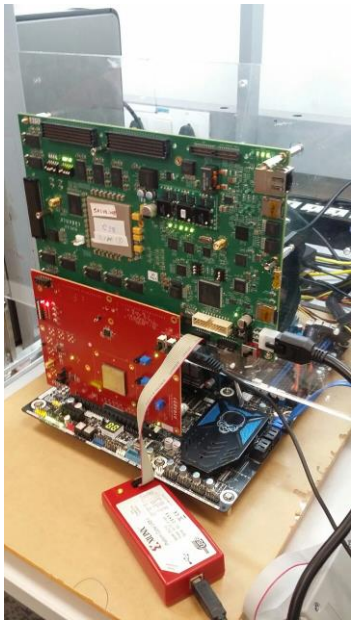
Company Presenters

Platinum	cadence	**Booth 3** – Sachin Dhingra, Senior Product Marketing Manager
	SYNOPSYS® Silicon to Software™	**Booth 2** – Scott Knowlton, Senior Product Marketing Manager
	TELEDYNE LECROY Everywhereyoulook™	**Booth 4** – John Wiedemeier, Product Marketing Manager
Gold	KEYSIGHT TECHNOLOGIES	**Booth 8** – Rick Eads, Principal PCI Express Solutions Planner
	Mentor Graphics®	**Booth 9** – Jason Polychronopoulos, Mgr. Verification IP Solutions
	PLDA	**Booth 12** – Stephane Hauradou, Co-founder
	VIAVI	**Booth 5** – Rob Venzina, Senior Application Engineer
Exhibitor	DIODES INCORPORATED	**Booth 1** – Kay Annamalai, Senior Marketing Director
	NEC	**Booth 7** – Gursimranjit Singh, Senior Systems Engineer

Cadence

Cadence IP Solution for PCI Express® 4.0 Architecture

- **Complete, integrated, pre-verified Cadence® IP solution**
  - High-performance, low-latency controller
  - Multi-link, multi-protocol PHY
  - Verification IP with extensive test suite and debug utilities
- **Application-optimized solutions**
  - Enterprise
    - Multi-packet design allows >95% link utilization
    - Flexible PHY configurations to maximize utilization of bandwidth
  - Mobile
    - Lowest active power with L0 state power
    - Lowest area and flexible placement for smallest overall SoC
  - Automotive
    - First PCIe® 4.0 PHY audited by SGS-TÜV and deemed ASIL-B ready
    - Solution supports comprehensive automotive safety features
- **Technical presentation**
  - *Challenges and Techniques for Implementing Lane Margining – Gopi K, Architect*



cadence

Booth #3

Synopsys

Finish First with DesignWare IP Solutions for PCIe® Technology

Validated in Over 1500 Designs & Shipping Billions of Units

- **PCIe® 4.0 Architecture Ready**
  - PHYs, controllers, verification IP & IP prototyping kits conforming to the 0.7 revision of the PCIe 4.0 specification
  - Validated PCIe 4.0 testing and interoperability with ecosystem partners: Mellanox, Teledyne LeCroy and more
    - Demos: Full system PCIe 4.0 interoperability @ 16GT/s with Mellanox; DesignWare® PHY IP; verification IP

News

- **Automotive Ready**
  - Certified PHY and controller IP solutions meet automotive functional safety, reliability and temperature requirements
    - Demo: Reliability, debug, error injection features

News

In position to lead the industry in powering next-gen products beyond 16GT/s

SYNOPSYS®
Silicon to Software™

Booth #2

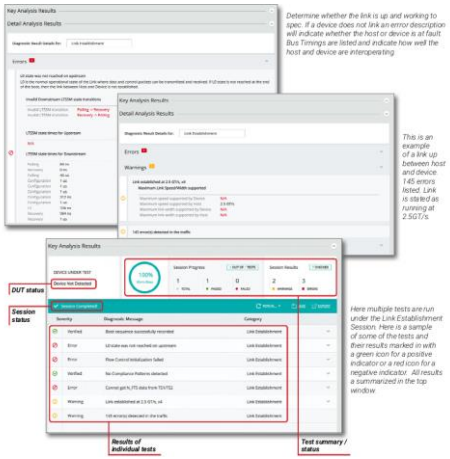
Teledyne LeCroy

PCIe® 4.0 Protocol Test Equipment

Summit T416
Protocol Analyzer

Summit Z416
Protocol Exerciser

Link Expert



Makes Protocol Analysis Easy

PCIe technology with SMBus Support

90° Rack Mount

Standard
Interposer

PCIe External
Cable 3.0
Interposer

M.2
Interposer

U.2(SFF-8639) 5”

SFF-8639
Dual12”
Interposer

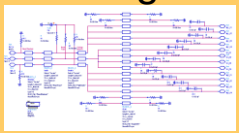
TELEDYNE LECROY
Everywhereyoulook™

Booth #4

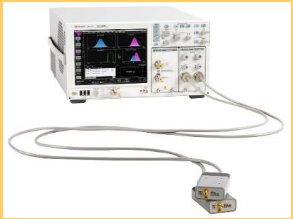
Keysight Technologies

PCI Express® 4.0 Technology – Keysight Total Solution

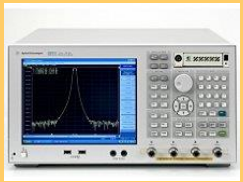
Physical layer – interconnect design



ADS design software



86100D DCA-X/TDR

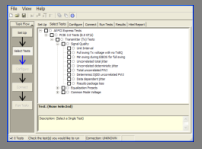


E5071C ENA option TDR

Verify PCIe 4.0 Compliant Channels
Verify Return Loss Compliance

Physical layer-transmitter test

V-Series, Z-Series Real-Time Oscilloscopes



N5393F PCI Express 4.0 TX Electrical compliance software

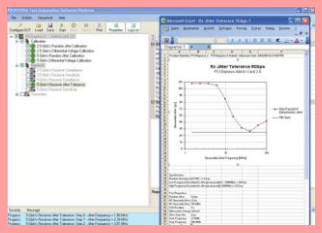
86100CU-400 PLL and Jitter Spectrum Measurement SW

DSA V-series & Z-Series Real-Time Oscilloscopes

Physical layer-receiver test

M8020A J-BERT High Perfformance, Protocol Aware BERT

N5990A automated compliance and device characterization test software



Automated RX Test software
- Accurate, Efficient
- Comprehensive RX Testing

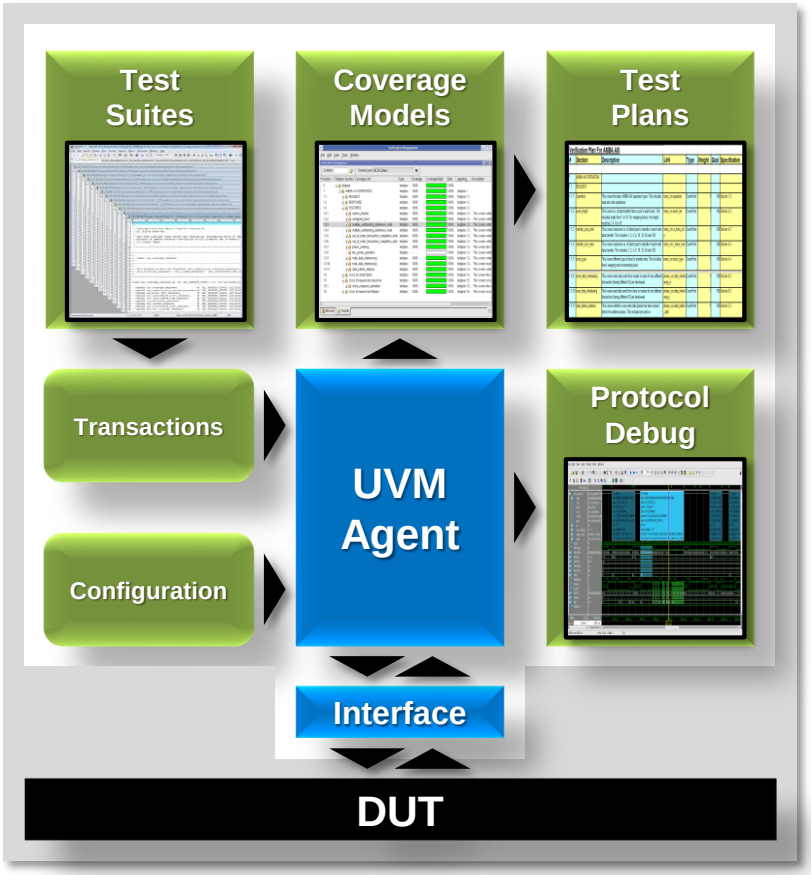
PCIe 4.0 16GT/s TX/RX/Testing

KEYSIGHT TECHNOLOGIES

Booth #8

Mentor Graphics

- **Industry leading support for PCIe® Technology & NVMe®**
  - PCIe 4.0 specification, NVMe, AHCI, SRIOV, MRIOV, etc
- **Part of a complete Verification IP solution**
  - Protocols: AMBA®, Display, Ethernet, MIPI®, PCIe architecture, USB, etc.
  - Memory models: DDR, HBM, WideIO, SD, ONFI, etc
- **Architected for rapid productivity**
  - Standards based SV UVM support
  - **New** configuration GUI
  - **New** sequence library
- **Complete protocol assurance**
  - Comprehensive test suite, checking & coverage
- **High performance verification**
  - Optimized simulation models
  - Synthesizable transactors for testbench acceleration
  - Virtual models for Acceleration and ICE



Booth #9

PLDA

- **PLDA launches PCIe Inspector, a Plug & Play PCIe 4.0 16GT/s host platform with built-in PCIe traffic monitoring, ideal for:**
  - Interoperability validation of PCIe endpoints (up to PCIe 4.0 architecture)
  - Real-time benchmarking and performance monitoring
  - Applications performance optimization
  - Early PCIe 4.0 software development
  - Performance validation of PCIe 4.0 PoCs

Booth #12

Viavi

Viavi Solutions Storage Network Test Solutions

- Gold Sponsor
- Viavi provides storage network testing solutions for PCIe® technology, NVMe, Fibre Channel and ethernet
- Viavi announces Xgig 4K16 PCI Express 4.0 Protocol Analyzer/Jammer
- Single platform offers simultaneous protocol analysis and error injection for PCIe 4.0 technology traffic at all layers of the stack

Booth #5

Diodes Incorporated

PCI Express® Technology Solution

- Broad portfolio of PCI Express (PCIe) products in the industry including timing, switching, muxing and signal conditioning to support up to 16Gbps.
- Timing ICs (PCIe 2.0 and PCIe 3.0-based architectures) minimize clock jitter that can degrade signal integrity at the source
- ReDrivers / Repeaters (PCIe 2.0 and PCIe 3.0-based architectures) compensate for known channel losses at the transmitter and restore signal integrity at the receiver
- Signal Switches / Multiplexers (PCIe 2.0, PCIe 3.0 and PCIe 4.0-based solutions) provide efficient and clear signal routing
- Packet Switches (PCIe 2.0-based architecture) efficiently aggregate multiple I/O devices without compromising signal integrity
- Bridges (PCIe to UART/USB/PCI/PCI-X) enable reliable, turn-key connectivity between PCIe hosts and legacy peripherals

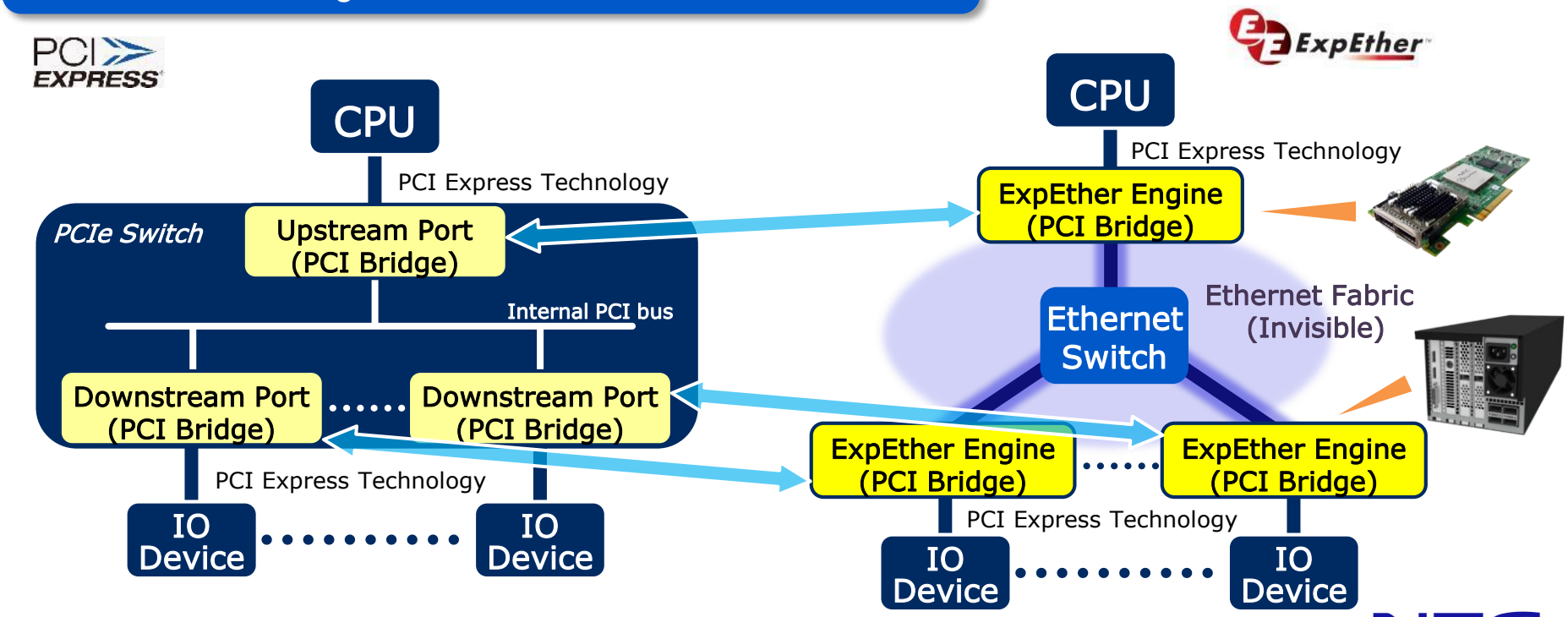
Booth #1

NEC

ExpEther – Expansion of PCIe® Switch over Ethernet

ExpEther Engine is seen as PCIe Switch from CPU

- Ethernet region is invisible from the CPU



ExpEther is fully compatible with PCIe Specification

NEC

Booth #7

PCI-SIG® Exhibiting Member Companies

Platinum Sponsors

cadence™

SYNOPSYS®
Silicon to Software™

TELEDYNE LECROY
Everywhereyoulook™

Gold Sponsors

avery design systems

KEYSIGHT TECHNOLOGIES

Mentor Graphics®

PLDA

VIAVI

Exhibitors

DIODES INCORPORATED

NEC

Tektronix®

PCI-SIG® DevCon Schedule

Lunch and Exhibit

11:30 a.m. – 1:00 p.m.

Conference Sessions

1:00 p.m. – 3:00 p.m.

Afternoon Break and Exhibit

3:00 p.m. – 3:30 p.m.

Conference Sessions

3:30 p.m. – 4:30 p.m.

PCI-SIG 25th Anniversary Party

5:30 p.m. – 8:00 p.m.

Conference Sessions

The following sessions are open for press attendance:

Wednesday, June 7

Track 2: PCI-SIG Architecture
- 1:00-2:00 p.m. – PCI Express Basics
- 3:30-4:30 p.m. – M.2 Updates

Track 3: Member Implementation
- 2:00-3:00 p.m. – In-system Debugging of PCIe Devices
- 3:30-4:30 p.m. – Performance Tuning PCIe Systems

Note: Thursday, June 8 is closed to press