



STORAGE DEVELOPER CONFERENCE

SNIA ■ SANTA CLARA, 2015

# PCI Express® Architecture: Driving the Future of Storage I/O



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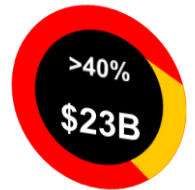
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# Agenda

- **Recent Storage Industry Trends**
- PCIe™ Technology as Storage Interconnect
- Summary & Call to Action

# Storage Industry Trends

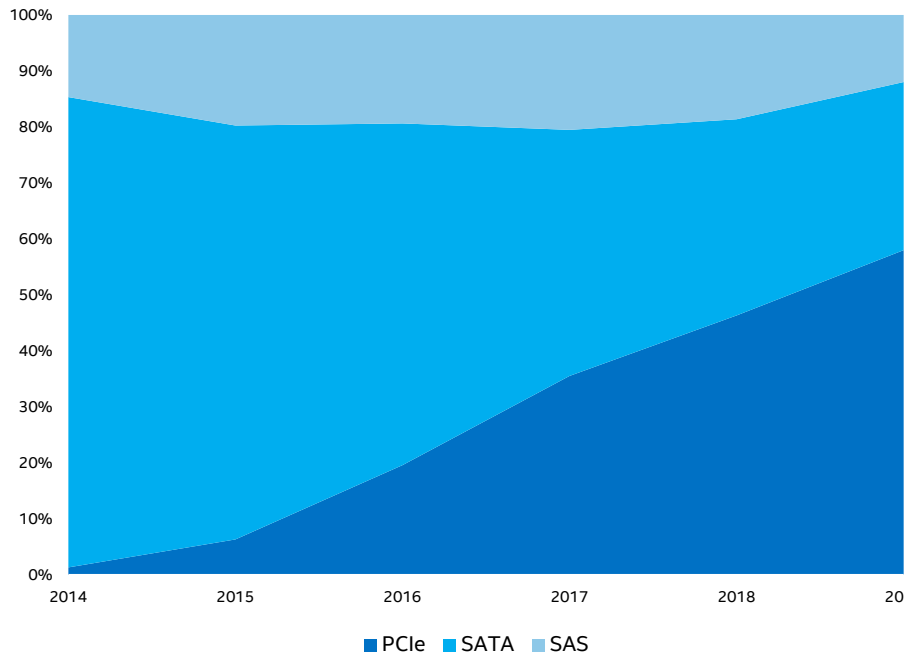
- ❑ Massive growth in data driving SSD adoption
  - ❑ Anticipated growth to \$10B by 2018
- ❑ Robust growth in Data Center Storage TAM
  - ❑ SSD adoption growing at faster than 40%
- ❑ Accelerating NVMe\* adoption in Data Center
  - ❑ Over half of Data Center SSDs by 2017



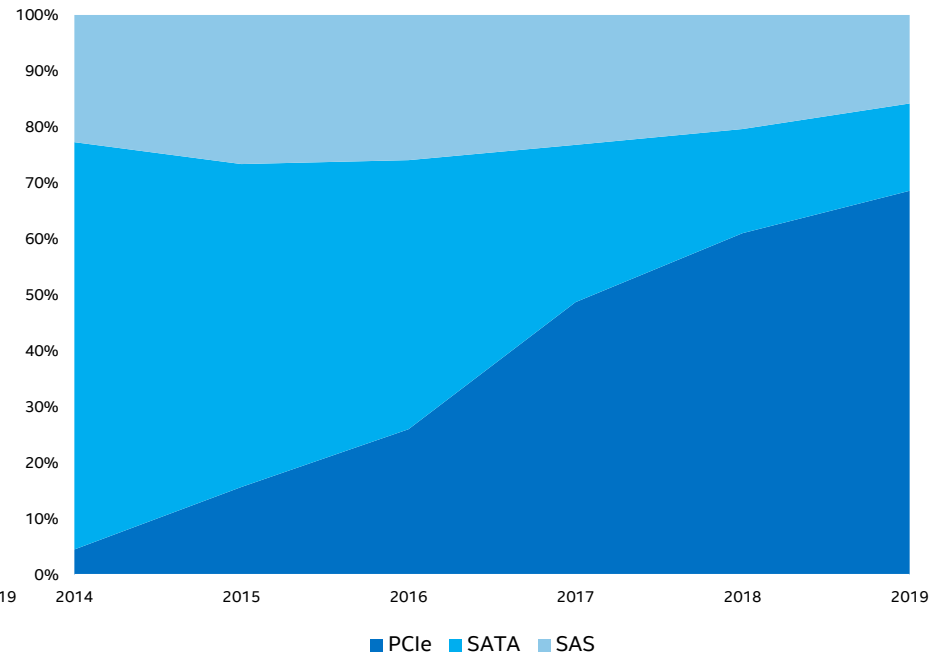
# Storage Industry Trends

- PCIe adoption pace makes it the interconnect for storage
  - Outpacing other interconnects in both units and bandwidth/capacity

Data Center SSD Units by Interface



Data Center SSD total GB by Interface



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# PCIe I/O for Storage – Performance

- ❑ PCIe 4.0 specification
  - ❑ 16GT/s performance w/ high-volume manufacturability
  - ❑ Backwards compatible to PCIe 1/2/3
  - ❑ Standardized repeater for long channels (>10", 1 connector)
  - ❑ Base spec on track for rev0.7 maturity by 4Q'15-1Q'16

|          | Raw Bit Rate | Link BW | BW/Lane/Way | Total BW x16 |
|----------|--------------|---------|-------------|--------------|
| PCIe 1.x | 2.5GT/s      | 2Gb/s   | ~250MB/s    | ~8GB/s       |
| PCIe 2.x | 5.0GT/s      | 4Gb/s   | ~500MB/s    | ~16GB/s      |
| PCIe 3.x | 8.0GT/s      | 8Gb/s   | ~1GB/s      | ~32GB/s      |
| PCIe 4.0 | 16GT/s       | 16Gb/s  | ~2GB/s      | ~64GB/s      |

- ❑ Near-0 link idle power
  - ❑ L1 Sub-states ECN published in 2014
- ❑ ½ swing spec for lower link active power
  - ❑ Available since PCIe 1.1 (circa 2004)

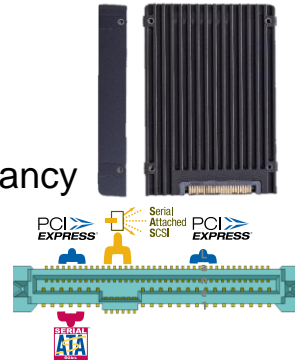
| Sub-state |      | Status |          |     | Targets      |              |
|-----------|------|--------|----------|-----|--------------|--------------|
| Link      | PHY  | PLL    | Tx/Rx    | CM  | 1-Lane Power | Exit Latency |
| L1        | P1   | On/Off | Off/Idle | On  | ~10mW        | <5µs         |
| L1.1      | P1.1 | Off    | Off      | On  | <500µW       | <20µs        |
| L1.2      | P1.2 | Off    | Off      | Off | <10µW        | <70µs        |

- ❑ M-PCIe™ for PCIe functionality where M-PHY\* exists

# PCIe I/O for Storage – CEM++ Expansion

## ❑ SFF-8639 (U.2)

- ❑ Dense packing 2.5" SSDs, hot-plug, serviceable, x1/x2/x4, multi-topology, compliancy



## ❑ M.2

- ❑ 42/80/110mm, boot or max storage density, client & server compliancy, compliancy

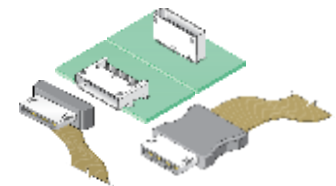


## ❑ BGA

- ❑ For volume-constrained mobile platforms, saves 0.5-1.5mm on Z-height and ~20% on area

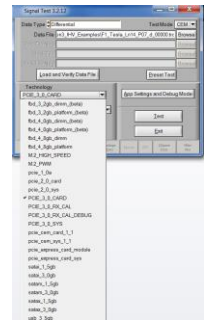
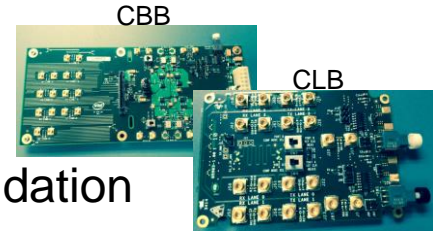
## ❑ OCuLink w/ SRIS

- ❑ Low-cost, low EMI, x1/x2/x4, internal cabling for SATA transition



# PCIe I/O for Storage – Compliance

- ❑ Industry-leading compliance program
  - ❑ MB & AIC test fixtures – Test channels for silicon validation
  - ❑ Sigtest – Jitter/voltage noise separation for signal integrity
  - ❑ CV – Configuration space verifier
  
- ❑ SFF-8639 (U.2) & M.2 also supported
  - ❑ PCI-SIG extending its C&I program to SFF (U.2) & M.2
  - ❑ Initial SFF (U.2) C&I testing completed in August 2015
  - ❑ Future C&I workshops will integrate M.2 testing





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# Summary

- ❑ SSD attach is transitioning to PCIe interconnect
- ❑ PCIe architecture is all you need for storage applications in any device or system topology
  - ❑ PCI-SIG has numerous form factors for increased flexibility in storage I/O expansion
  - ❑ PCI-SIG has robust compliance program for end-to-end interoperability
- ❑ PCIe 4.0 architecture provides unbeatable performance headroom with low power features

Visit [www.pcisig.com](http://www.pcisig.com) for more info on PCIe technology!

10